TPS715A, 24-V High Input Voltage, Micropower, 80-mA LDO Voltage Regulator

1 Features

- 24 V Maximum Input Voltage
- Low 3.2-µA Quiescent Current at 80 mA
- Stable With Any Capacitor (≥ 0.47 µF)
- 80-mA Specified Current
- Available in Fixed and Adjustable (1.2 V to 15 V) Versions
- Specified Current Limit
- 3-mm × 3mm and 2-mm × 2-mm SON Packages
- –40°C to 125°C Specified Junction Temperature Range
- For MSP430-Specific Output Voltages See the TPS715xx

2 Applications

- Ultralow Power Microcontrollers
- Industrial and Automotive Applications
- PDAs
- Portable, Battery-Powered Equipment
- Medical Imaging

3 Description

The TPS715A low-dropout (LDO) voltage regulators offer the benefits of high input voltage, low-dropout voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor (≥ 0.47 µF). The high maximum input voltage combined with excellent power dissipation capability makes this part particularly well-suited to industrial and automotive applications.

A PMOS pass element behaves as a low-value resistor. The low dropout voltage, typically 670 mV at 80 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 µA typically) is nearly constant over the entire range of output load current (0 mA to 80 mA).

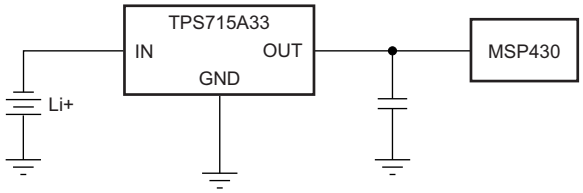
The TPS715A is available in 3-mm × 3-mm package ideal for high power dissipation and small 2-mm × 2-mm package ideal for handheld and ultra-portable applications. The 3-mm × 3-mm package is also available as a non-magnetic package for medical imaging applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS715A	SON (8)	3.00 mm × 3.00 mm
	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

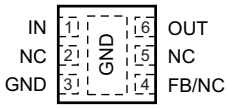
Changes from Revision F (October 2012) to Revision G	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision E (June 2011) to Revision F	Page
• Updated Figure 15.	10

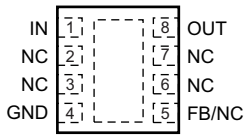
Changes from Revision D (May, 2007) to Revision E	Page
• Added last Applications bullet	1
• Added last sentence to Description section	1

5 Pin Configuration and Functions

DRV Package
6-Pin SON
Top View



DRB Package
8-Pin SON
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	8-PIN SON		6-PIN SON			
	FIXED	ADJ.	FIXED	ADJ.		
FB	—	4	—	5	I	Adjustable version. This terminal is used to set the output voltage.
GND	3, Pad	3, Pad	4, Pad	4, Pad	—	Ground
NC	2, 4, 5	2, 5	2, 3, 5, 6, 7	2, 3, 6, 7	—	No connection. May be left open or tied to Ground for improved thermal performance.
IN	1	1	1	1	I	Unregulated input voltage.
OUT	6	6	8	8	O	Regulated output voltage, any output capacitor ≥ 0.47 µF can be used for stability.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range, unless otherwise noted.(1)

	MIN	MAX	UNIT
V_{IN}	–0.3	24	V
Peak output current	Internally limited		
Continuous total power dissipation	See *Dissipation Ratings*		
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		24	V
I_{OUT}	Output current	0		80	mA
C_{IN}	Input capacitor	0	0.047		µF
C_{OUT}	Output capacitor	0.47	1		µF

6.4 Thermal Information

THERMAL METRIC(1)		TPS715A		UNIT
		DRV (SON)	DRB (SON)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.5	69	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	110.5	76.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	44.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	8.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	44.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.3	27.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 1 µF, unless otherwise noted. The TPS715A01 device is tested with V_{OUT} = 2.8 V. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage(1)	V_{IN}	I_{OUT} = 10mA	2.5		24	V
		I_{OUT} = 80mA	3		24	
Voltage range (TPS715A01)	V_{OUT}		1.2		15	V
Output voltage accuracy(1)	TPS715A01	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, 1.2 V ≤ V_{OUT} ≤ 15V, 0 ≤ I_{OUT} ≤ 80 mA	0.96 × $V_{OUT(nom)}$	$V_{OUT(nom)}$	1.04 × $V_{OUT(nom)}$	V
	TPS715A33	4.3 V < V_{IN} < 24 V, 0 ≤ I_{OUT} ≤ 80 mA	3.135	3.3	3.465	
Output voltage line regulation(1)	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 1V < V_{IN} ≤ 24 V		20	60	mV
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 80 mA		35		mV
Dropout voltage V_{IN} = $V_{OUT(NOM)}$ – 0.1V	V_{DO}	I_{OUT} = 80 mA		670	1120	mV
Output current limit	I_{CL}	V_{OUT} = 0 V	160		1100	mA
Ground pin current	I_{GND}	T_J = –40°C to 85°C, 0 mA ≤ I_{OUT} ≤ 80 mA		3.2	4.2	µA
		0 mA ≤ I_{OUT} ≤ 80 mA		3.2	4.8	
		V_{IN} = 24 V, 0 mA ≤ I_{OUT} ≤ 80 mA			5.8	
Power-supply ripple rejection	PSRR	f = 100 kHz, C_{OUT} = 10 µF		60		dB
Output noise voltage	V_{IN}	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms

(1) Minimum V_{IN} = V_{OUT} + V_{DO}, or the value shown for Input voltage, whichever is greater.

6.6 Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JA}$°C/W	DERATING FACTOR ABOVE T_A = 25°C	T_A ≤ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
High-K(1)	DRV	65	15.4mW/°C	1.54 W	0.85 W	0.62 W
High-K(1)	DRB	40	25 mW/°C	2.50 W	1.38 W	1.00 W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

6.7 Typical Characteristics

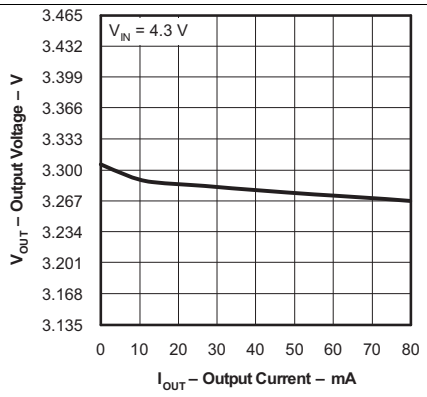


Figure 1. TPS715A33 Output Voltage vs Output Current

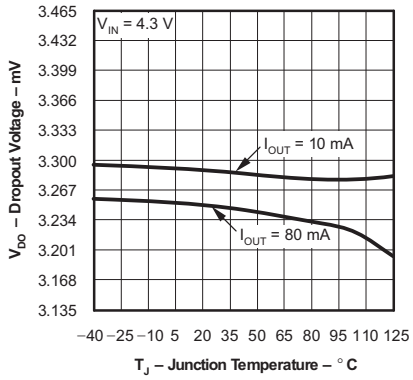


Figure 2. TPS715A33 Dropout Voltage vs Junction Temperature

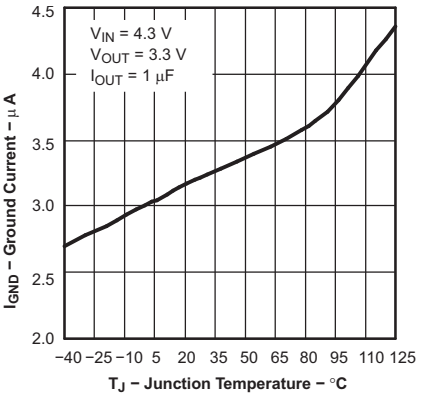


Figure 3. Ground Current vs Junction Temperature

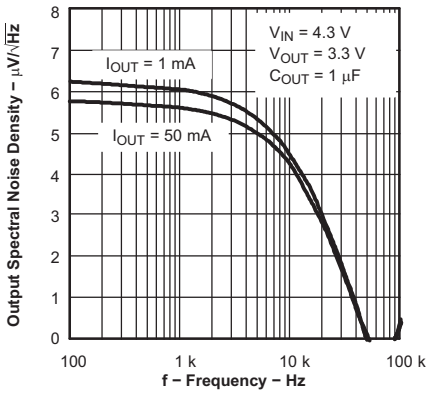


Figure 4. Output Spectral Noise Density vs Frequency

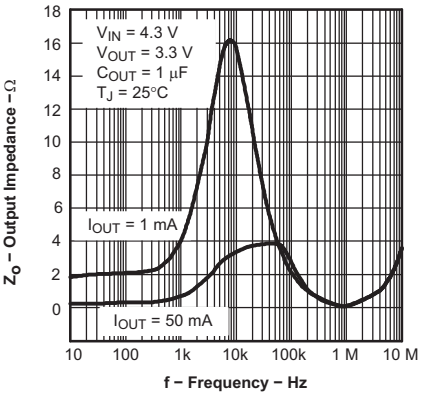


Figure 5. Output Impedance vs Frequency

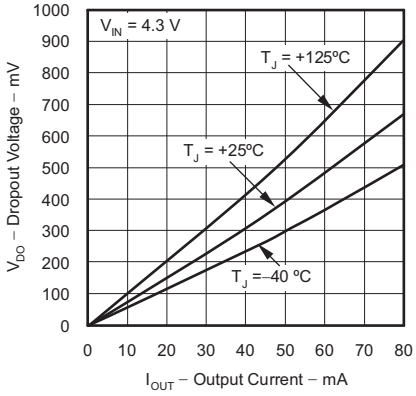


Figure 6. TPS715A33 Dropout Voltage vs Output Current

Typical Characteristics (continued)

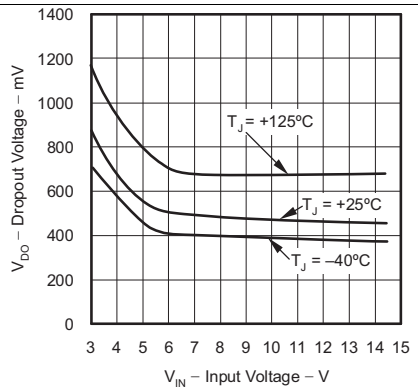


Figure 7. TPS715A01 Dropout Voltage vs Input Voltage

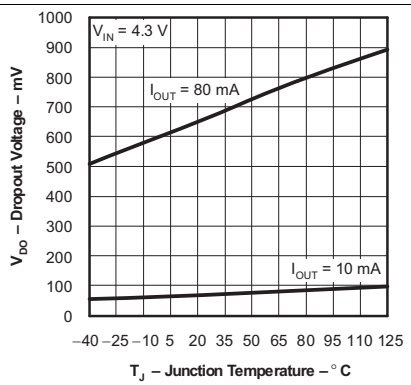


Figure 8. TPS715A33 Dropout Voltage vs Junction Temperature

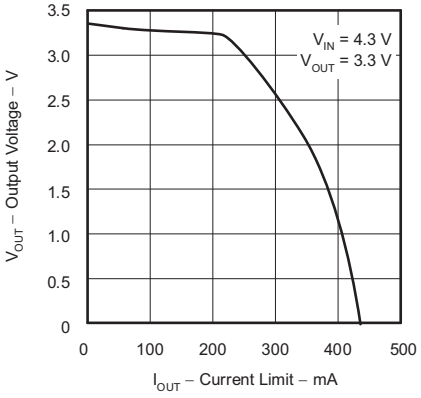


Figure 9. Output Voltage vs Current Limit

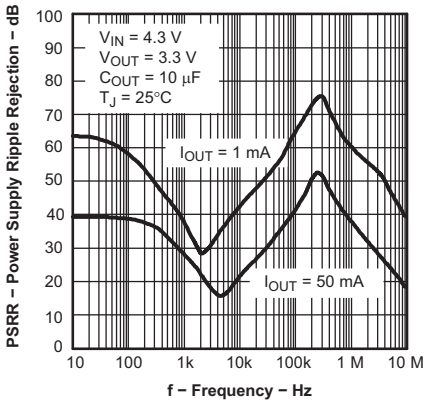


Figure 10. Power-Supply Ripple Rejection vs Frequency

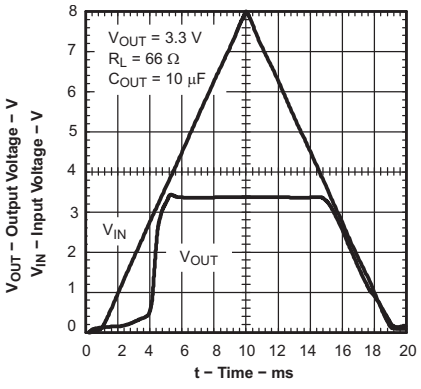


Figure 11. Power Up and Power Down

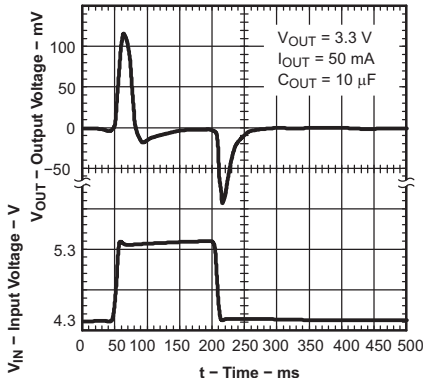


Figure 12. Line Transient Response

Typical Characteristics (continued)

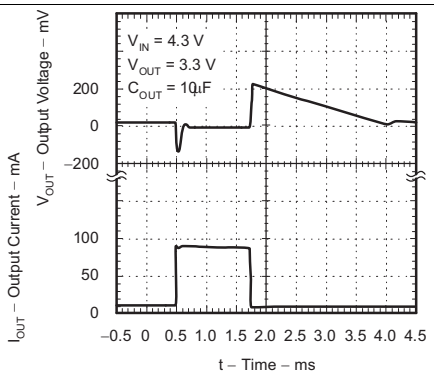


Figure 13. Load Transient Response

7 Detailed Description

7.1 Overview

The TPS715A family of low dropout regulators consume only 3.2 µA of current while offering a wide input voltage range and low-dropout voltage in a small package. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor greater than or equal to 0.47 µF. The low quiescent current makes the TPS715A ideal for powering battery management ICs. Specifically, because the TPS715A is enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery charging ICs.

7.2 Functional Block Diagrams

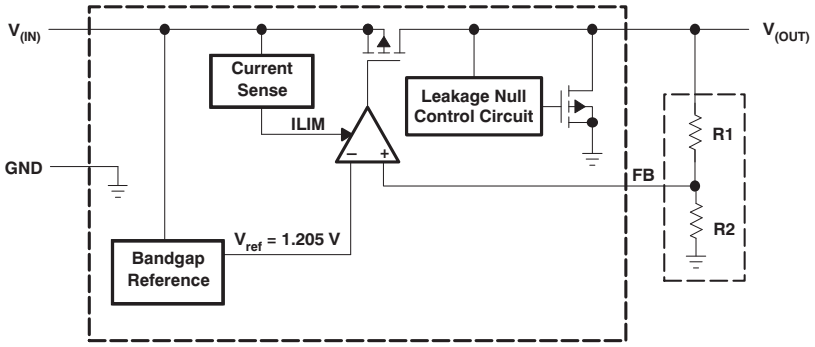


Figure 14. Functional Block Diagram—Adjustable Version

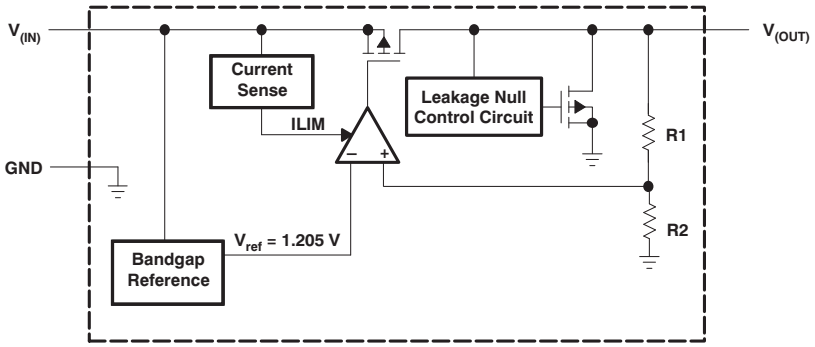


Figure 15. Functional Block Diagram—Fixed Version

7.3 Feature Description

7.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is ideal for applications that have either large transients or high DC voltage supplies.

7.3.2 Low Supply Current

This device only requires 3.2 µA (typical) of supply current and has a maximum current consumption of 5.8 µA at –40°C to 125°C.

7.3.3 Stable With Any Capacitor ≥ 0.47 µF

Any capacitor, including both ceramic and tantalum, greater than or equal to 0.47 µF properly stabilizes this loop.

Feature Description (continued)

7.3.4 Internal Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases.

NOTE

if a current limit occurs and the resulting output voltage is low, excessive power is dissipated across the LDO, resulting in possible damage to the device.

7.3.5 Reverse Current

The TPS715A device PMOS-pass transistor has a built-in back diode that conducts current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be required.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Disabled	—	—

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than 125°C.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS715A family of LDO regulators has been optimized for ultralow-power applications such as the MSP430 microcontroller. The ultralow-supply current of the TPS715A device maximizes efficiency at light loads, and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

8.2 Typical Applications

8.2.1 Typical Application (Fixed-Voltage Version)

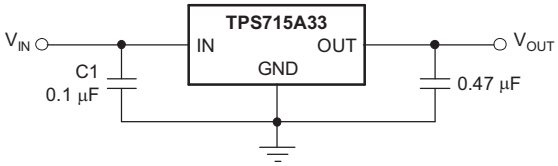


Figure 16. Typical Application Circuit (Fixed-Voltage Version)

8.2.1.1 Design Requirements

8.2.1.1.1 Power the MSP430 Microcontroller

Several versions of the TPS715A are ideal for powering the MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (TYP)	APPLICATION
TPS715A19	1.9 V	$V_{OUT(min)}$ > 1.8 V required by many MSP430s. Allows lowest power consumption operation.
TPS715A23	2.3 V	$V_{OUT(min)}$ > 2.2 V required by some MSP430s flash operation.
TPS715A30	3 V	$V_{OUT(min)}$ > 2.7 V required by some MSP430s Flash operation.
TPS715A345	3.45 V	$V_{OUT(max)}$ < 3.6 V required by some MSP430s. Allows highest speed operation.

The TPS715A family of devices offers many output voltage versions to allow designers to optimize the supply voltage for the MSP430, thereby minimizing the supply current consumed by the MSP430.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Capacitor Requirements

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS715A device requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) greater than or equal to 0.47 µF properly stabilizes this loop. TI recommends the X7R or X5R type capacitors because they have a wider temperature spec and lower temperature coefficient, but other types of capacitors may be used.

8.2.1.2.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$). However, in the *Electrical Characteristics*, V_{DO} is defined as the $V_{IN} – V_{OUT}$ voltage at the rated current, where the pass-FET is fully enhanced in the ohmic region of operation and is characterized by the classic $R_{DS(on)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(on)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. $R_{DS(on)}$ can be calculated using Equation 1.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

8.2.1.3 Application Curves

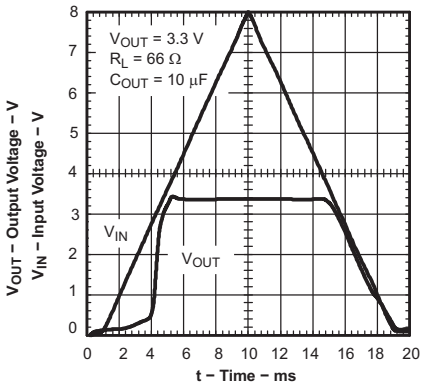


Figure 17. Power Up and Power Down

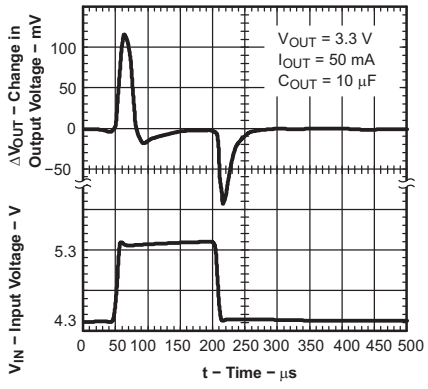


Figure 18. Line Transient Response

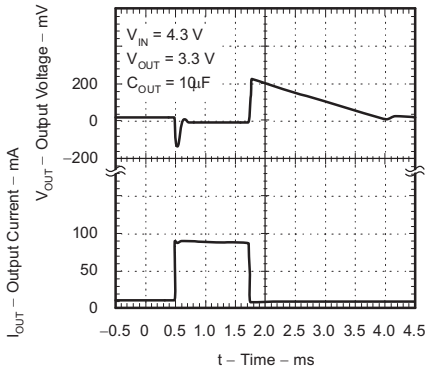
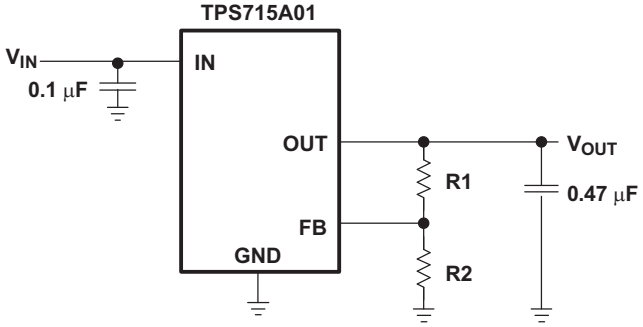


Figure 19. Load Transient Response

8.2.2 TPS715A01 Adjustable LDO Regulator Programming



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	392 kΩ	806 kΩ
2.8 V	1.07 MΩ	806 kΩ
5.0 V	2.55 MΩ	806 kΩ

Figure 20. TPS715A01 Adjustable LDO Regulator Programming

8.2.2.1 Detailed Design Procedure

8.2.2.1.1 Setting V_{OUT} for the TPS715A01 Adjustable LDO

The TPS715A family of devices contains an adjustable-version, the TPS715A01 device, which sets the output voltage using an external resistor divider as shown in Figure 20. The output voltage operating range is 1.2 V to 15 V, and is calculated using Equation 2.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where

- V_{REF} = 1.205 V (typical)

Resistors R1 and R2 should be chosen to allow approximately 1.5-µA of current through the resistor divider. Lower value resistors can be used for improved noise performance, but will consume more power. Higher resistor values should be avoided as leakage current into or out of FB across R1/R2 creates an offset voltage that is proportional to V_{OUT} divided by V_{REF}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using Equation 3.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times 2 \quad (3)$$

Figure 20 shows this configuration.

8.3 Do's and Don'ts

Place at least one 0.47-µF capacitor as close as possible to the OUT and GND terminals of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor of 0.047 µF as close as possible to the IN and GND terminals of the regulator for best performance.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

The TPS715A is designed to operate with an input voltage supply range from 2.5 V to 24 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit-board and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. TI strongly discourages using vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because that will negatively affect system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. TI also recommends embedding a ground reference plane either in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane assures accuracy of the output voltage and shields the LDO from noise.

10.2 Layout Example

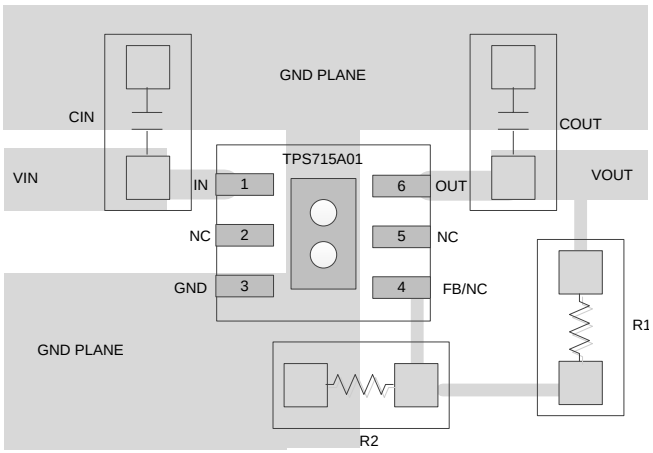


Figure 21. Example Layout for TPS715A01DRV

10.3 Power Dissipation

To ensure reliable operation, worst-case junction temperature should not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 4.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (4)$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator power dissipation is calculated using Equation 5.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

For a higher power package version of the TPS715A, see the TPS715A.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS715A. The TPS715AXXEVM-065 evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS715A is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS715A**xxyyyz**	**XX** is nominal output voltage (for example 33 = 3.3V, 01 = Adjustable) **YYY** is Package Designator **Z** is Package Quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS71533EVM LDO Evaluation Module User Guide*, SLVU061

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS715A	Click here	Click here	Click here	Click here	Click here
TPS715A30	Click here	Click here	Click here	Click here	Click here
TPS715A33	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS715A01DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANO	Samples
TPS715A01DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANO	Samples
TPS715A01DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANO	Samples
TPS715A01DRBT-NM	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	ANONM	Samples
TPS715A01DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANO	Samples
TPS715A01DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBE	Samples
TPS715A01DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBE	Samples
TPS715A30DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAV	Samples
TPS715A30DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SAV	Samples
TPS715A33DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANN	Samples
TPS715A33DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANN	Samples
TPS715A33DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANN	Samples
TPS715A33DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANN	Samples
TPS715A33DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ANN	Samples
TPS715A33DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ANN	Samples
TPS715A33DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ANN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

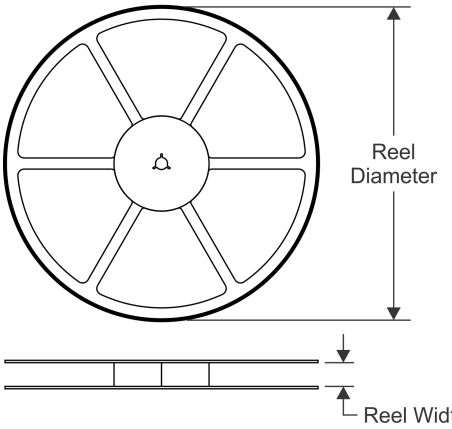
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

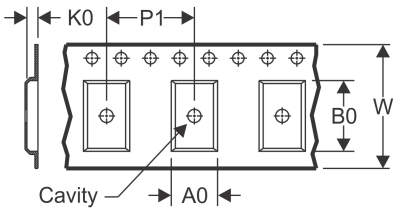
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

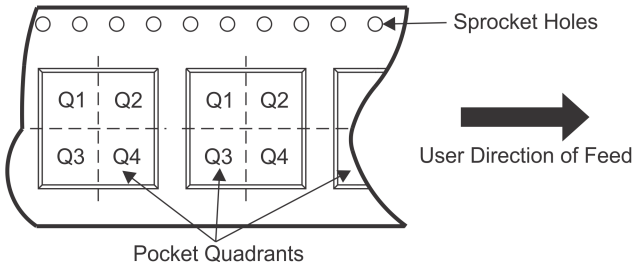


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

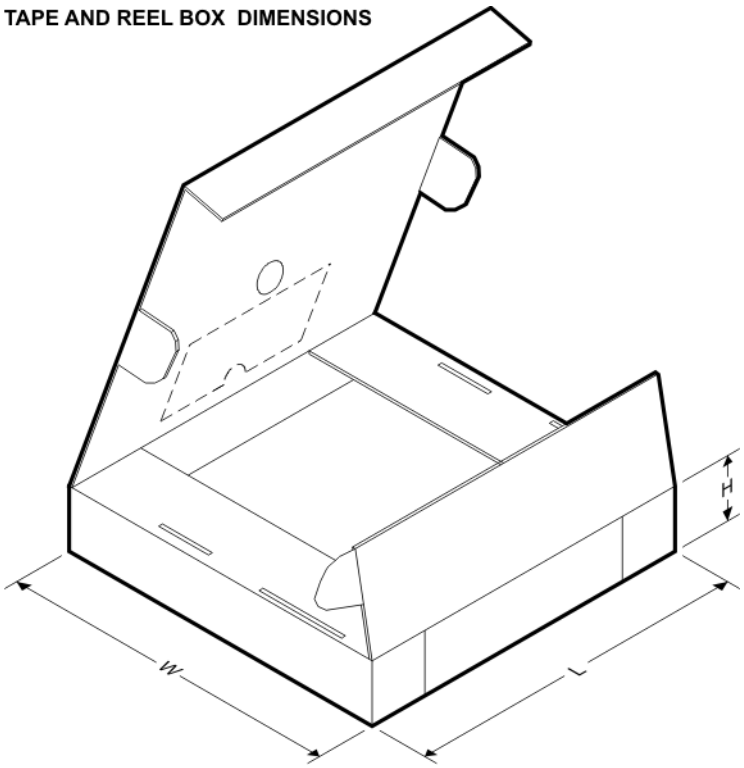
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS715A01DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A01DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A01DRBT-NM	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A01DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A01DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A30DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A30DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A33DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A33DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A33DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A33DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

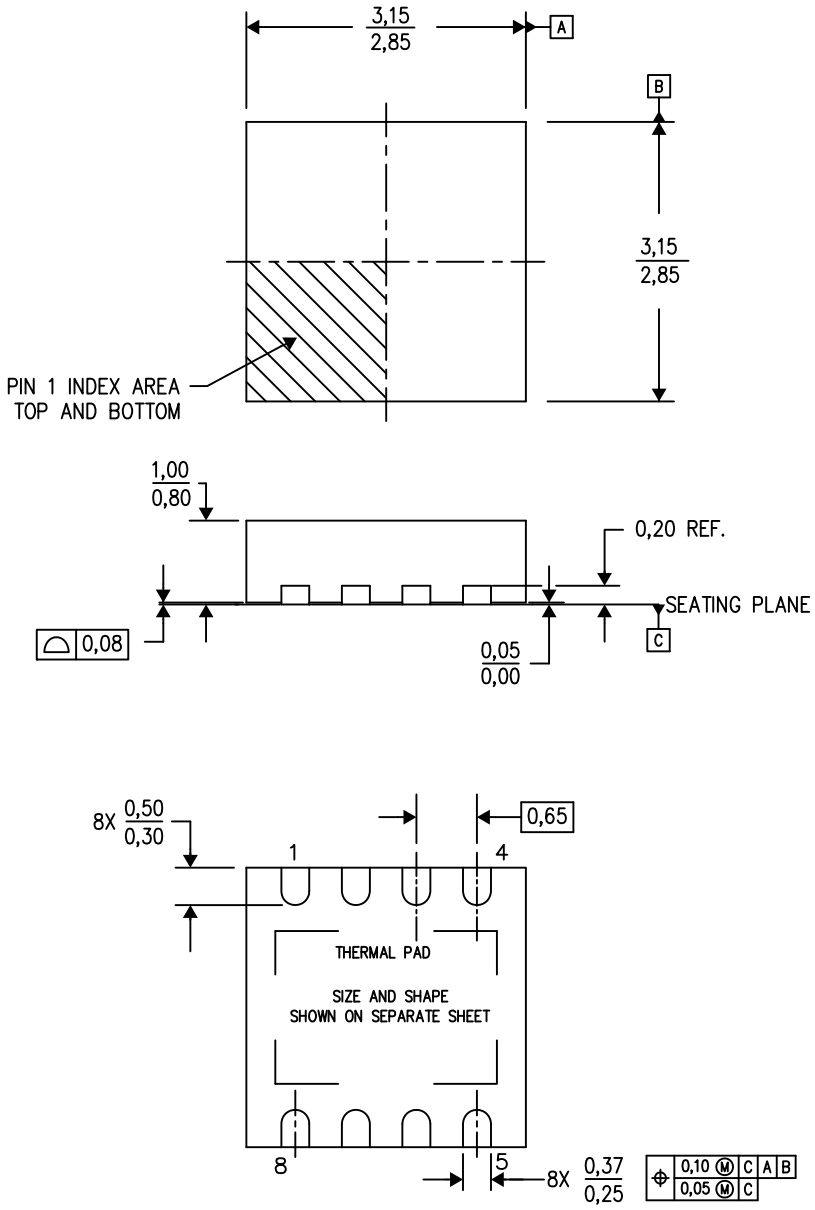
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS715A01DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS715A01DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS715A01DRBT-NM	SON	DRB	8	250	210.0	185.0	35.0
TPS715A01DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS715A01DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS715A30DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS715A30DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS715A33DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS715A33DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS715A33DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS715A33DRVT	SON	DRV	6	250	195.0	200.0	45.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

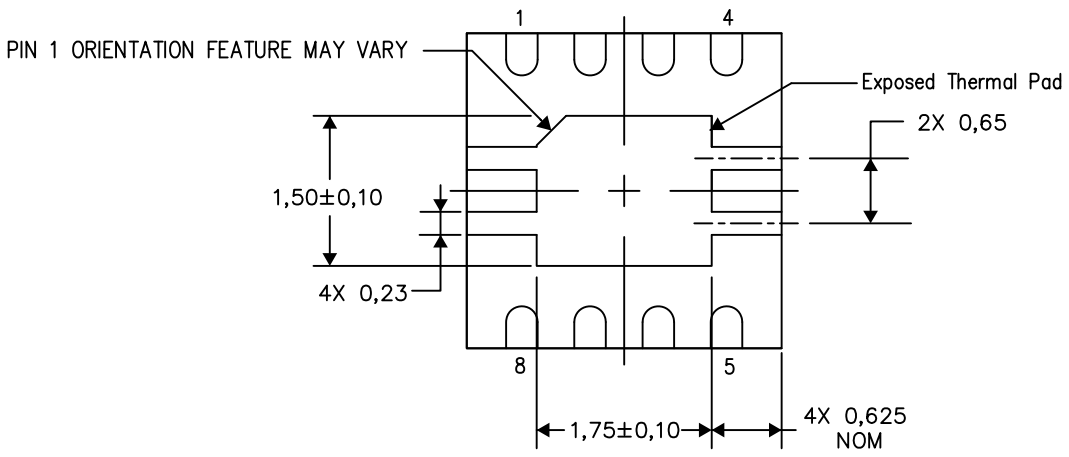
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



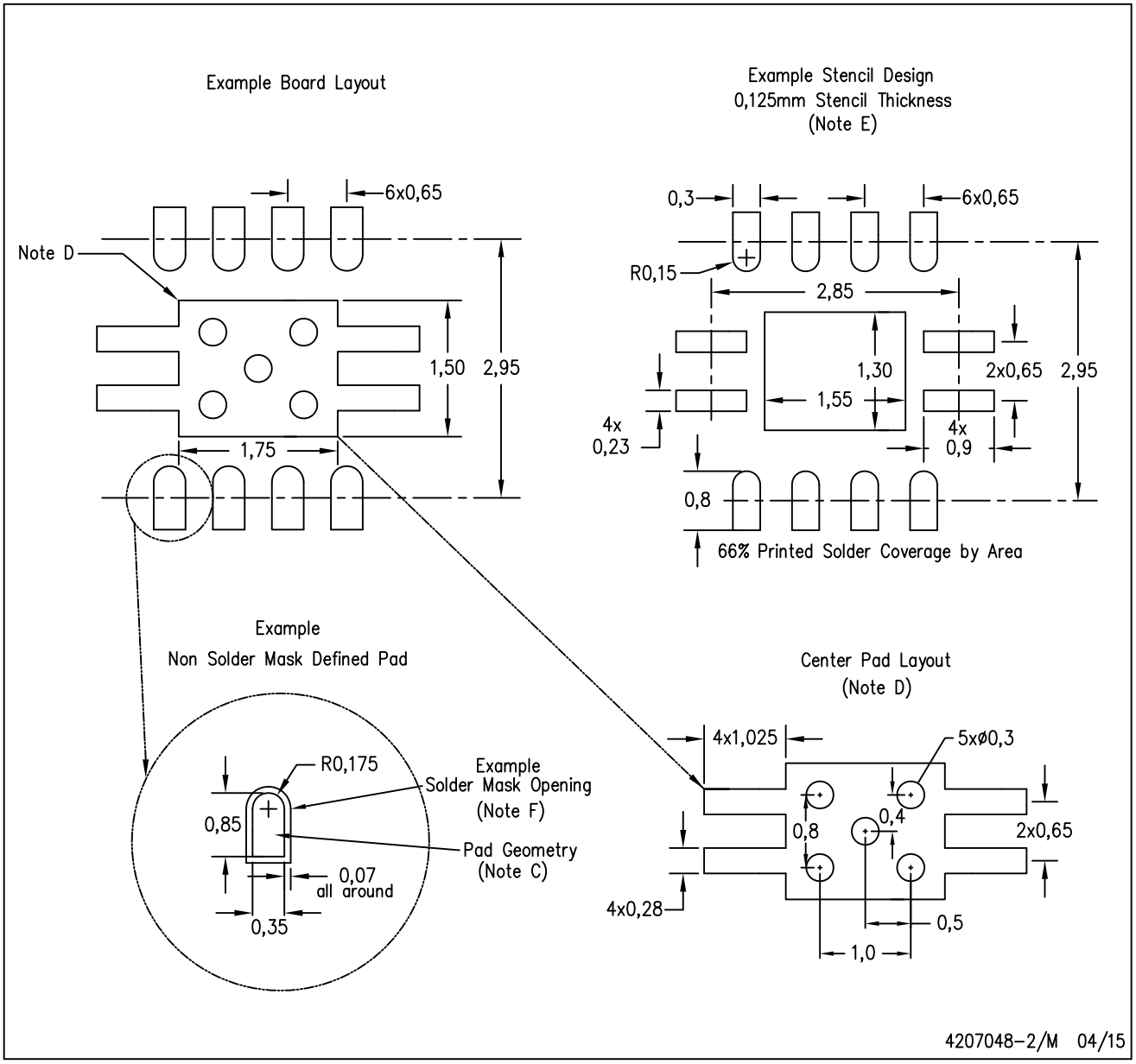
Bottom View

Exposed Thermal Pad Dimensions

4206340–2/Q 04/15

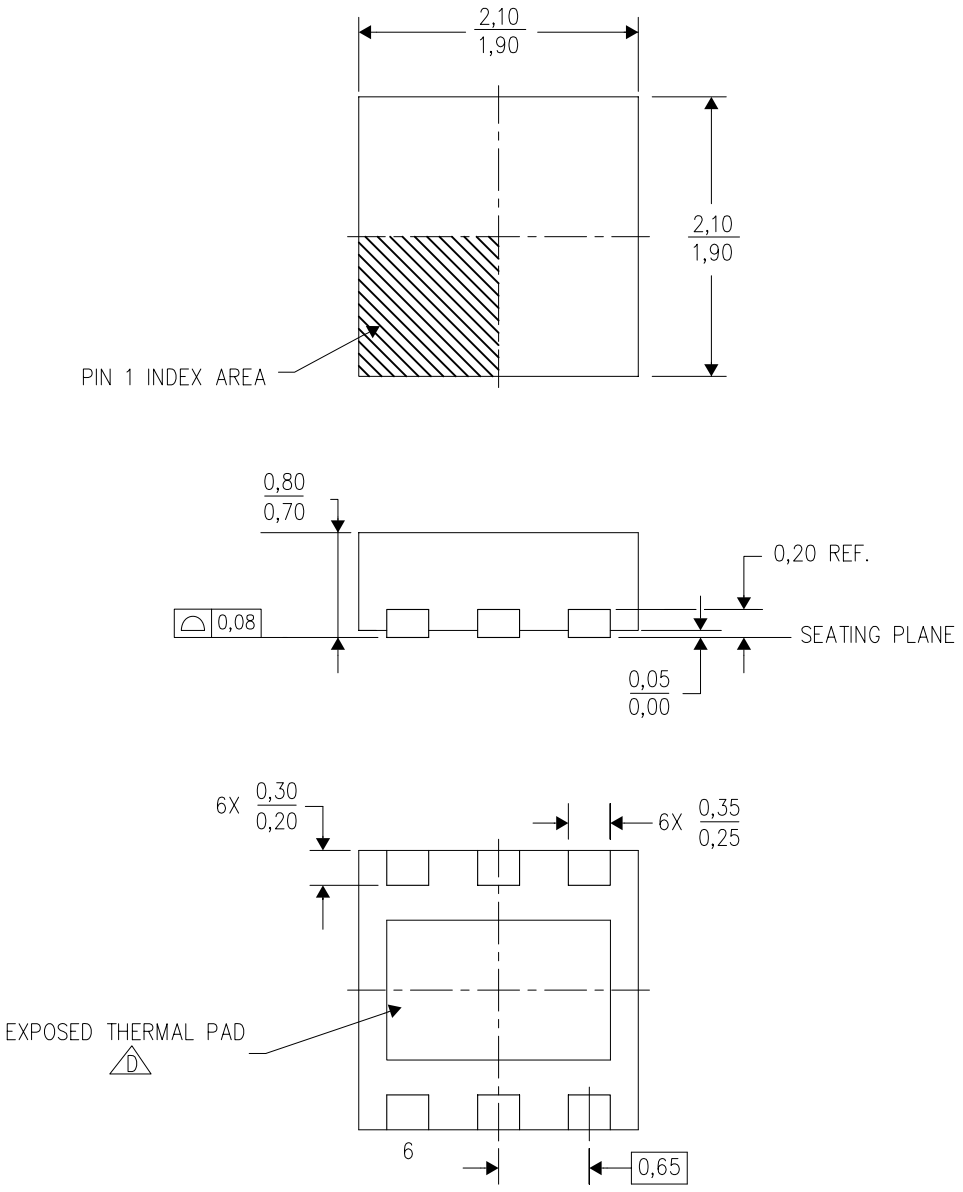
NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

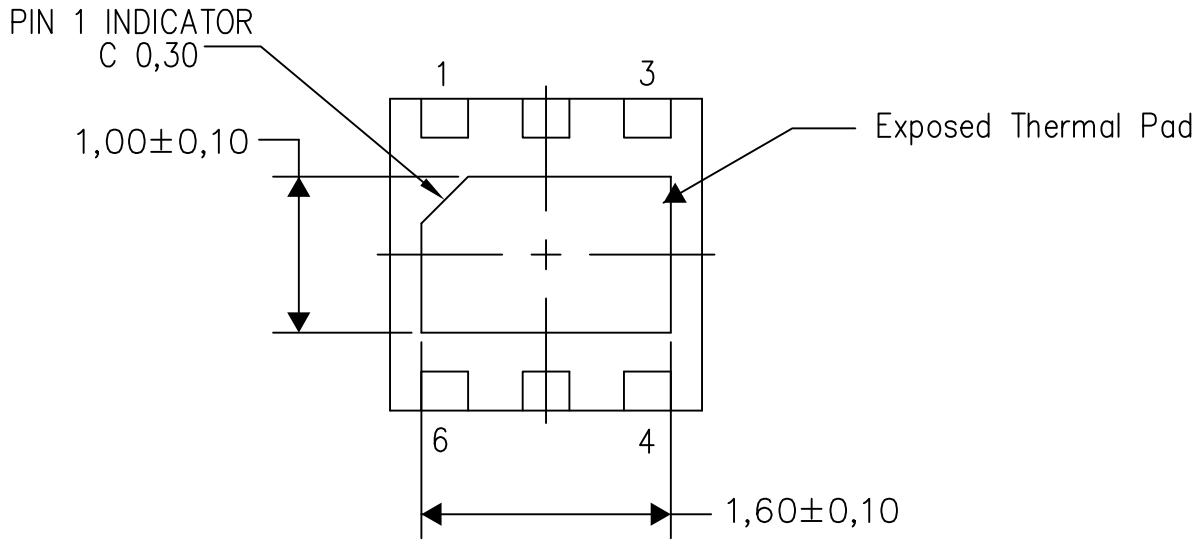
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



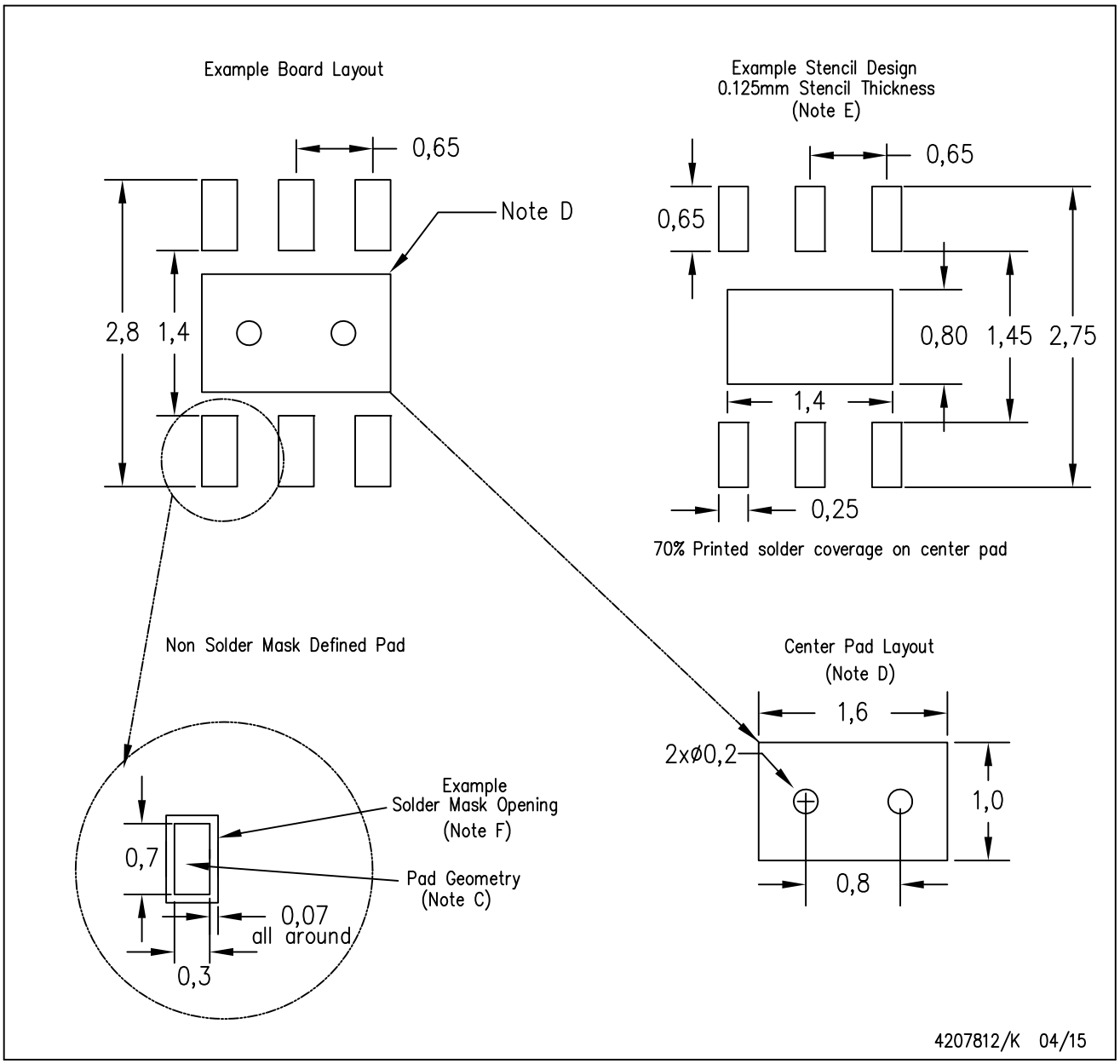
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
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Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

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