TPS720 350 mA, Ultra-Low V_{IN}, RF Low-Dropout Linear Regulator With Bias Pin

1 Features

- 350-mA High-Performance LDO
- Low Quiescent Current: 38 µA
- Excellent Load Transient Response: ±15 mV for I_{LOAD} = 0 mA to 350 mA in 1 µs
- Excellent Line Transient Response: ΔV_{OUT} = ±2 mV for ΔV_{BIAS} = ±600 mV in 1 µs; ΔV_{OUT} = ±200 µV for ΔV_{IN} = ±400 mV in 1 µs
- Low Noise: 48 μV_{RMS} (10 Hz to 100 kHz)
- 80 dB V_{IN} PSRR (10 Hz to 10 kHz)
- 70 dB V_{BIAS} PSRR (10 Hz to 10 kHz)
- Fast Start-Up Time: 140 µs
- Built-In Soft-Start With Monotonic V_{OUT} Rise and Start-Up Current Limited to 100 mA + I_{LOAD}
- Overcurrent and Thermal Protection
- Low Dropout: 110 mV at I_{LOAD} = 350 mA
- Stable with 2.2-µF Output Capacitor
- Available in 1.33 mm × 0.96 mm DSBGA-5 and 2 mm × 2 mm SON-6 Packages

2 Applications

- Digital Cameras
- Cellular Camera Phones
- Wireless LAN
- Handheld Products

3 Description

The TPS720 family of dual rail, low-dropout linear regulators (LDOs) offers outstanding ac performance (PSRR, load and line transient response), while consuming a very low quiescent current of 38 µA.

The V_{BIAS} rail that powers the control circuit of the LDO draws very low current (on the order of the quiescent current of the LDO) and can be connected to any power supply that is equal to or greater than 1.4 V above the output voltage. The main power path is through V_{IN}, which can be a lower voltage than V_{BIAS}; it can be as low as V_{OUT} + V_{DO}, increasing the efficiency of the solution in many power-sensitive applications. For example, V_{IN} can be an output of a high-efficiency, DC-DC step-down regulator.

The TPS720 supports a novel feature in which the output of the LDO regulates under light loads when the IN pin is left floating. The light-load drive current is sourced from V_{BIAS} under this condition. This feature is particularly useful in power-saving applications where the DC-DC converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load.

The TPS720 is stable with ceramic capacitors and uses an advanced BICMOS fabrication process that yields a dropout of 110 mV at a 350-mA output load. The TPS720 has the unique feature of providing a monotonic V_{OUT} rise (overshoot limited to 3%) with V_{IN} inrush current limited to 100 mA + I_{LOAD} with an output capacitor of 2.2 µF.

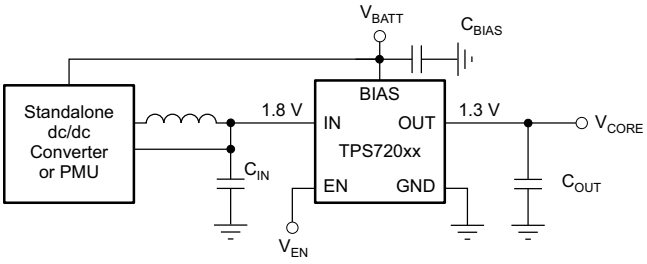
The TPS720 uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over load, line, process, and temperature extremes. An ultra-small DSBGA package makes the TPS720 ideal for handheld applications. The TPS720 is also available in a SON-8 package. This family of devices is fully specified over the temperature range of T_J = –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS720	DSBGA (5)	1.36 mm × 0.96 mm
	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2009) to Revision E **Page**

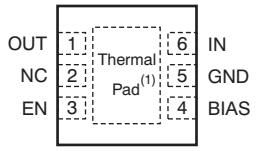
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (September, 2008) to Revision D **Page**

- Added electrical specifications for DRV package ... 5
- Noted electrical specifications for YZU package ... 5

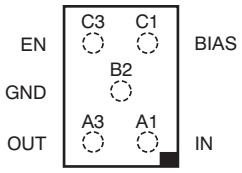
5 Pin Configuration and Functions

DRV Package
6-Pin SON With Exposed Thermal Pad
Top View



(1) TI recommends connecting the SON (DRV) package thermal pad to ground.

YZU Package
5-Pin DSBGA
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRV	YZU		
OUT	1	A3	O	Output pin. A 2.2-µF ceramic capacitor is connected from this pin to ground, for stability and to provide load transients. See *Input and Output Capacitor Requirements*.
NC	2	—	—	No connection.
EN	3	C3	I	Enable pin. A logic high signal on this pin turns the device on and regulates the voltage from IN to OUT. A logic low on this pin turns off the device.
BIAS	4	C1	I	Bias supply pin. TI recommends bypassing this input with a ceramic capacitor to ground for better transient performance. See *Input and Output Capacitor Requirements*.
GND	5	B2	—	Ground pin.
IN	6	A1	I	Input pin. This pin can be a maximum of 4.5 V; V_{IN} must not exceed V_{BIAS}. Bypass this input with a ceramic capacitor to ground. See *Input and Output Capacitor Requirements*.

6 Specifications

6.1 Absolute Maximum Ratings

At T_J = –40°C to 125°C (unless otherwise noted). All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
V_{IN}(2)	Input voltage (steady-state)	–0.3	V_{BIAS} or 5(3)	V
V_{IN_PEAK}(4)	Peak transient input		5.5	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	5	V
I_{OUT}	Peak output current	Internally limited		
	Output short circuit duration	Indefinite		
P_{DISS}	Total continuous power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–55	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To ensure proper operation of the device it is necessary that $V_{IN} \le V_{BIAS}$ under all conditions.
(3) Whichever is less.
(4) For durations no longer than 1ms each, for a total of no more than 1000 occurrences over the lifetime of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage (steady-state)	1.1		V_{BIAS} or 4.5 (1)	V
V_{BIAS}	Bias voltage	2.5 or or VOUT + 1.4 (2)		5.5	V
V_{OUT}	Output voltage	0.9		3.6	V
I_{OUT}	Peak output current	0		350	mA
C_{IN}	Input capacitance		1		µF
C_{BIAS}	Bias capacitance		0.1		µF
C_{OUT} (3)	Output capacitance	2.2			µF

(1) Whichever is less
(2) Whichever is greater
(3) Maximum ESR should be less than 250 mΩ.

6.4 Thermal Information

THERMAL METRIC (1)		TPS720		UNIT
		DRV (SON)	YZU (WSCP)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.5	144.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.2	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	27.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.6	27.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater); $V_{IN} \geq V_{OUT}$ + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage				1.1(1)		V_{BIAS} or 4.5(2)	V
V_{BIAS}	Bias voltage				2.5		5.5	V
V_{OUT}(3)	Output voltage(4)				0.9		3.6	V
	Output accuracy	Nominal	T_J = 25°C		–3		3	mV
		Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –40°C to 125°C	V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, 0 mA ≤ I_{OUT} ≤ 350 mA		–2%		2%	
		Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –40°C to 125°C	**DRV package only:** V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, 0 mA ≤ I_{OUT} ≤ 350 mA, V_{OUT} < 1.2 V		–25		25	mV
		Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –10°C to 85°C	**YZU package only:** V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, 0 mA ≤ I_{OUT} ≤ 350 mA 1.6 V ≤ V_{OUT} ≤ 3.3 V		–1%		1%	
		V_{IN} floating	V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 0 µA ≤ I_{OUT} ≤ 500 µA			±1%		
$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} line regulation		V_{IN} = (V_{OUT} + 0.5 V) to 4.5 V, I_{OUT} = 1 mA			16		µV/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	V_{BIAS} line regulation		V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater) to 5.5 V, I_{OUT} = 1 mA			16		µV/V
	V_{IN} line transient		ΔV_{IN} = 400 mV, t_{RISE} = t_{FALL} = 1 µs			±200		µV
	V_{BIAS} line transient		ΔV_{BIAS} = 600 mV, t_{RISE} = t_{FALL} = 1 µs			±0.8		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0 mA ≤ I_{OUT} ≤ 350 mA (no load to full load)			–15		µV/mA
	Load transient		0 mA ≤ I_{OUT} ≤ 350 mA, t_{RISE} = t_{FALL} = 1 µs			±15		mV
V_{DO_IN}	V_{IN} dropout voltage(5)		V_{IN} = $V_{OUT(NOM)}$ – 0.1 V, (V_{BIAS} – $V_{OUT(NOM)}$) = 1.4 V, I_{OUT} = 350 mA			110	200	mV
V_{DO_BIAS}	V_{BIAS} dropout voltage(6)		V_{IN} = $V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 350 mA			1.09	1.4	V
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(NOM)}$		420	525	800	mA
I_{GND}	Ground pin current		I_{OUT} = 100 µA			38		µA
			I_{OUT} = 0 mA to 350 mA			54	80	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4 V, T_J = –40°C to 85°C			0.5	2	µA
PSRR	V_{IN} power-supply rejection ratio		V_{IN} – V_{OUT} ≥ 0.5 V, V_{BIAS} = V_{OUT} + 1.4 V, I_{OUT} = 350 mA	f = 10 Hz		85		dB
				f = 100 Hz		85		
				f = 1 kHz		85		
				f = 10 kHz		80		
				f = 100 kHz		70		
				f = 1 MHz		50		

(1) Performance specifications are ensured up to a minimum V_{IN} = V_{OUT} + 0.5 V.
(2) Whichever is less.
(3) Minimum V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater) and V_{IN}= V_{OUT} + 0.5 V.
(4) V_O nominal value is factory programmable through the onchip EEPROM.
(5) Measured for devices with $V_{OUT(NOM)} \geq$ 1.2 V.
(6) V_{BIAS} – V_{OUT} with V_{OUT} = $V_{OUT(NOM)}$ – 0.1 V. Measured for devices with $V_{OUT(NOM)} \geq$ 1.8 V.

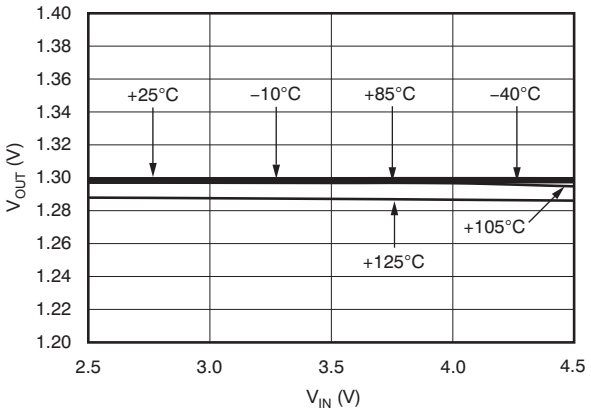
Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater); V_{IN} ≥ V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	V_{BIAS} power-supply rejection ratio	V_{IN} – V_{OUT} ≥ 0.5 V, V_{BIAS} = V_{OUT} + 1.4 V, I_{OUT} = 350 mA	f = 10 Hz		80		dB
			f = 100 Hz		80		
			f = 1 kHz		75		
			f = 10 kHz		65		
			f = 100 kHz		55		
			f = 1 MHz		35		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{BIAS} ≥ 2.5 V, V_{IN} = V_{OUT} + 0.5 V			48		μV_{RMS}
I_{VIN_INRUSH}	Inrush current on V_{IN}	V_{BIAS} = (V_{OUT} +1.4 V) or 2.5 V (whichever is greater), V_{IN} = V_{OUT} + 0.5 V			100 + I_{LOAD}		mA
t_{STR}	Start-up time	V_{OUT} = 95% $V_{OUT(NOM)}$, I_{OUT} = 350 mA, C_{OUT} = 2.2 µF			140		µs
$V_{EN(HI)}$	Enable pin high (enabled)			1.1			V
$V_{EN(LO)}$	Enable pin low (disabled)			0		0.4	V
I_{EN}	Enable pin current	V_{EN} = 5.5 V , V_{IN} = 4.5 V, V_{BIAS} = 5.5 V				1	µA
UVLO	Undervoltage lockout	V_{BIAS} rising		2.41	2.45	2.49	V
	Hysteresis	V_{BIAS} falling			150		mV
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		
T_J	Operating junction temperature			–40		125	°C

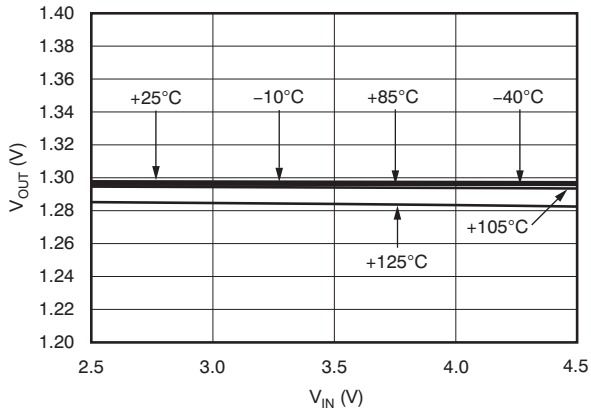
6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater); V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.



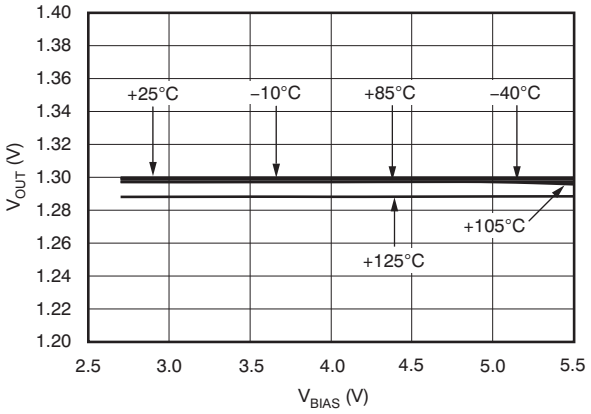
I_{OUT} = 0 mA

Figure 1. V_{IN} Line Regulation (TPS72013YZU)



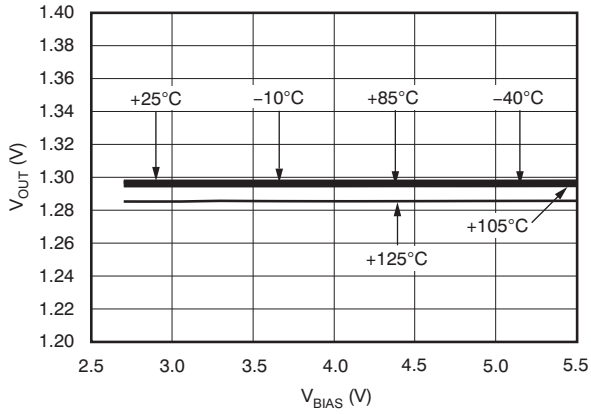
I_{OUT} = 350 mA

Figure 2. V_{IN} Line Regulation (TPS72013YZU)



I_{OUT} = 0 mA

Figure 3. V_{BIAS} Line Regulation (TPS72013YZU)



I_{OUT} = 350 mA

Figure 4. V_{BIAS} Line Regulation (TPS72013YZU)

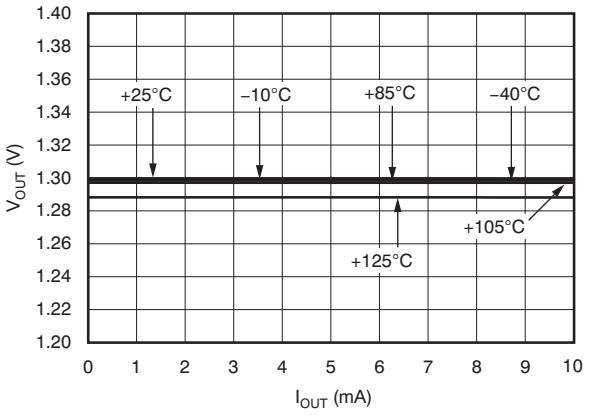


Figure 5. Load Regulation Under Light Loads (TPS72013YZU)

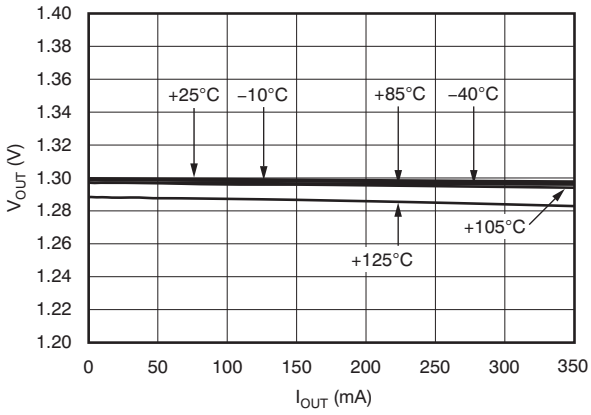


Figure 6. Load Regulation (TPS72013YZU)

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater); V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.

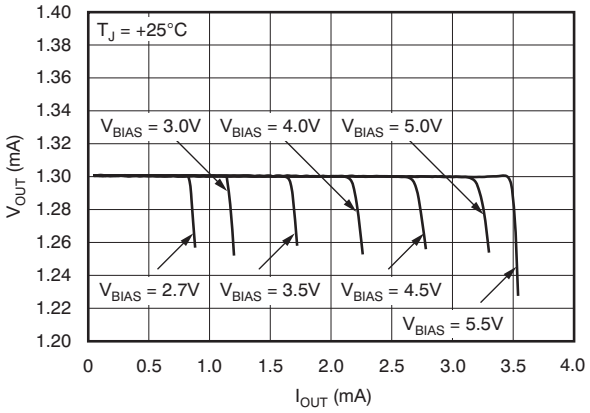


Figure 7. Load Regulation With V_{IN} Floating (TPS72013YZU)

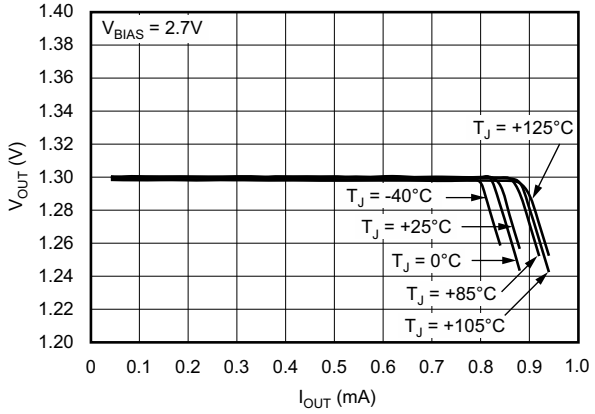


Figure 8. Load Regulation With V_{IN} Floating (TPS72013YZU)

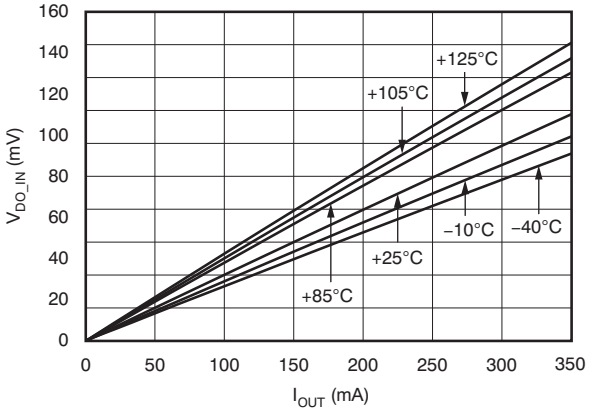


Figure 9. VIN Dropout Voltage vs Output Current (TPS72013YZU)

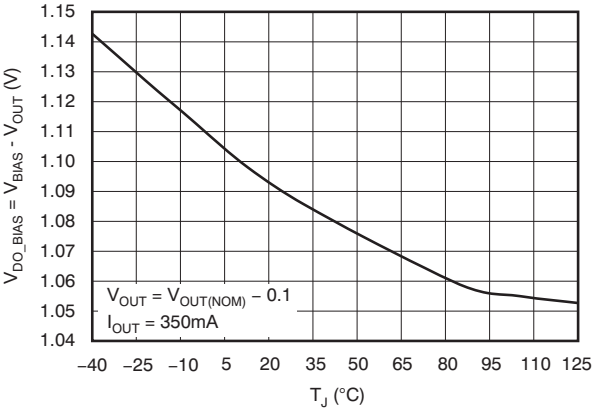


Figure 10. VBIAS Dropout Voltage vs Temperature (TPS72033YZU)

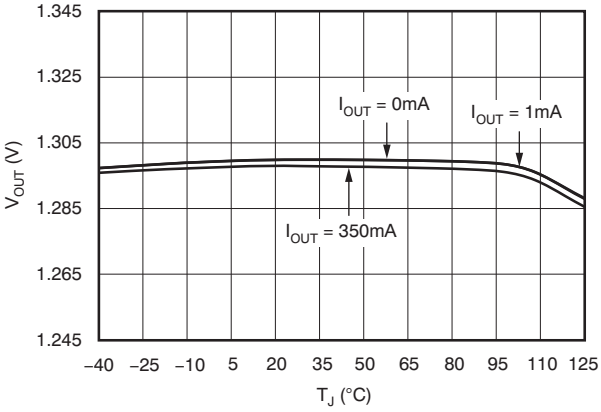


Figure 11. Output Voltage vs Temperature (TPS72013YZU)

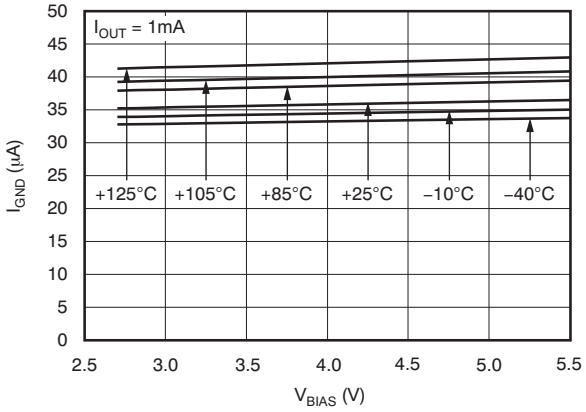


Figure 12. Ground Pin Current vs VBIAS Input Voltage (TPS72013YZU)

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater); V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.

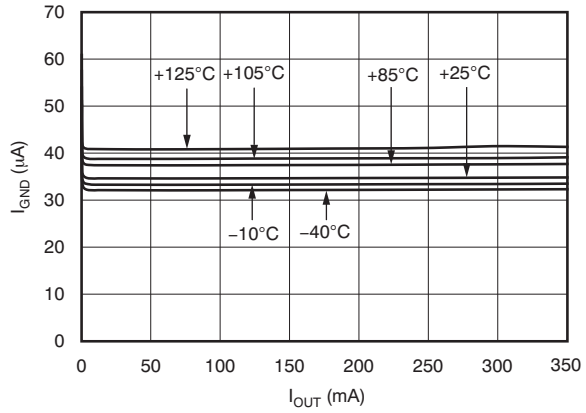


Figure 13. Ground Pin Current vs Output Current (TPS72013YZU)

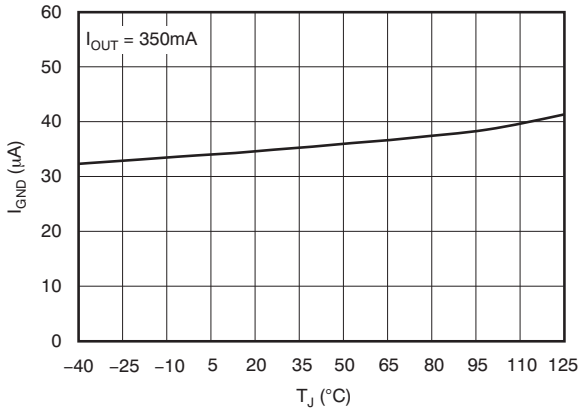


Figure 14. Ground Pin Current vs Temperature (TPS72013YZU)

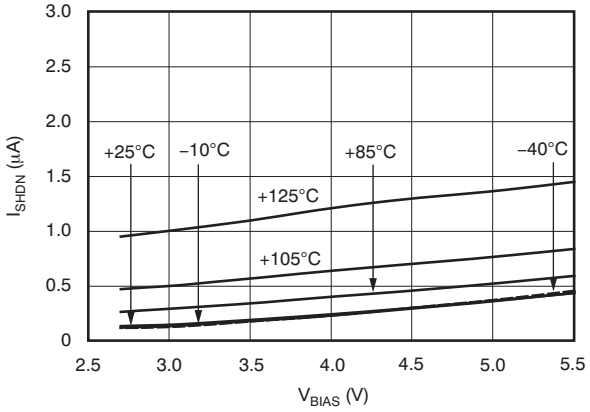


Figure 15. Shutdown Current vs VBIAS Input Voltage (TPS72013YZU)

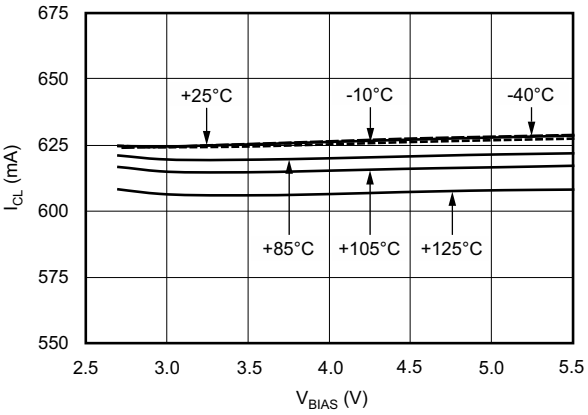


Figure 16. Current Limit vs VBIAS Input Voltage (TPS72013YZU)

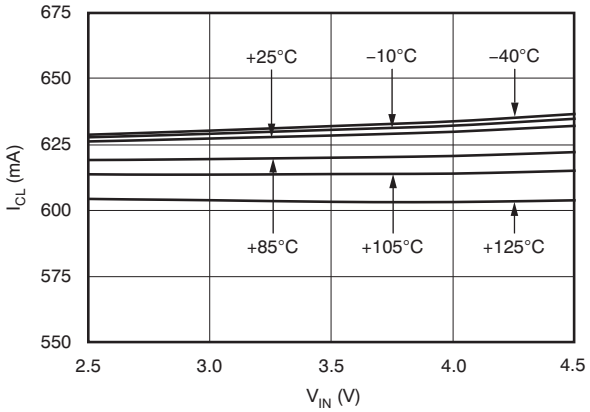


Figure 17. Current Limit vs VIN Input Voltage (TPS72013YZU)

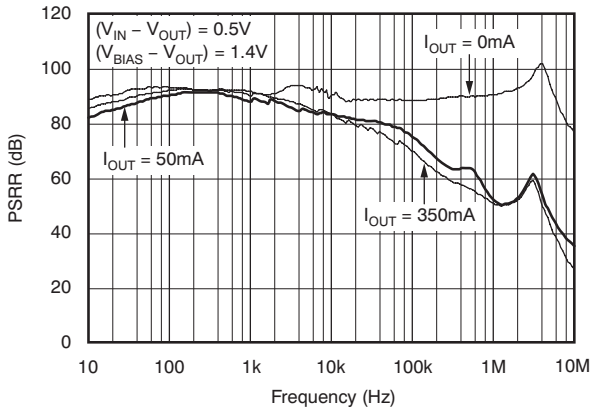


Figure 18. VIN Power-Supply Ripple Rejection vs Frequency (TPS72015YZU)

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater); V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.

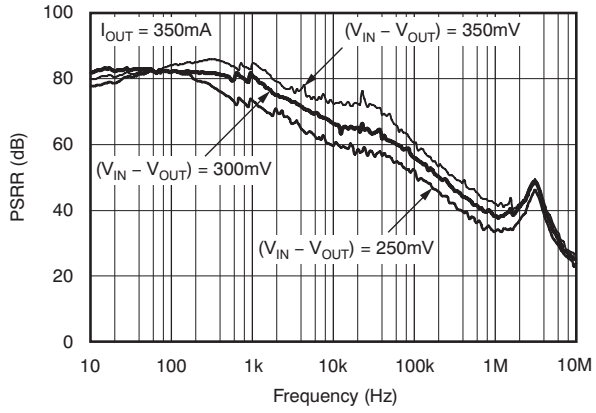


Figure 19. VIN Power-Supply Ripple Rejection vs Frequency (TPS72015YZU)

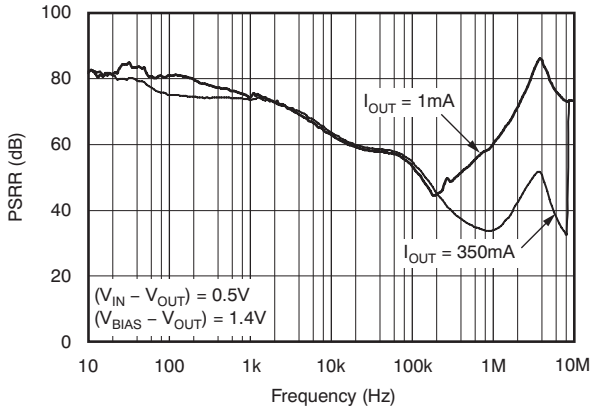


Figure 20. VBIAS Power-Supply Ripple Rejection vs Frequency (TPS72015YZU)

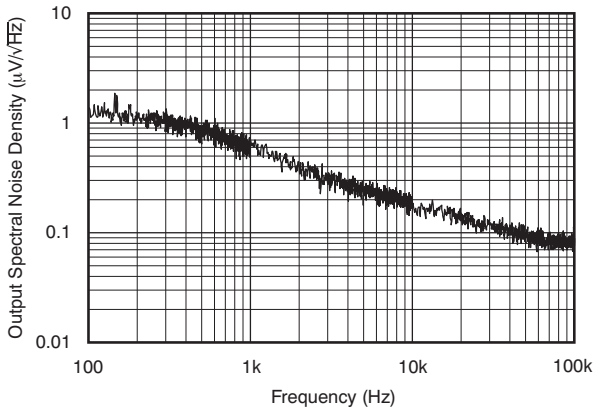
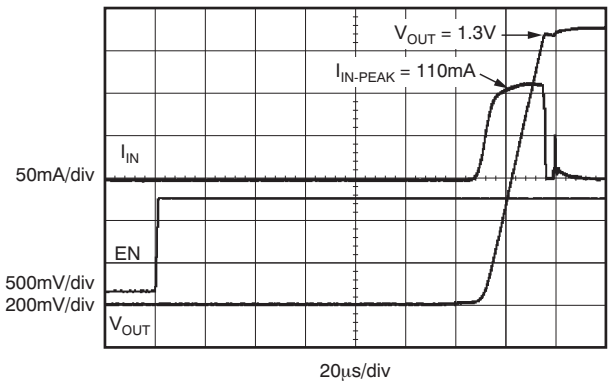
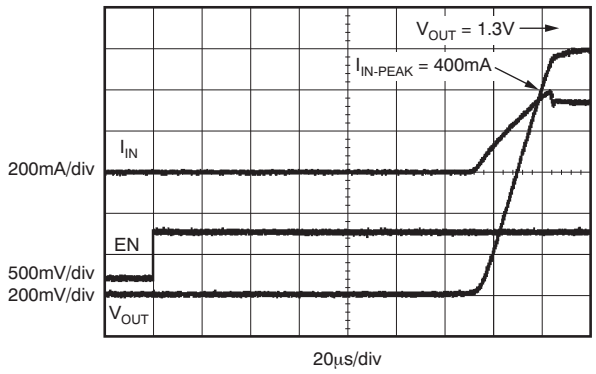


Figure 21. Output Spectral Noise Density vs Frequency (TPS72015YZU)



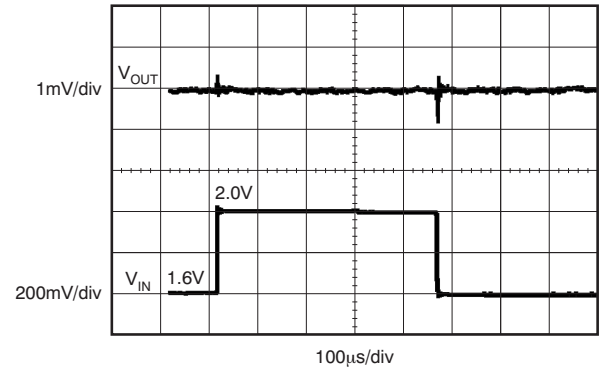
V_{IN} = 1.8 V V_{OUT} = 1.3 V V_{BIAS} = 2.7 V
I_{OUT} = 0 mA

Figure 22. V_{IN} Inrush Current



V_{IN} = 1.8 V V_{OUT} = 1.3 V V_{BIAS} = 2.7 V
I_{OUT} = 350 mA

Figure 23. V_{IN} Inrush Current

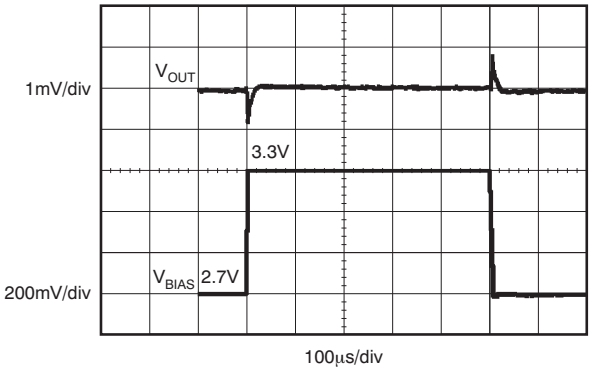


V_{IN} = 1.6 to 2 V V_{OUT} = 1.3 V V_{BIAS} = 2.7 V
V_{IN} Slew Rate = 1 V/µs I_{OUT} = 350 mA

Figure 24. V_{IN} Line Transient Response

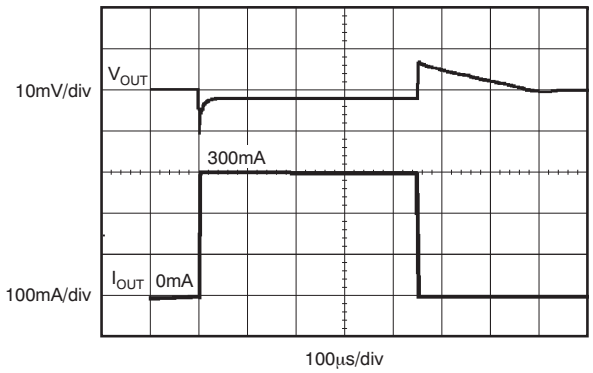
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater); V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.



V_{IN} = 1.8 V V_{OUT} = 1.3 V V_{BIAS} = 2.7 V to 3.3 V
V_{BIAS} Slew Rate = 600 m/µs I_{OUT} = 350 mA

Figure 25. V_{BIAS} Line Transient Response



V_{IN} = 1.8 V V_{OUT} = 1.3 V V_{BIAS} = 2.7 V
t_{RISE} = 1 µs

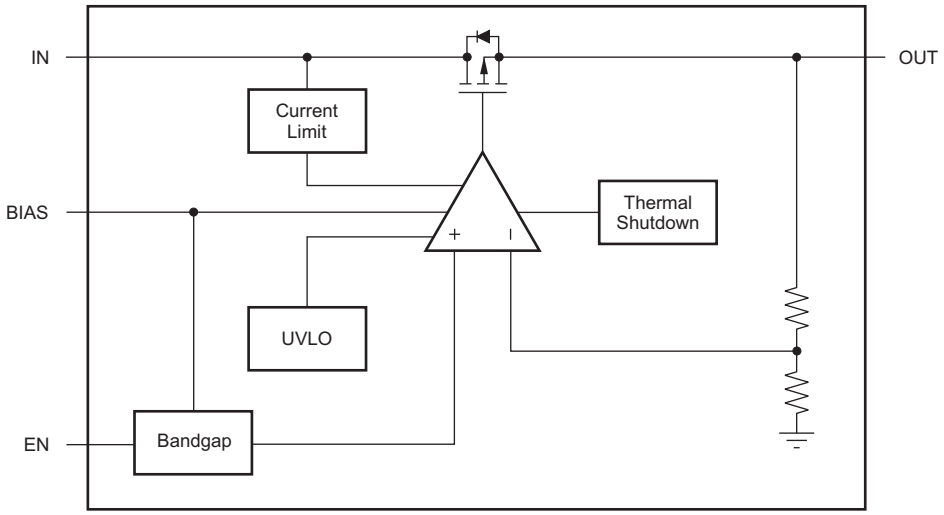
Figure 26. Load Transient Response

7 Detailed Description

7.1 Overview

The TPS720 belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1 MHz) at very low headroom (V_{IN} – V_{OUT}). The implementation of the BIAS pin on the TPS720 vastly improves efficiency of low V_{OUT} applications by allowing the use of a preregulated, low-voltage input supply. The TPS720 supports a novel feature in which the output of the LDO regulates under light loads (<500 µA) when the IN pin is left floating. The light-load drive current is sourced from V_{BIAS} under this condition. This feature is particularly useful in power-saving applications where the DC-DC converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load. These features, combined with low noise, low ground pin current, and ultra-small packaging, make this device ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS720 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The NMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shut down is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Considerations* section for more details.

The NMOS pass element in the TPS720 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

7.3.2 Inrush Current Limit

The TPS720 family of LDO regulators implement a novel inrush current limit circuit architecture: the current drawn through the IN pin is limited to a finite value. This $I_{INRUSHLIMIT}$ charges the output to its final voltage. All the current drawn through V_{IN} goes to charge the output capacitance when the load is disconnected. The following equation shows the inrush current limit performed by the circuit:

$$I_{INRUSHLIMIT}(A) = C_{OUT}(\mu F) \times 0.0454545\ (V/\mu s) + I_{LOAD}(A) \quad (1)$$

Feature Description (continued)

Assuming a C_{OUT} of 2.2 µF with the load disconnected (that is, I_{LOAD} = 0) the $I_{INRUSHLIMIT}$ is calculated to be 100 mA. The inrush current charges the LDO output capacitor. If the output of the LDO regulates to 1.3 V, then the LDO charges the output capacitor to the final output value in approximately 28.6 µs.

Another consideration is when a load is connected to the output of an LDO. The connected load tries to steer a portion of the current away from V_{OUT}. The TPS720 inrush current limit circuit employs a new technique that supplies not only the $I_{INRUSHLIMIT}$, but also the additional current needed by the load. If I_{LOAD} = 350 mA, then the $I_{INRUSHLIMIT}$ calculates to be approximately 450 mA (from Equation 1).

7.3.3 Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

7.3.4 Undervoltage Lockout (UVLO)

The TPS720 uses an undervoltage lock-out circuit on the BIAS pin to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50-µs duration.

7.4 Device Functional Modes

Driving the EN pin over 1.1 V turns on the regulator. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 500 nA, typically.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability on the IN pin, it is good analog design practice to connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the IN pin input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located close to the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The BIAS pin does not require an input capacitor because it does not source high currents. However, if source impedance is not sufficiently low, then TI recommends a small 0.1-µF bypass capacitor.

The TPS720 is designed to be stable with standard ceramic capacitors with values of 2.2 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 250 mΩ.

8.1.2 Output Regulation With IN Pin Floating

The TPS720 supports a novel feature in which the output of the LDO regulates under light loads when the IN pin is left floating. Under normal conditions, when the IN pin is connected to a power source, the BIAS pin draws only tens of milliamperes. However, when the IN pin is floating, an innovative circuit is used that allows a maximum current of 500 µA to be drawn by the load through the BIAS pin, while maintaining the output in regulation. This feature is particularly useful in power-saving applications where a DC-DC converter connected to the IN pin is disabled, but the LDO is required to regulate the output voltage to a light load.

Figure 27 shows an application example where a microcontroller is not turned off (to maintain the state of the internal memory), but where the regulated supply (shown as the TPS62xxx) is turned off to reduce power. In this case, the TPS720 BIAS pin provides sufficient load current to maintain a regulated voltage to the microcontroller.

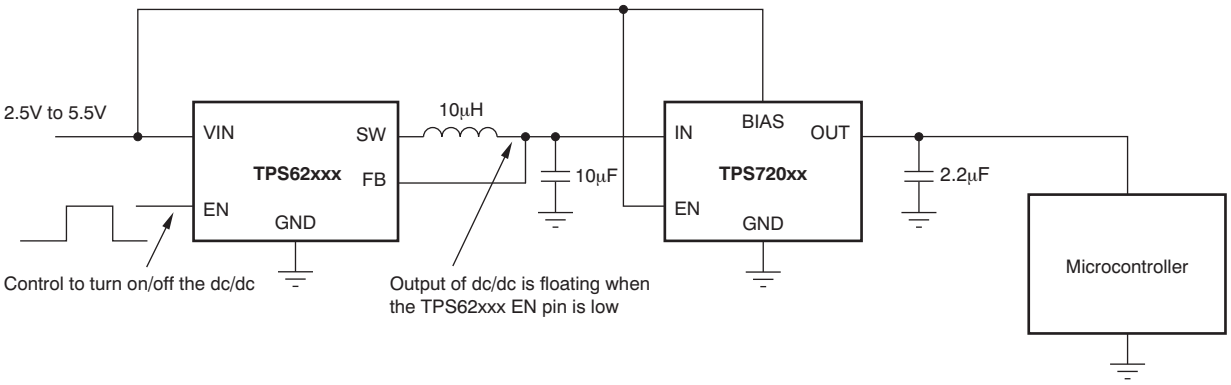


Figure 27. Example of Floating IN Pin Regulation

Application Information (continued)

8.1.3 Dropout Voltage

The TPS720 uses a NMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the NMOS pass element. V_{DO} approximately scales with output current because the NMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 19.

8.1.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response.

8.1.5 Minimum Load

The TPS720 is stable with no output load. Traditional LDOs suffer from low loop gain at very light output loads. The TPS720 employs an innovative, low-current mode circuit under very light or no-load conditions, resulting in improved output voltage regulation performance reduced to zero output current.

8.2 Typical Application

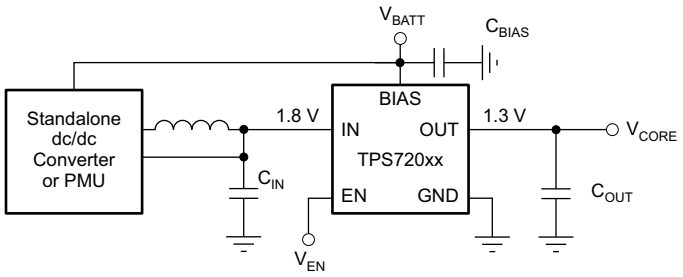


Figure 28. Typical Application Schematic

8.2.1 Design Requirements

Table 1 shows the parameters for this design example.

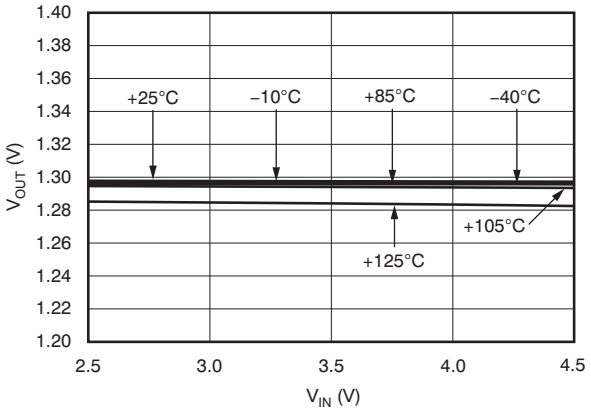
Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.8 V
V_{BIAS}	2.7 V
V_{OUT}	1.3 V
I_{OUT}	10-mA typical, 350-mA peak

8.2.2 Detailed Design Procedures

A small-size solution is desired, so select the minimum recommended component size. Set C_{IN} = 1 µF, C_{BIAS} = 100 nF, C_{OUT} = 2.2 µF.

8.2.3 Application Curves



I_{OUT} = 350 mA

Figure 29. V_{IN} Line Regulation (TPS72013YZU)

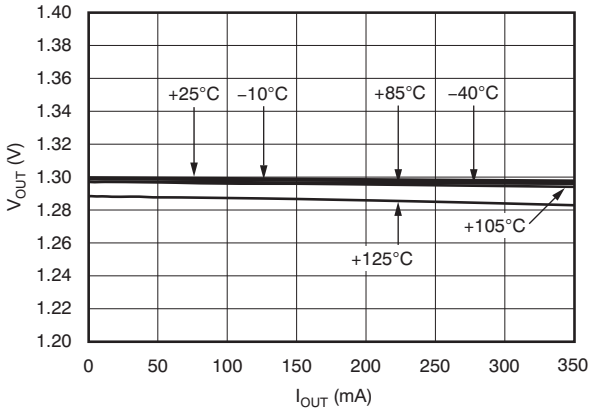
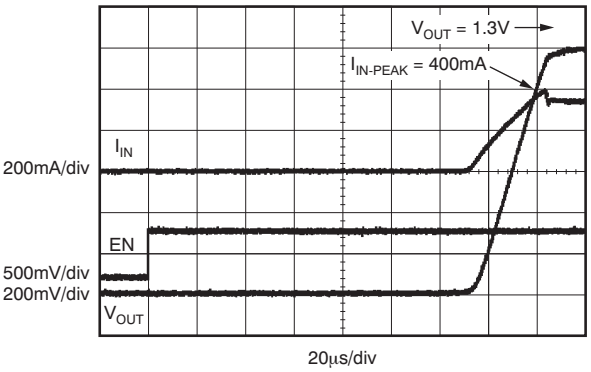
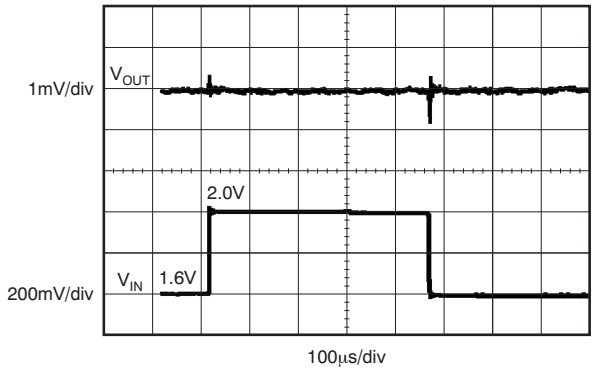


Figure 30. Load Regulation (TPS72013YZU)



V_{IN} = 1.8 V V_{OUT} = 1.3 V V_{BIAS} = 2.7 V
I_{OUT} = 350 mA

Figure 31. V_{IN} Inrush Current



V_{IN} = 1.6 to 2 V V_{OUT} = 1.3 V V_{BIAS} = 2.7 V
V_{IN} Slew Rate = 1 V/µs I_{OUT} = 350 mA

Figure 32. V_{IN} Line Transient Response

9 Power Supply Recommendations

The input supply and bias supply for the LDO must be within its recommended operating conditions and provide adequate headroom for the device to have a regulated output. The minimum capacitor requirements must be met, and if the input supply is noisy, then additional input capacitors with low ESR can help improve transient performance.

10 Layout

10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High equivalent series resistance (ESR) capacitors may degrade PSRR. The BIAS pin draws very little current and can be routed as a signal (make sure to shield it from high-frequency coupling).

10.2 Layout Example

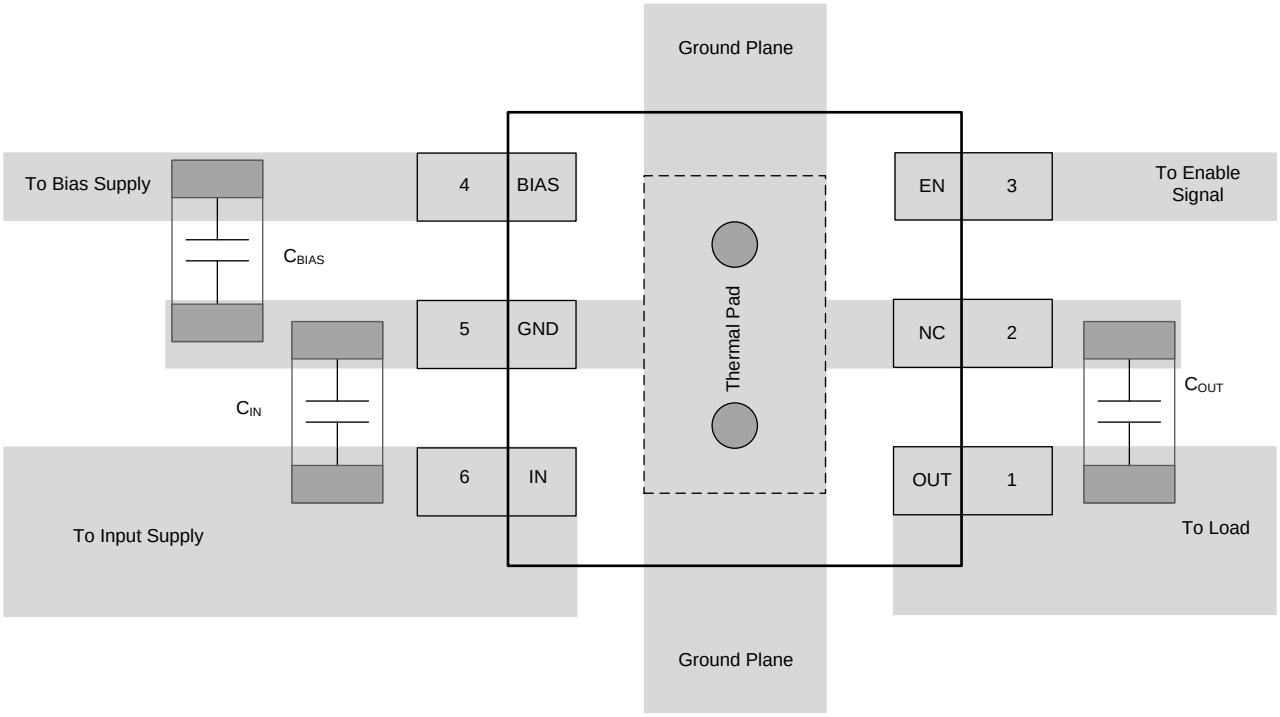


Figure 33. Recommended Layout

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Thermal Considerations (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS720 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS720 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS720. The TPS720xxDRVEVM evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Table 2. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TPS720**xx(x)**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.9 V to 3.6 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS720xxDRVEVM Evaluation Module*, SBVU024
- *Using New Thermal Metrics*, SBVA025

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Mounting

Solder pad footprint recommendations for the TPS720 are available from the Texas Instruments website at www.ti.com.

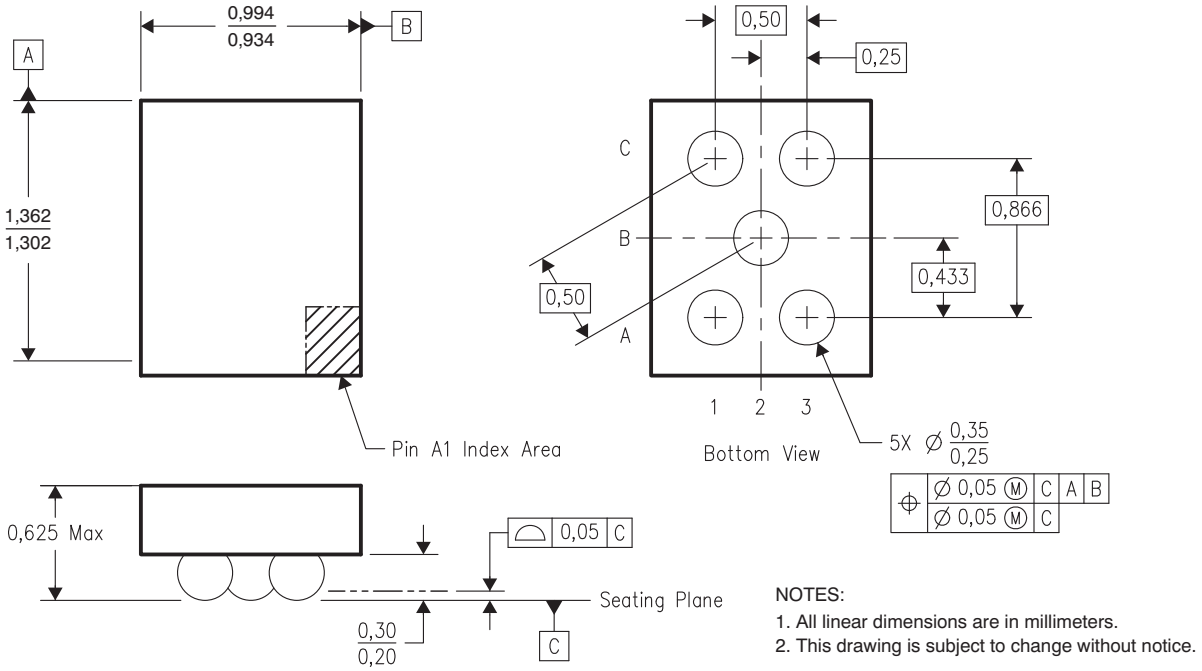


Figure 34. YZU Wafer Chip-Scale Package Dimensions (in mm)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72009YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G3	Samples
TPS72009YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G3	Samples
TPS720105DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ODC	Samples
TPS720105DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ODC	Samples
TPS720105YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	NM	Samples
TPS720105YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	NM	Samples
TPS72010DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAA	Samples
TPS72010DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAA	Samples
TPS720115DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHP	Samples
TPS720115DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHP	Samples
TPS72011DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAR	Samples
TPS72011DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAR	Samples
TPS72011YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ	Samples
TPS72011YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ	Samples
TPS72012DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAB	Samples
TPS72012DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAB	Samples
TPS72012YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	NN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72012YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	NN	Samples
TPS72013YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FS	Samples
TPS72013YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FS	Samples
TPS72015DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAC	Samples
TPS72015DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAC	Samples
TPS72015YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FT	Samples
TPS72015YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FT	Samples
TPS72017YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GC	Samples
TPS72017YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GC	Samples
TPS72018DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAD	Samples
TPS72018DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAD	Samples
TPS72018YZUR	ACTIVE	DSBGA	YZU	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GD	Samples
TPS72018YZUT	ACTIVE	DSBGA	YZU	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

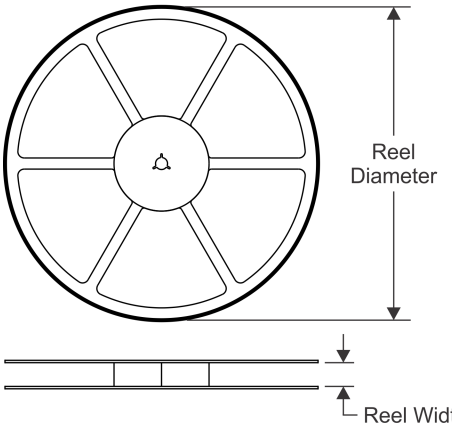
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

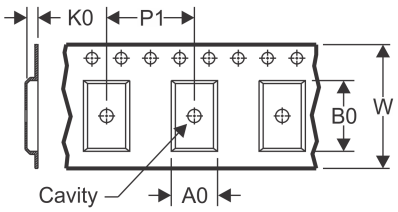
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

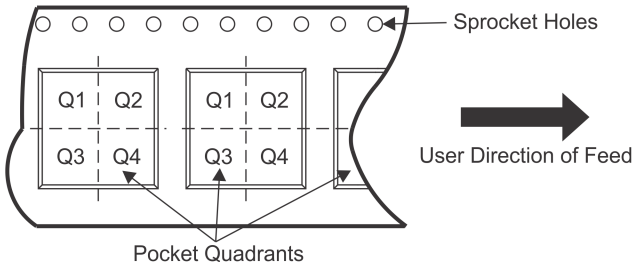


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

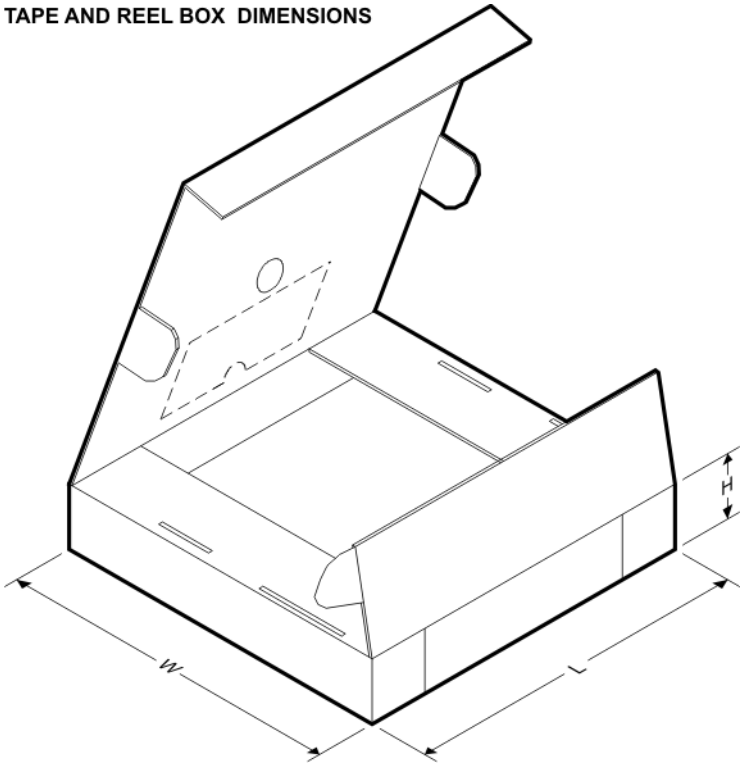


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72009YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72009YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS720105DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS720105DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS720105YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS720105YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72010DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72010DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS720115DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS720115DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72011DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72011DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72011YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72011YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72012DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72012DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72012YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72012YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72013YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72013YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72015DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72015DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72015DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72015DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS72015YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72015YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72017YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72017YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72018DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72018DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS72018YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS72018YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

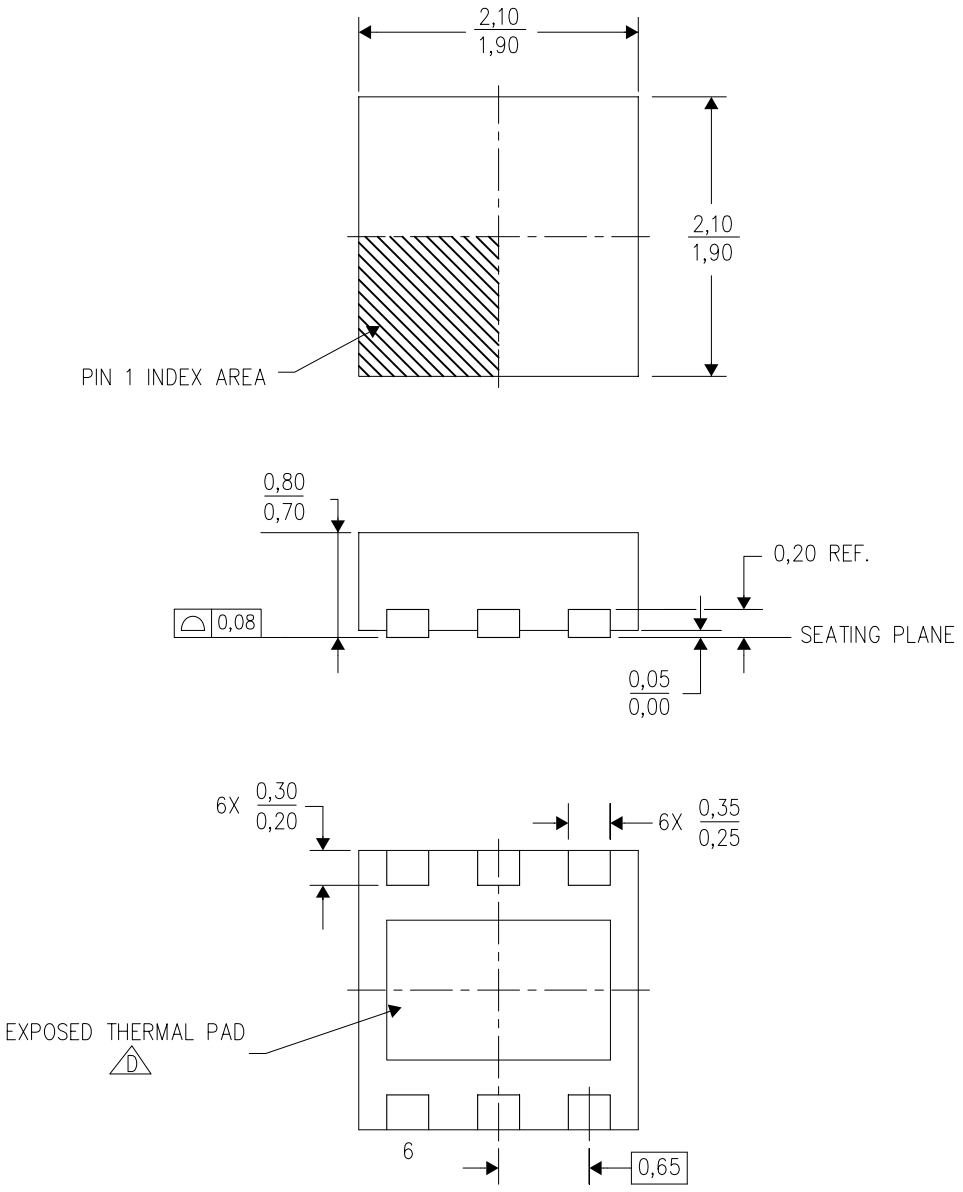


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72009YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS72009YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS720105DRVR	SON	DRV	6	3000	203.0	203.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS720105DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS720105YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS720105YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS72010DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS72010DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS720115DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS720115DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS72011DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS72011DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS72011YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS72011YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS72012DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS72012DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS72012YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS72012YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS72013YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS72013YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS72015DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS72015DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS72015DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS72015DRVT	SON	DRV	6	250	210.0	185.0	35.0
TPS72015YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS72015YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS72017YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS72017YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0
TPS72018DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS72018DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS72018YZUR	DSBGA	YZU	5	3000	210.0	185.0	35.0
TPS72018YZUT	DSBGA	YZU	5	250	210.0	185.0	35.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

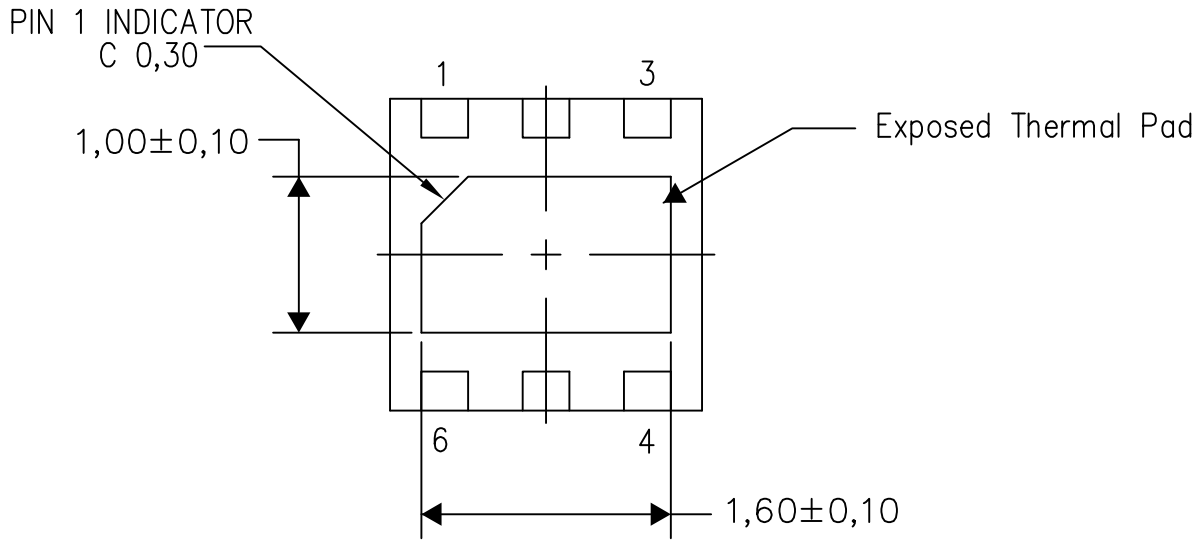
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



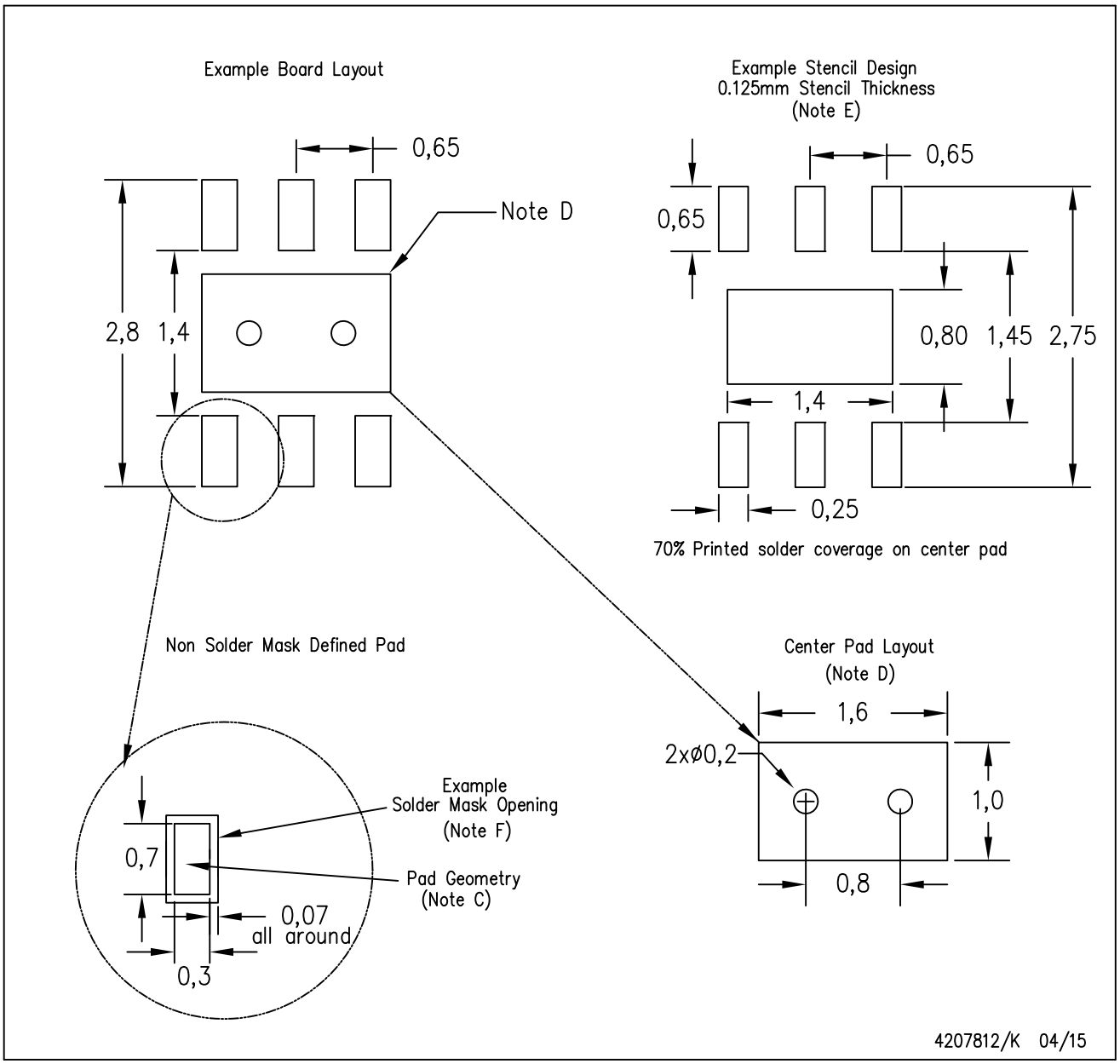
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



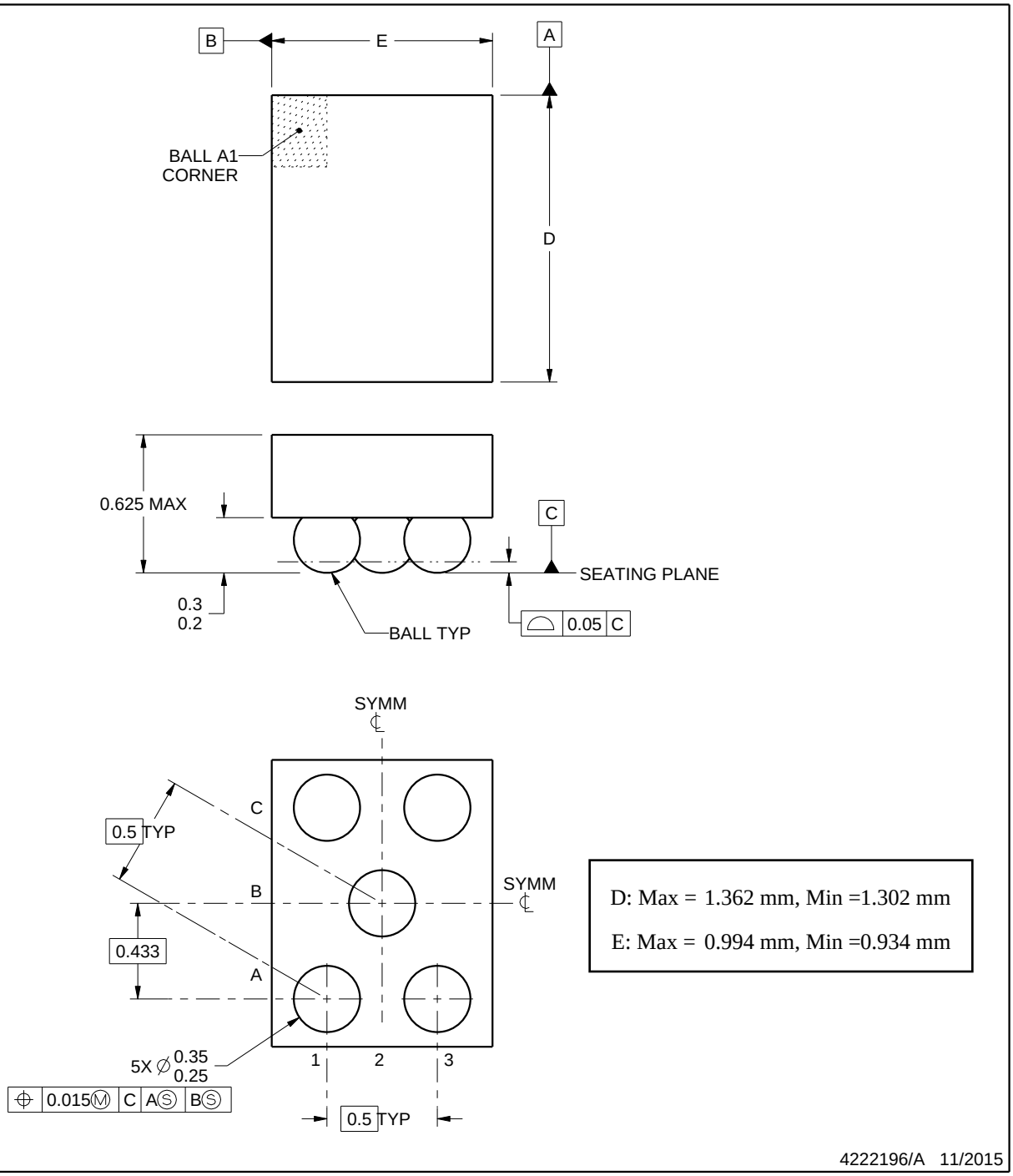
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

PACKAGE OUTLINE

YZU0005

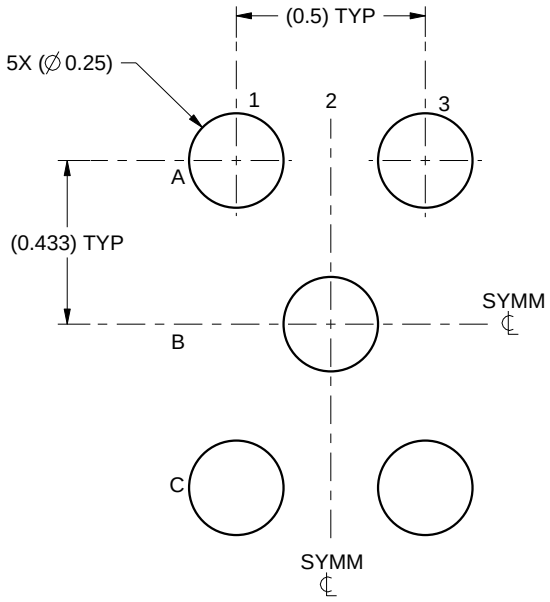
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

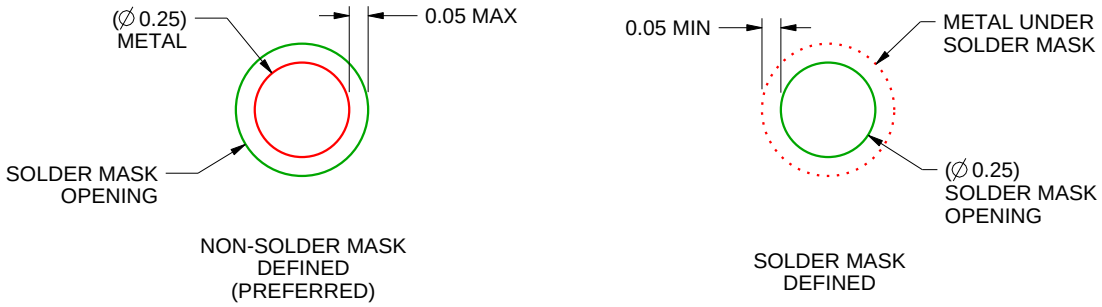


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4222196/A 11/2015

NOTES: (continued)

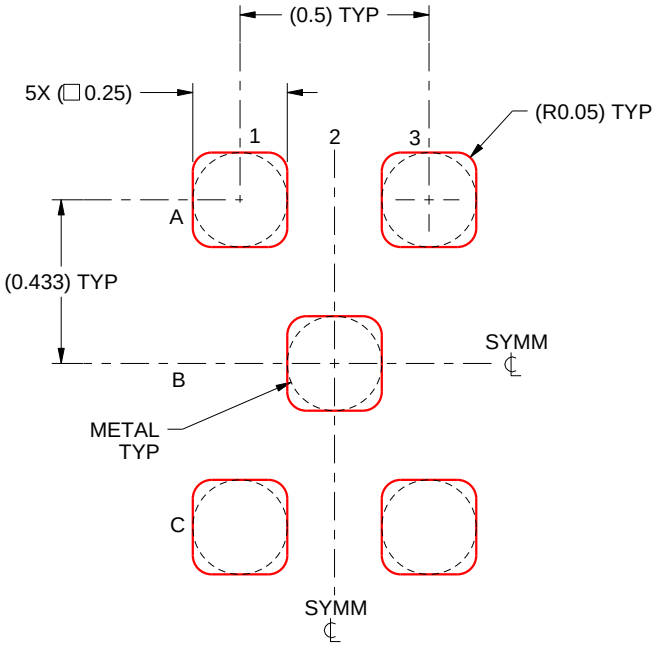
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4222196/A 11/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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