

CAP-FREE NMOS 250-mA LOW-DROPOUT REGULATOR WITH REVERSE-CURRENT PROTECTION

Check for Samples: [TPS73201-Q1](#), [TPS73225-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Stable with No Output Capacitor or Any Value or Type of Capacitor
- Input Voltage Range: 1.7 V to 5.5 V
- Ultralow Dropout Voltage: 40 mV Typ at 250 mA
- Excellent Load Transient Response—With or Without Optional Output Capacitor
- New NMOS Topology Provides Low Reverse Leakage Current
- Low Noise: 30 μV_{RMS} Typ (10 kHz to 100 kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy (Line, Load, and Temperature)
- Less Than 1 μA Max I_{Q} in Shutdown Mode
- Thermal Shutdown and Specified Min/Max Current Limit Protection
- Available in Multiple Output Voltage Versions
 - Fixed Outputs of 1.2 V, 1.5 V, 1.6 V, 1.8 V, 2.5 V, 3 V, 3.3 V, and 5 V
 - Adjustable Outputs From 1.2 V to 5.5 V
 - Custom Outputs Available

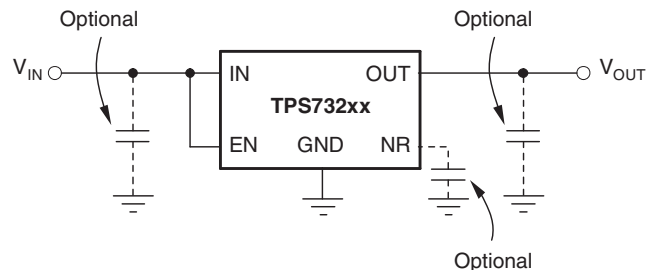
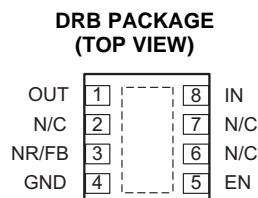
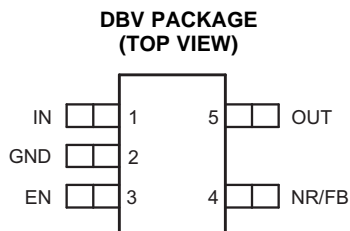
APPLICATIONS

- Portable/Battery-Powered Equipment
- Post-Regulation for Switching Supplies
- Noise-Sensitive Circuitry Such as VCOs
- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors

DESCRIPTION

The TPS732xx family of low-dropout (LDO) voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS732xx uses an advanced BiCMOS process to yield high precision while delivering low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 μA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1 μF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.



Typical Application Circuit for Fixed-Voltage Versions

Figure 1.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

| T _J | V _{OUT} (TYP) ⁽²⁾ | PACKAGE ⁽³⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------------------------------|------------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | Adjustable or 1.2 V ⁽⁴⁾ | SOT23-5 – DBV | Reel of 3000 | TPS73201QDBVRQ1 | PJOQ |
| | | VSON-8 – DRB | Reel of 3000 | TPS73201QDRBRQ1 | PSAQ |
| | 2.5 V | SOT23-5 – DBV | Reel of 3000 | TPS73225QDBVRQ1 | PJNQ |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Custom output voltages from 1.3 V to 4 V in 100-mV increments are available on a quick-turn basis for prototyping. Production quantities are available; minimum order quantities apply. Contact Texas Instruments for details and availability.
- (3) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (4) For fixed 1.2-V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted⁽¹⁾

| | TPS732xx | UNIT |
|--|---|------|
| V _{IN} range | -0.3 to 6 | V |
| V _{EN} range | -0.3 to 6 | V |
| V _{OUT} range | -0.3 to 5.5 | V |
| Peak output current | Internally limited | |
| Output short-circuit duration | Indefinite | |
| Continuous total power dissipation | See Power Dissipation Ratings | |
| Junction temperature range, T _J | -55 to +150 | °C |
| Storage temperature range | -65 to +150 | °C |
| ESD rating, HBM ⁽²⁾ | (H2) 4 | kV |
| ESD rating, CDM ⁽²⁾ | (C4) 1 | kV |
| ESD rating, MM ⁽²⁾ | (M2) 200 | V |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) ESD Protection Level per AEC Q100 Classification

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾⁽²⁾ | TPS732xx-Q1 ⁽³⁾ | | UNITS |
|---|----------------------------|--------|-------|
| | DRB | DBV | |
| | 8 PINS | 5 PINS | |
| θ_{JA} Junction-to-ambient thermal resistance ⁽⁴⁾ | 47.8 | 180 | °C/W |
| θ_{JCTop} Junction-to-case (top) thermal resistance ⁽⁵⁾ | 83 | 64 | |
| θ_{JB} Junction-to-board thermal resistance ⁽⁶⁾ | N/A | 35 | |
| ψ_{JT} Junction-to-top characterization parameter ⁽⁷⁾ | 2.1 | N/A | |
| ψ_{JB} Junction-to-board characterization parameter ⁽⁸⁾ | 17.8 | N/A | |
| θ_{JCbott} Junction-to-case (bottom) thermal resistance ⁽⁹⁾ | 12.1 | N/A | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953A](#).
- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).
- (3) Thermal data for the DRB and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
 - (a) DRB: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array.
 - (b) DBV: There is no exposed pad with the DBV package.
- (b) (a) DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
- (b) DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
- (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-in x 3-in copper area. To understand the effects of the copper area on thermal performance, see the [Power Dissipation](#) section of this data sheet.
- (4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (7) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
- (8) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
- (9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

POWER DISSIPATION RATINGS ⁽¹⁾

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A \leq 25^\circ\text{C}$ POWER RATING | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|-----------------------|---------|-----------------|-----------------|---|---|--|--|
| Low-K ⁽²⁾ | DBV | 64°C/W | 255°C/W | 3.9 mW/°C | 390 mW | 215 mW | 155 mW |
| High-K ⁽³⁾ | DBV | 64°C/W | 180°C/W | 5.6 mW/°C | 560 mW | 310 mW | 225 mW |
| High-K ⁽³⁾ | DRB | 1.2°C/W | 40°C/W | 25.0 mW/°C | 2.50 W | 1.38 W | 1 W |

- (1) See [Power Dissipation](#) in the *Application Information* section for more information related to thermal design.
- (2) The JEDEC Low-K (1s) board design used to derive this data was a 3-inch x 3-inch, two-layer board with 2-ounce copper traces on top of the board.
- (3) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}^{(1)}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|--|--|--|----------------------|----------------|---------------------|
| V_{IN} | Input voltage range ⁽¹⁾ | | 1.7 | | 5.5 | V |
| V_{FB} | Internal reference (TPS73201) | $T_J = 25^\circ\text{C}$ | 1.198 | 1.2 | 1.21 | V |
| V_{OUT} | Output voltage range (TPS73201) ⁽²⁾ | | V_{FB} | | $5.5 - V_{DO}$ | V |
| | Accuracy ⁽¹⁾ | Nominal | $T_J = 25^\circ\text{C}$ | | +0.5% | |
| | | V_{IN} , I_{OUT} , and T_J | $(V_{OUT} + 0.5\text{ V}) \leq V_{IN} \leq 5.5\text{ V}$, $10\text{ mA} \leq I_{OUT} \leq 250\text{ mA}$ | -1% | $\pm 0.5\%$ | +1% |
| $\Delta V_{OUT}\%/\Delta V_{IN}$ | Line regulation ⁽¹⁾ | $(V_{OUT(nom)} + 0.5\text{ V}) \leq V_{IN} \leq 5.5\text{ V}$ | | 0.06 | | %/V |
| $\Delta V_{OUT}\%/\Delta I_{OUT}$ | Load regulation | $1\text{ mA} \leq I_{OUT} \leq 250\text{ mA}$ | | 0.002 | | %mA |
| | | $10\text{ mA} \leq I_{OUT} \leq 250\text{ mA}$ | | 0.0008 | | |
| V_{DO} | Dropout voltage ⁽³⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$) | $I_{OUT} = 250\text{ mA}$ | | 40 | 150 | mV |
| $Z_O(\text{DO})$ | Output impedance in dropout | $1.7\text{ V} \leq V_{IN} \leq (V_{OUT} + V_{DO})$ | | 0.25 | | Ω |
| I_{CL} | Output current limit | $V_{OUT} = 0.9 \times V_{OUT(nom)}$ | 250 | 425 | 600 | mA |
| I_{SC} | Short-circuit current | $V_{OUT} = 0\text{ V}$ | | 300 | | mA |
| I_{REV} | Reverse leakage current ⁽⁴⁾ ($-I_{IN}$) | $V_{EN} \leq 0.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq V_{OUT}$ | | 0.1 | 10 | μA |
| I_{GND} | Ground pin current | $I_{OUT} = 10\text{ mA}$ (I_Q) | | 400 | 550 | μA |
| | | $I_{OUT} = 250\text{ mA}$ | | 650 | 950 | |
| I_{SHDN} | Shutdown current (I_{GND}) | $V_{EN} \leq 0.5\text{ V}$, $V_{OUT} \leq V_{IN} \leq 5.5$ | | 0.02 | 1 | μA |
| PSRR | Power-supply rejection ratio (ripple rejection) | $f = 100\text{ Hz}$, $I_{OUT} = 250\text{ mA}$ | | 58 | | dB |
| | | $f = 10\text{ kHz}$, $I_{OUT} = 250\text{ mA}$ | | 37 | | |
| V_N | Output noise voltage BW = 10 Hz – 100 kHz | $C_{OUT} = 10\text{ }\mu\text{F}$, No C_{NR} | | $27 \times V_{OUT}$ | | μV_{RMS} |
| | | $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$ | | $8.5 \times V_{OUT}$ | | |
| t_{STR} | Startup time | $V_{OUT} = 3\text{ V}$, $R_L = 30\text{ }\Omega$ $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$ | | 600 | | μs |
| $V_{EN}(\text{HI})$ | Enable high (enabled) | | 1.7 | | V_{IN} | V |
| $V_{EN}(\text{LO})$ | Enable low (shutdown) | | 0 | | 0.5 | V |
| $I_{EN}(\text{HI})$ | Enable pin current (enabled) | $V_{EN} = 5.5\text{ V}$ | | 0.02 | 0.1 | μA |
| T_{SD} | Thermal shutdown temperature | Shutdown, Temperature increasing | | 160 | | $^\circ\text{C}$ |
| | | Reset, Temperature decreasing | | 140 | | |

- (1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 1.7 V, whichever is greater.
- (2) TPS73201 is tested at $V_{OUT} = 2.5\text{ V}$.
- (3) V_{DO} is not measured for the TPS73215 or TPS73216, because minimum $V_{IN} = 1.7\text{ V}$.
- (4) Fixed-voltage versions only; see the *Application Information* section for more information.

FUNCTIONAL BLOCK DIAGRAMS

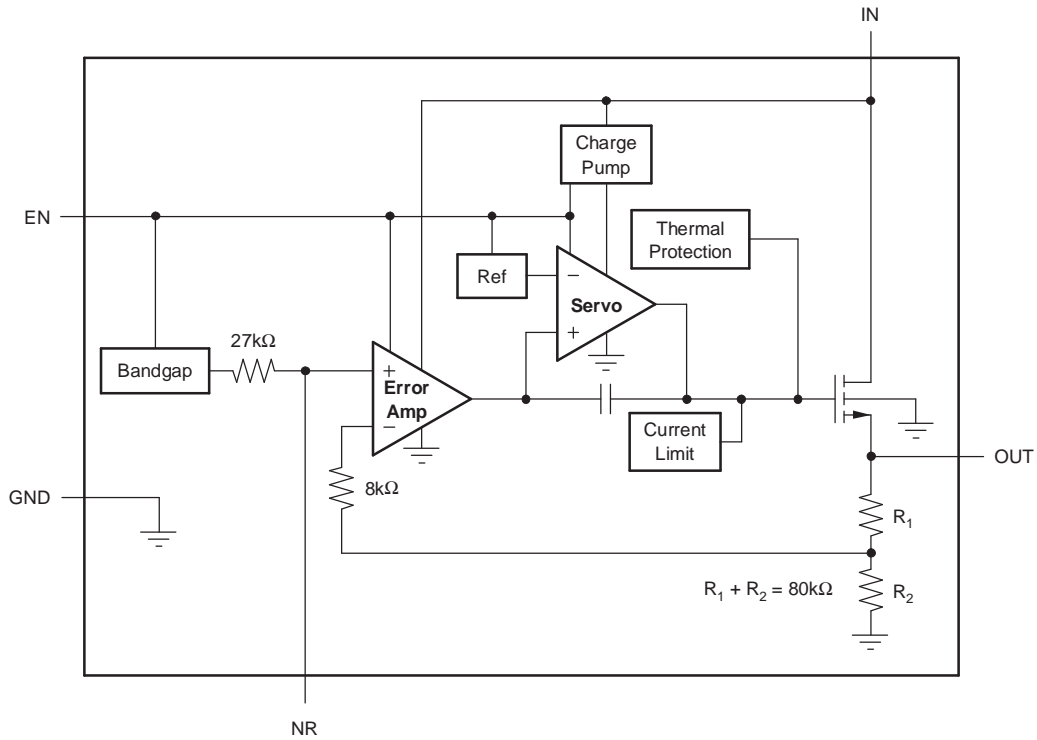


Figure 2. Fixed Voltage Version

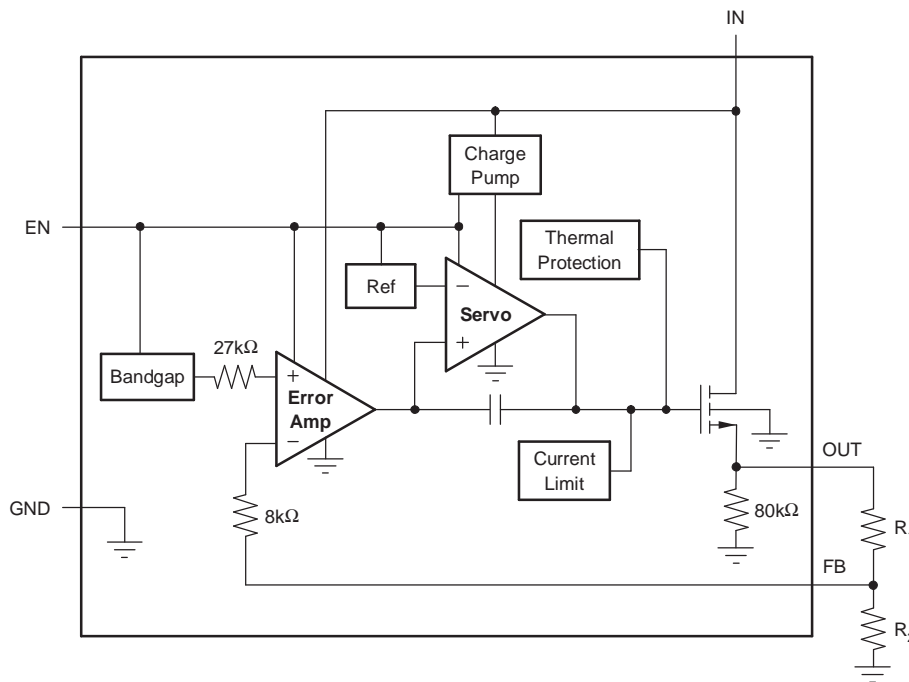


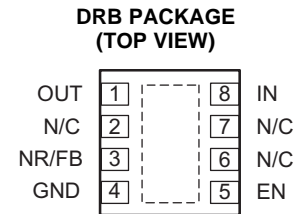
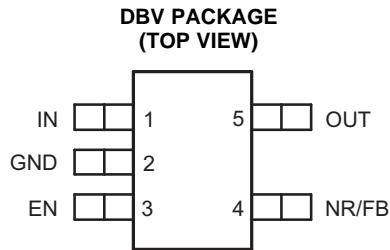
Figure 3. Adjustable Voltage Version

Table 1. Standard 1% Resistor Values for Common Output Voltages

| V _{OUT} | R ₁ | R ₂ |
|------------------|----------------|----------------|
| 1.2V | Short | Open |
| 1.5V | 23.2kΩ | 95.3kΩ |
| 1.8V | 28.0kΩ | 56.2kΩ |
| 2.5V | 39.2kΩ | 36.5kΩ |
| 2.8V | 44.2kΩ | 33.2kΩ |
| 3.0V | 46.4kΩ | 30.9kΩ |
| 3.3V | 52.3kΩ | 30.1kΩ |
| 5.0V | 78.7kΩ | 24.9kΩ |

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$;
 $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

| NAME | TERMINAL NO. | | DESCRIPTION |
|------|--------------|---------|---|
| | DBV | DRB | |
| IN | 1 | 8 | Unregulated input supply |
| GND | 2 | 4, Pad | Ground |
| EN | 3 | 5 | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the <i>Shutdown</i> section under <i>Applications Information</i> for more details. EN can be connected to IN if not used. |
| NR | 4 | 3 | Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to low levels. |
| FB | 4 | 3 | Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device. |
| NC | — | 2, 6, 7 | No internal connection |
| OUT | 5 | 1 | Output of the regulator. There are no output capacitor requirements for stability. |

TYPICAL CHARACTERISTICS

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$, unless otherwise noted

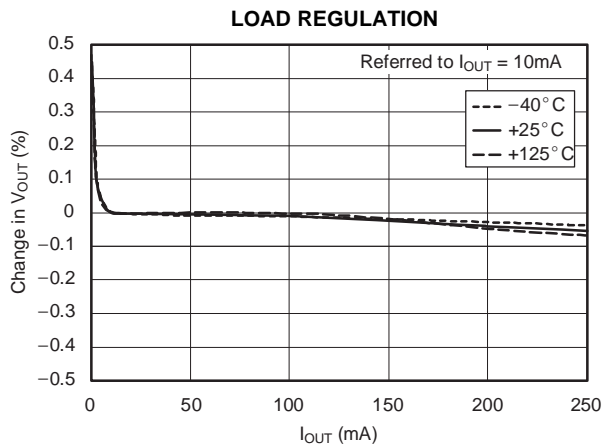


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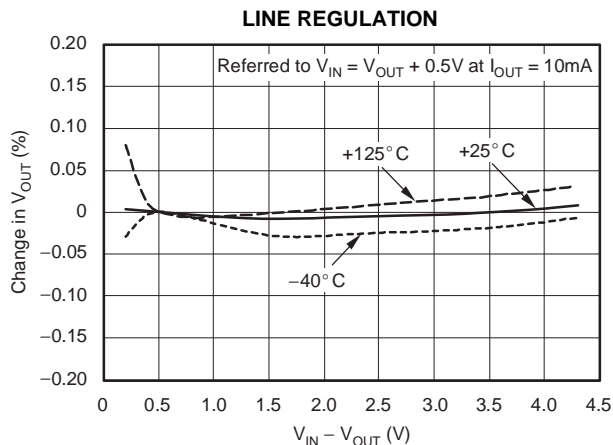


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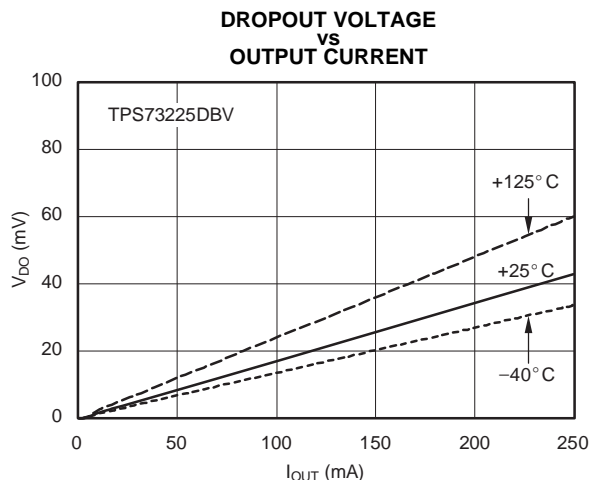


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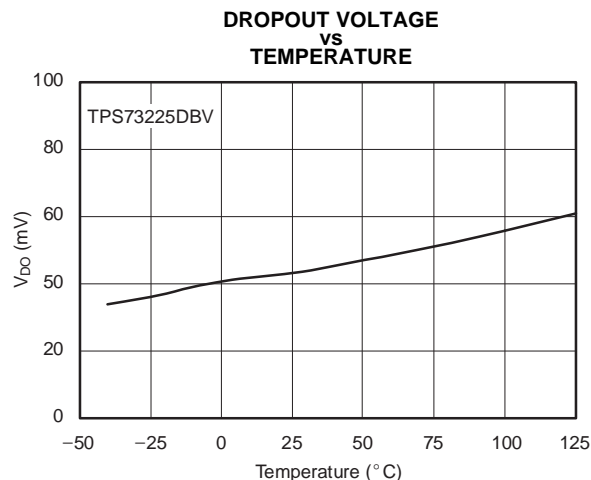


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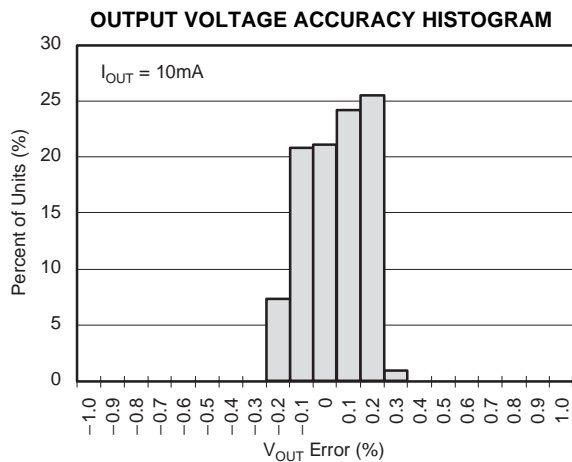


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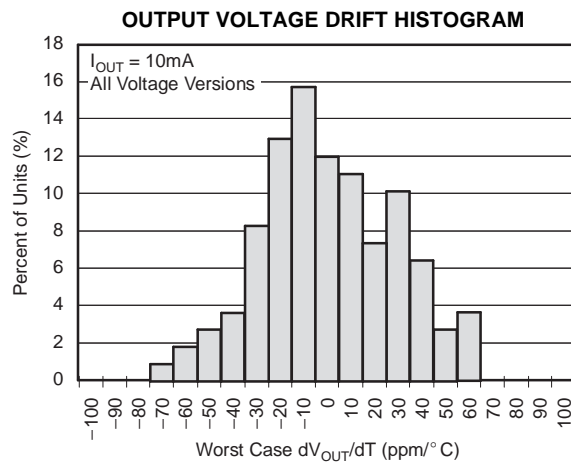


Figure 9.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$, unless otherwise noted

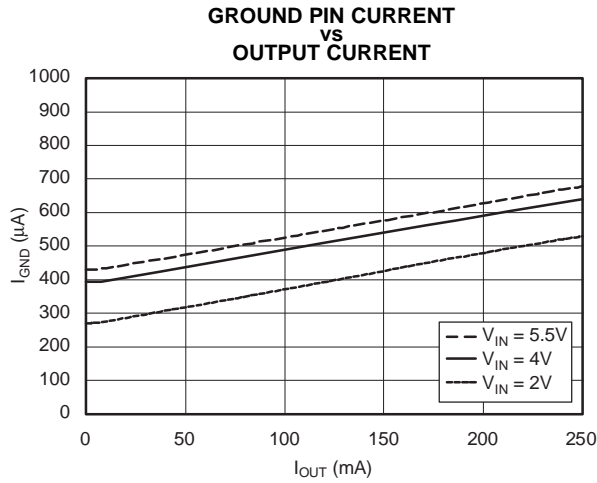


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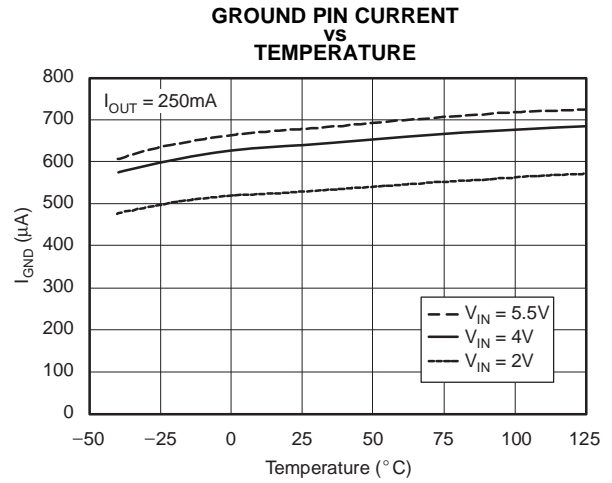


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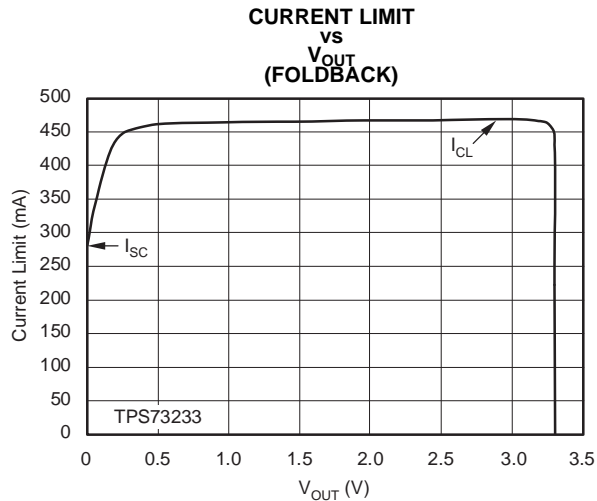


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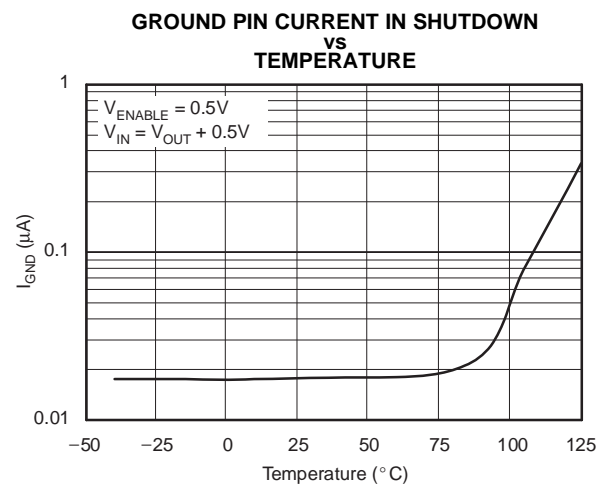


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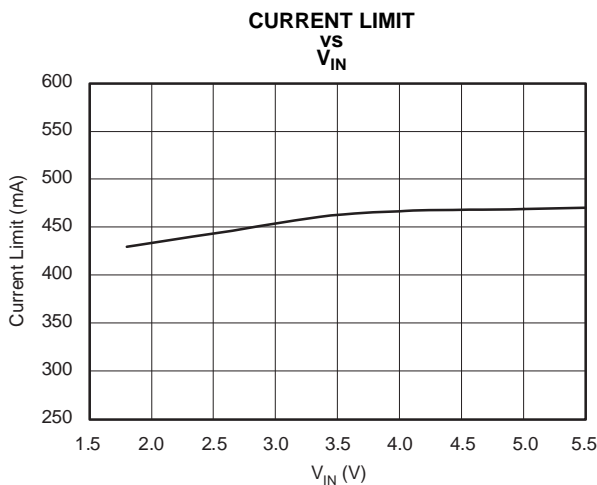


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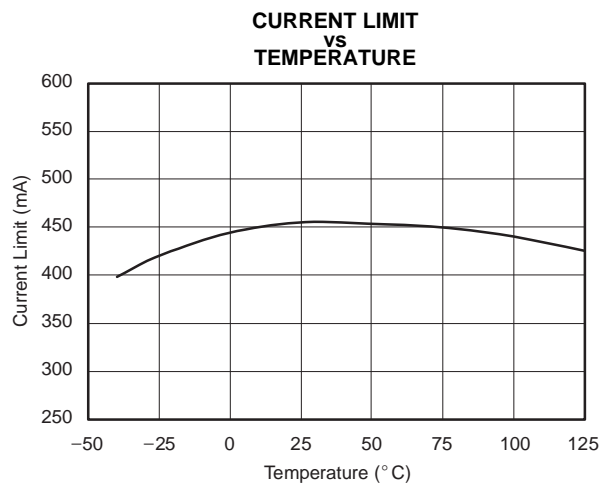


Figure 15.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted

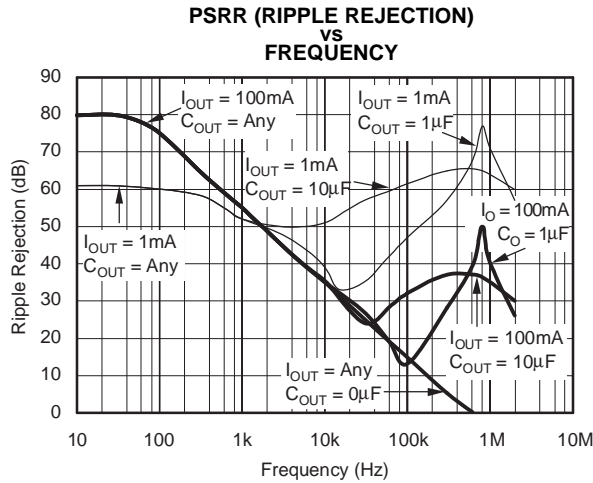


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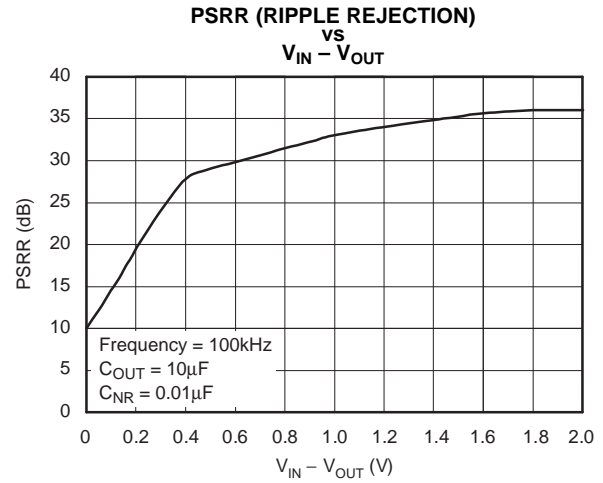


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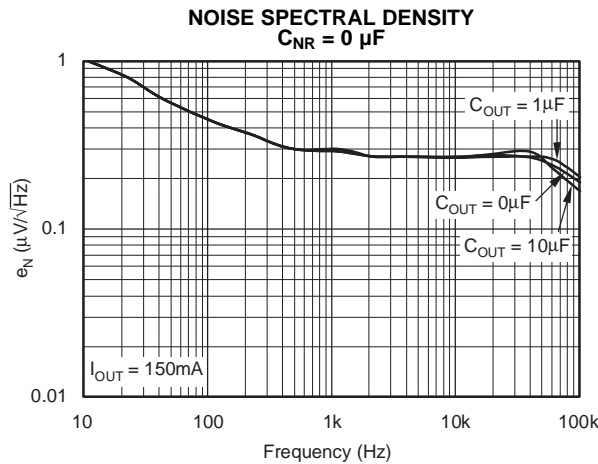


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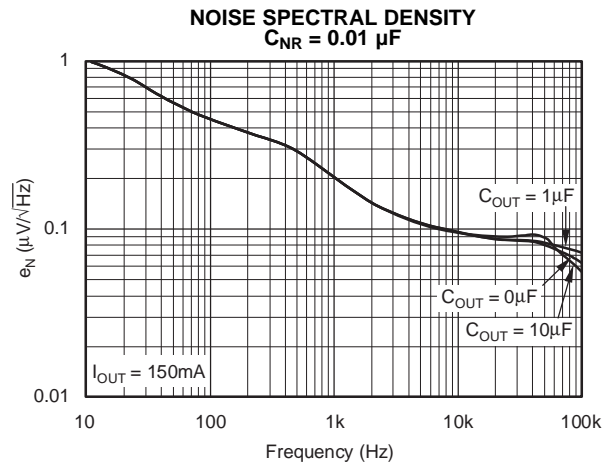


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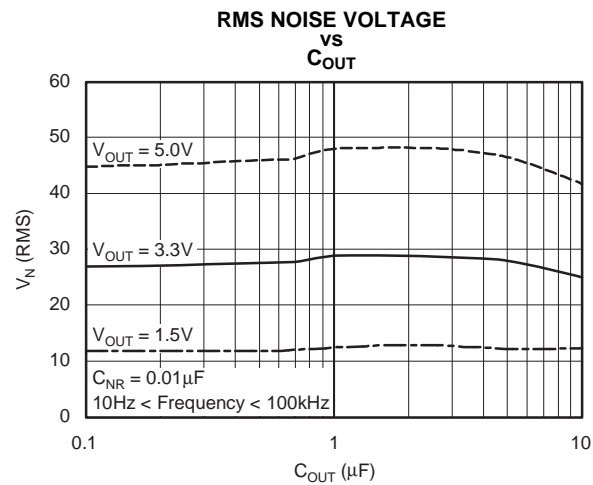


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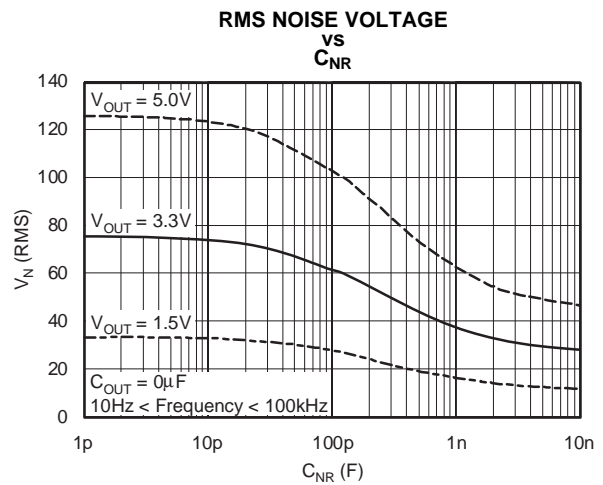


Figure 21.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$, unless otherwise noted

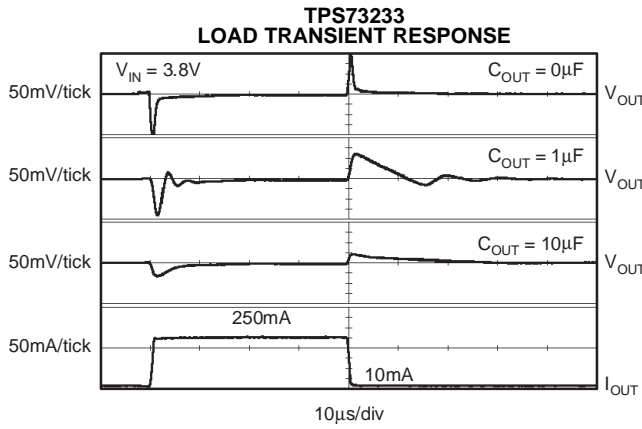


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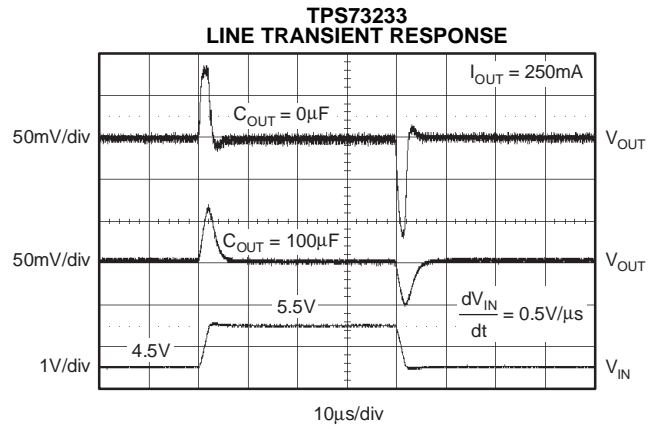


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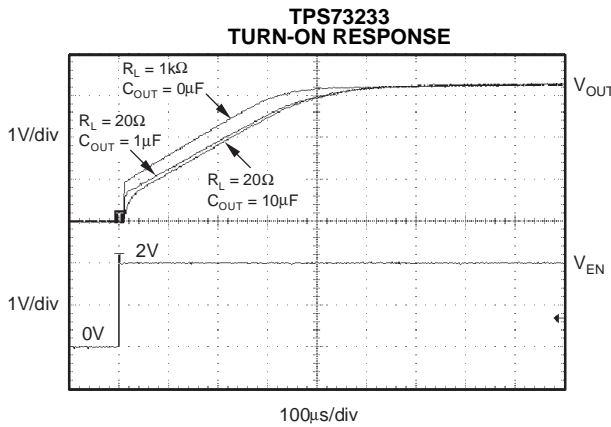


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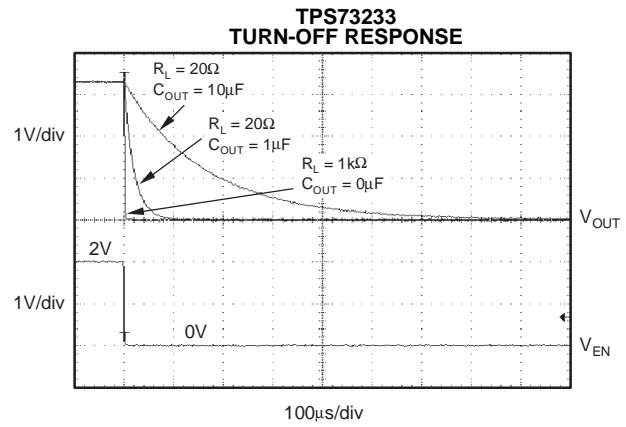


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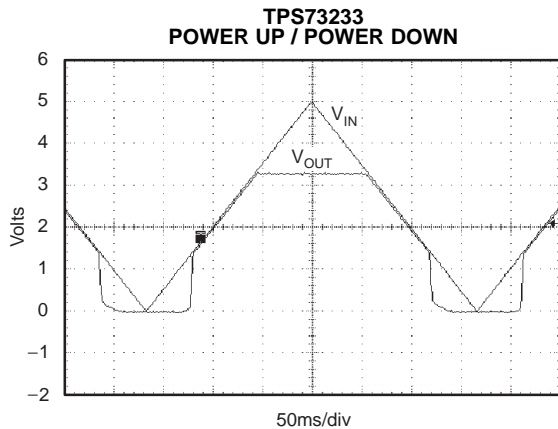


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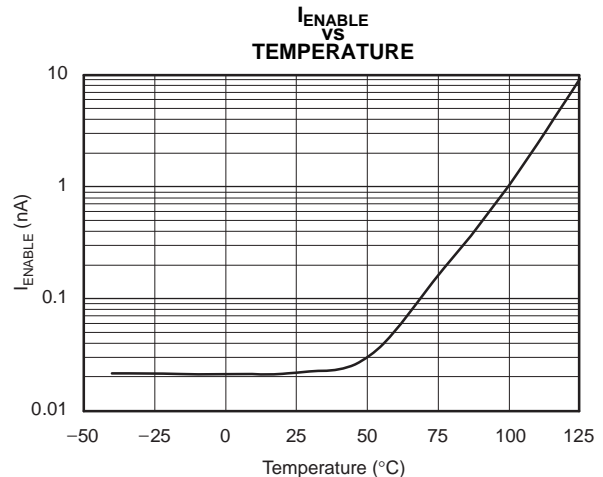


Figure 27.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted

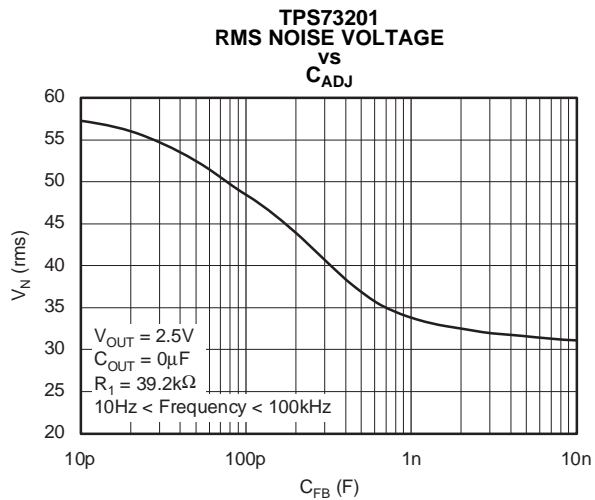


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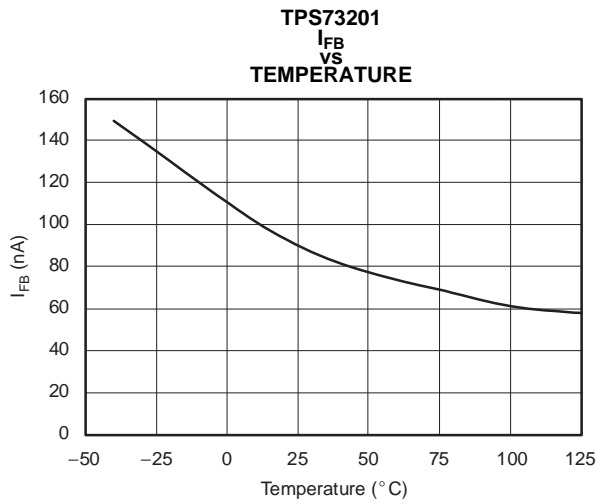


Figure 29.

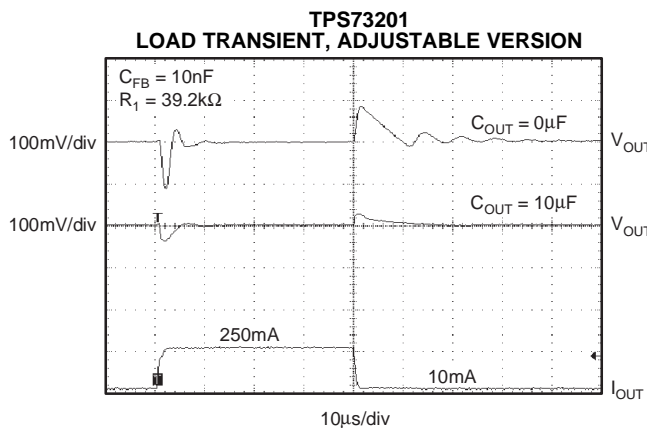


Figure 30.

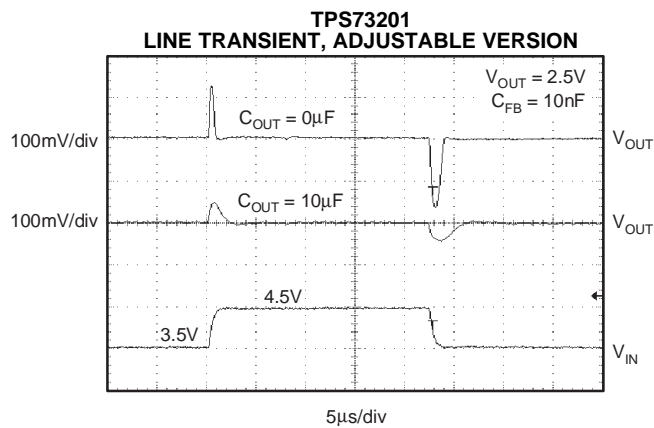


Figure 31.

APPLICATION INFORMATION

The TPS732xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 32 shows the basic circuit connections for the fixed voltage models. Figure 33 gives the connections for the adjustable output version (TPS73201).

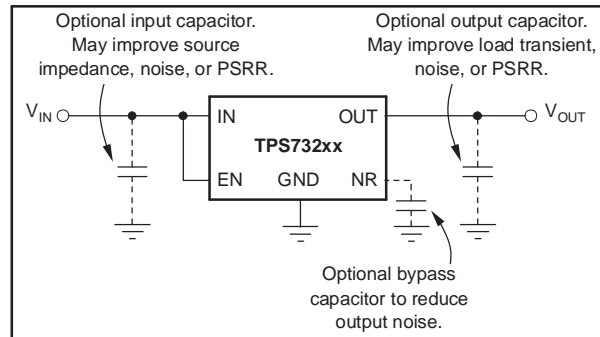


Figure 32. Typical Application Circuit for Fixed-Voltage Versions

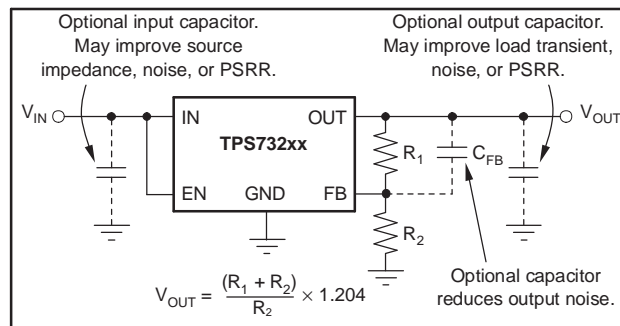


Figure 33. Typical Application Circuit for Adjustable-Voltage Versions

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 33. Sample resistor values for common output voltages are shown in Figure 3. For best accuracy, make the parallel combination of R_1 and R_2 approximately 19 k Ω .

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- μ F to 1- μ F low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732xx does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where $V_{IN} - V_{OUT} < 0.5$ V and multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF} . This reference is the dominant noise source within the TPS732xx and it generates approximately $32 \mu V_{RMS}$ (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32 \mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32 \mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR} .

An internal 27-k Ω resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR} , is connected from NR to ground. For $C_{NR} = 10$ nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of ~ 3.2 , giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (3)$$

for $C_{NR} = 10$ nF.

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristics section.

The TPS73201 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB} , from the output to the FB pin will reduce output noise and improve load transient performance.

The TPS732xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT} . The charge pump generates $\sim 250 \mu V$ of switching noise at ~ 2 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT} .

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS732xx internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See [Figure 12](#) in the *Typical Characteristics* section for a graph of I_{OUT} vs V_{OUT} .

Shutdown

The Enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (max) turns the regulator off and drops the ground pin current to approximately 10 nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN} . When a pullup resistor is used, and operation down to 1.8 V is required, use pullup resistor values below 50 k Ω .

Dropout Voltage

The TPS732xx uses an NMOS pass transistor to achieve extremely low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large step changes in load current, the TPS732xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of $V_{IN} - V_{OUT}$ above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with $(V_{IN} - V_{OUT})$ close to dc dropout levels], the TPS732xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 μ F) from the output pin to ground will reduce undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, C_{FB} , from the output to the adjust pin will also improve the transient response.

The TPS732xx does not have active pulldown when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega} \quad (4)$$

(Adjustable voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2)} \quad (5)$$

Reverse Current

The NMOS pass element of the TPS732xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80-k Ω internal resistor divider to ground (see [Figure 2](#) and [Figure 3](#)).

For the TPS73201, reverse current may flow when V_{FB} is more than 1 V above V_{IN} .

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS732xx into thermal shutdown will degrade device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the Power Dissipation Ratings table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

Package Mounting

Solder pad footprint recommendations for the TPS732xx are presented in the *Solder Pad Recommendations for Surface-Mount Devices (SBFA015)* application bulletin, available from the Texas Instruments web site at www.ti.com.

REVISION HISTORY

| Changes from Revision D (March 2009) to Revision E | Page |
|--|------|
| • Deleted TPS73215-Q1, TPS73216-Q1, TPS73218-Q1, TPS73230-Q1, TPS73233-Q1, and TPS73250-Q1 from the data sheet | 1 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS73201QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PJOQ | Samples |
| TPS73201QDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | PSAQ | Samples |
| TPS73225QDBVRQ1 | OBSOLETE | SOT-23 | DBV | 5 | | TBD | Call TI | Call TI | -40 to 125 | PJNQ | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS73201-Q1, TPS73225-Q1 :

- Catalog: [TPS73201](#), [TPS73225](#)
- Enhanced Product: [TPS73201-EP](#), [TPS73225-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS73201QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS73201QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

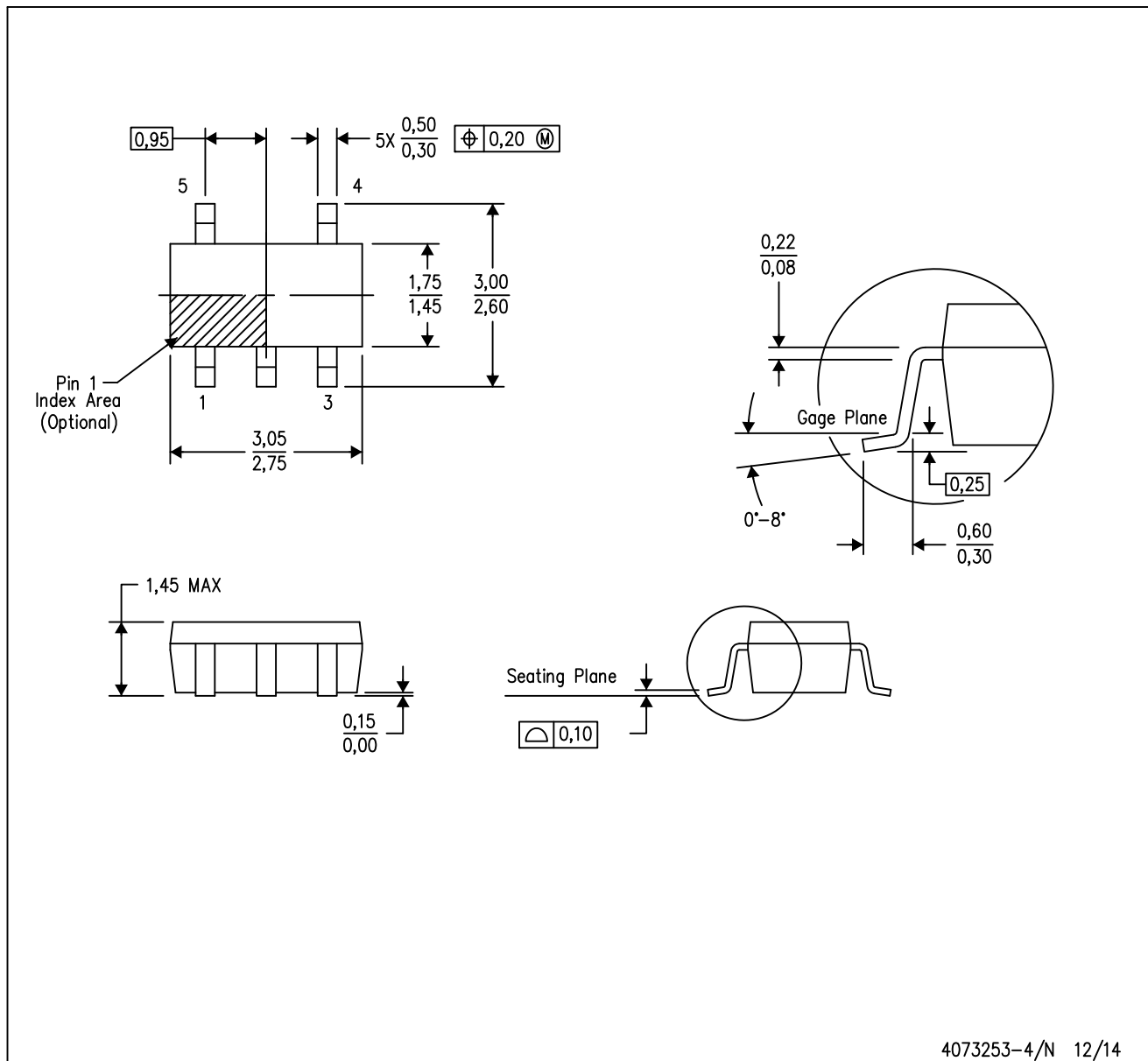
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS73201QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS73201QDRBRQ1 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |

DBV (R-PDSO-G5)

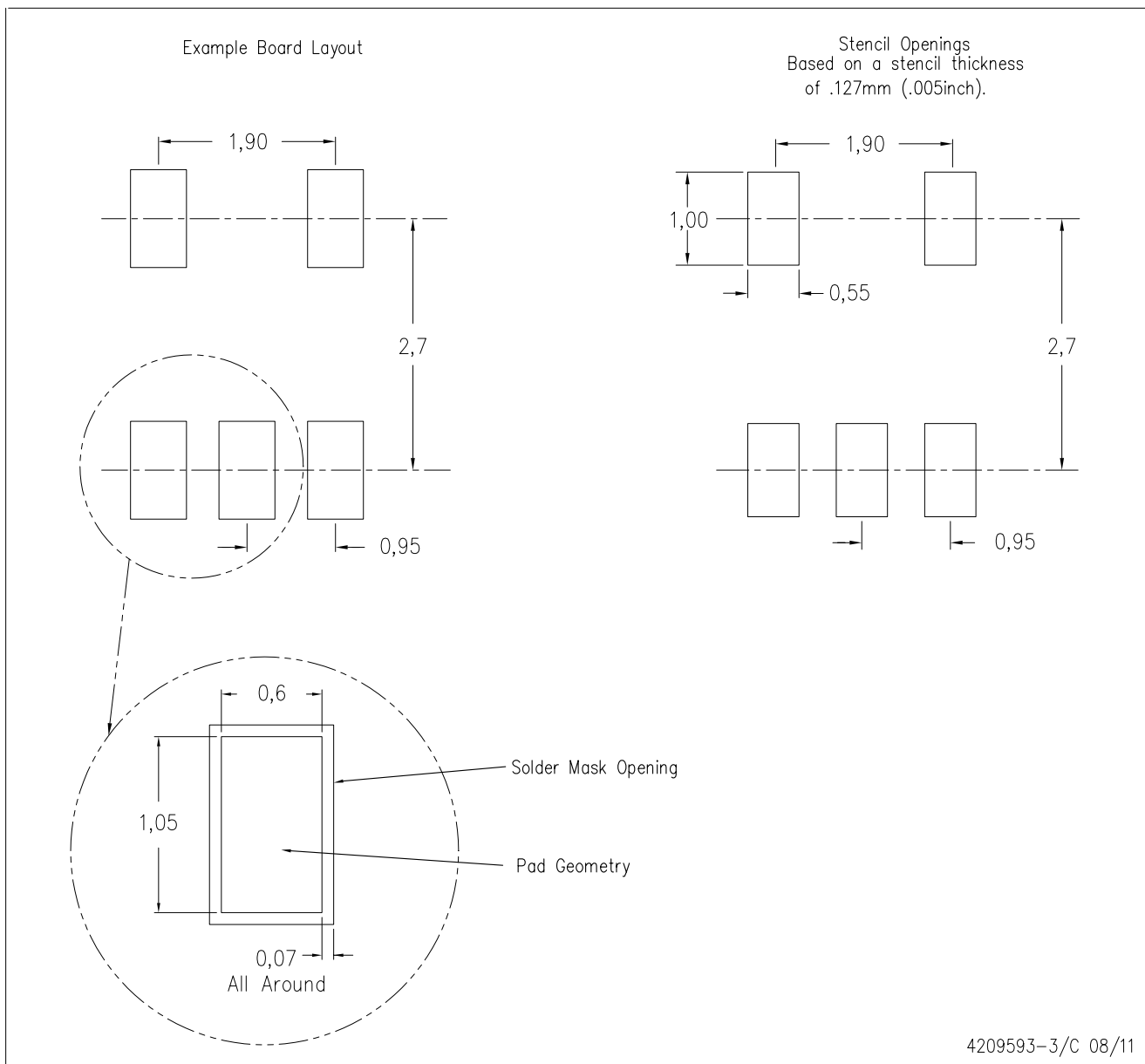
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

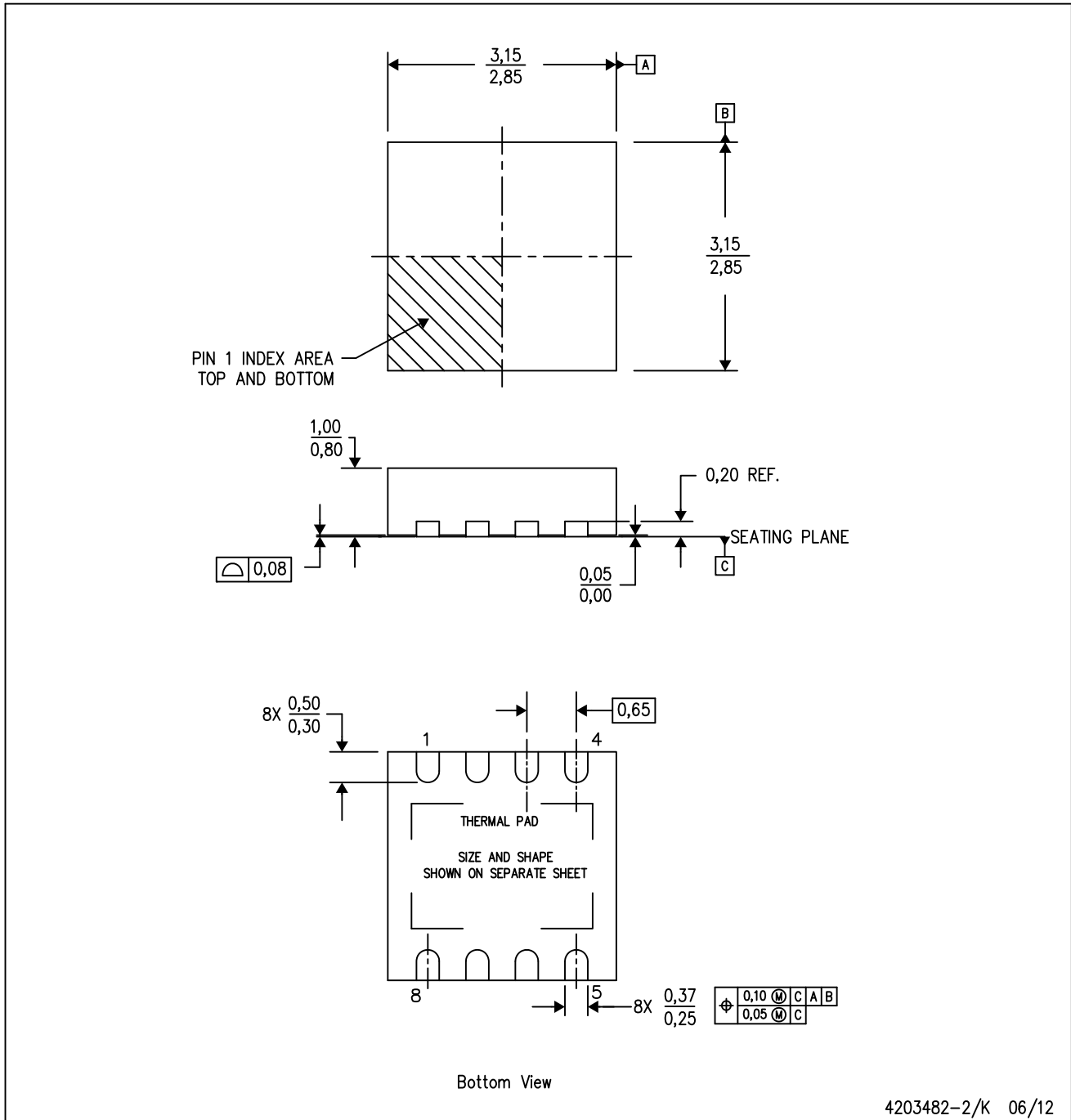
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)

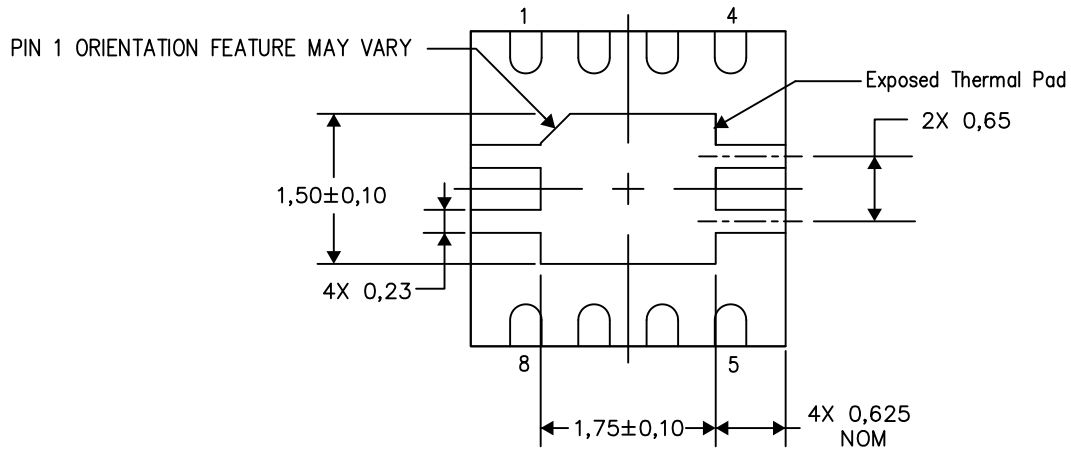
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

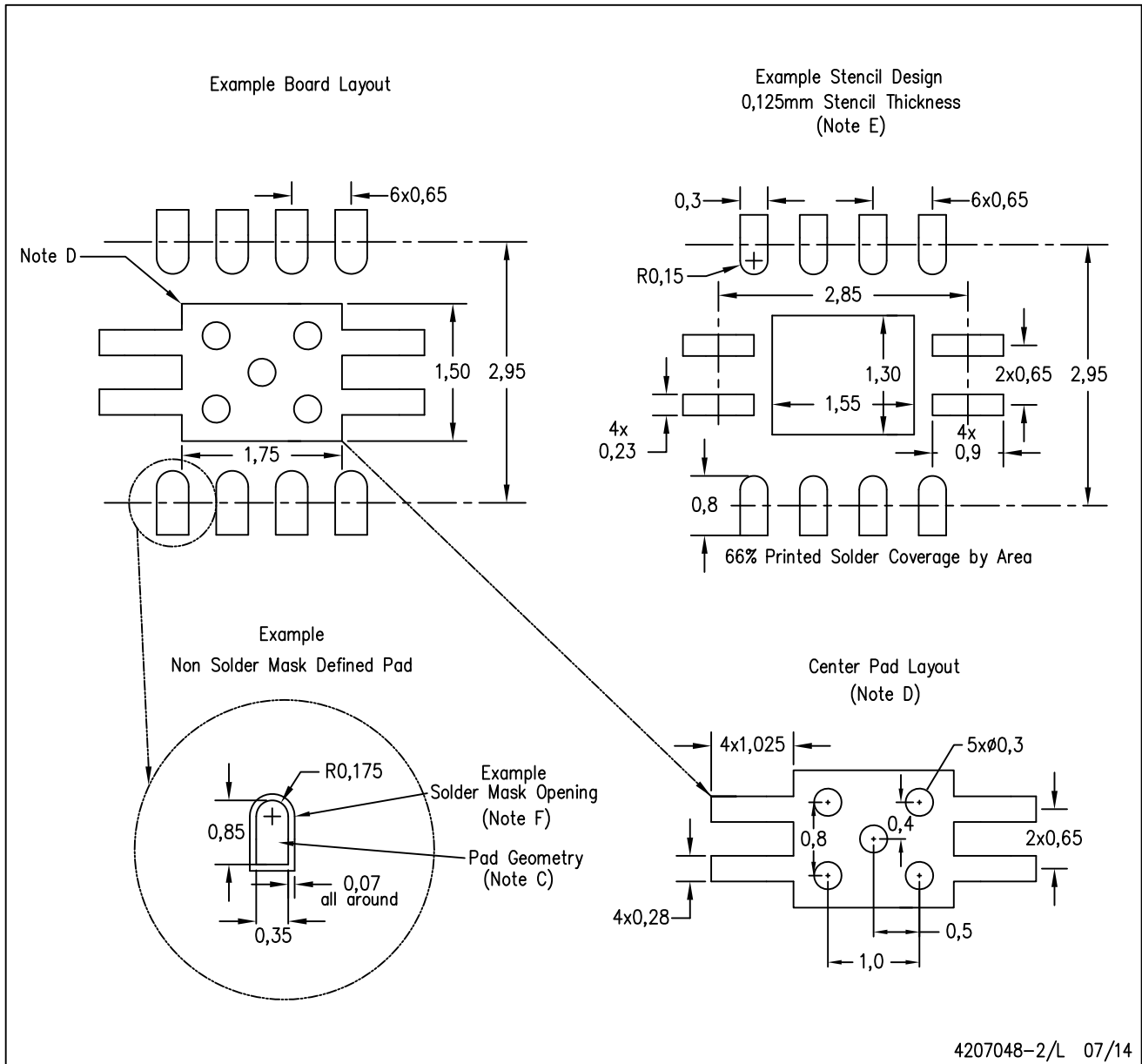
Exposed Thermal Pad Dimensions

4206340-2/P 07/14

NOTE: All linear dimensions are in millimeters

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.

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