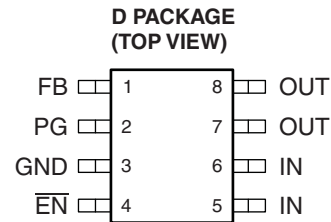


## FEATURES

- Qualified for Automotive Applications
- 150-mA Low-Dropout (LDO) Voltage Regulator
- Dropout Voltage to 85 mV (Typ) at 150 mA (TPS76550)
- Ultra-Low 35- $\mu$ A (Typ) Quiescent Current
- 3% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open-Drain Power Good Output
- Thermal Shutdown Protection

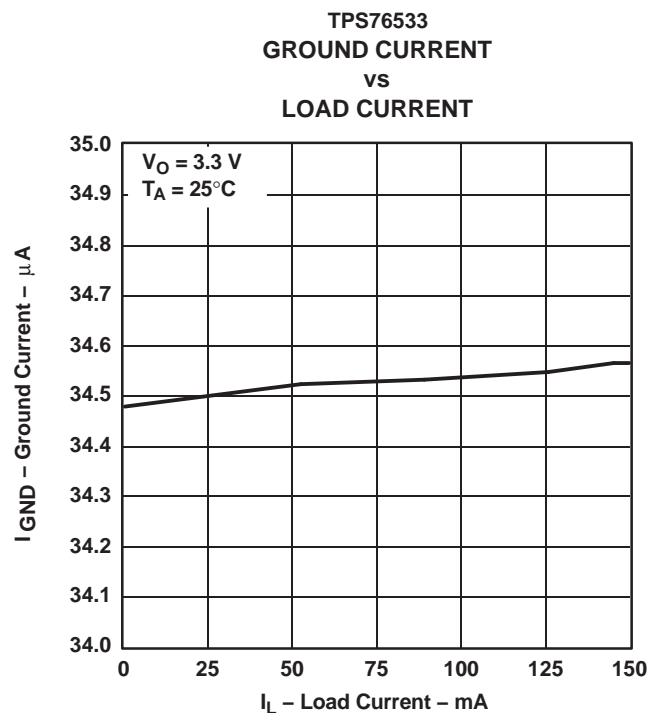
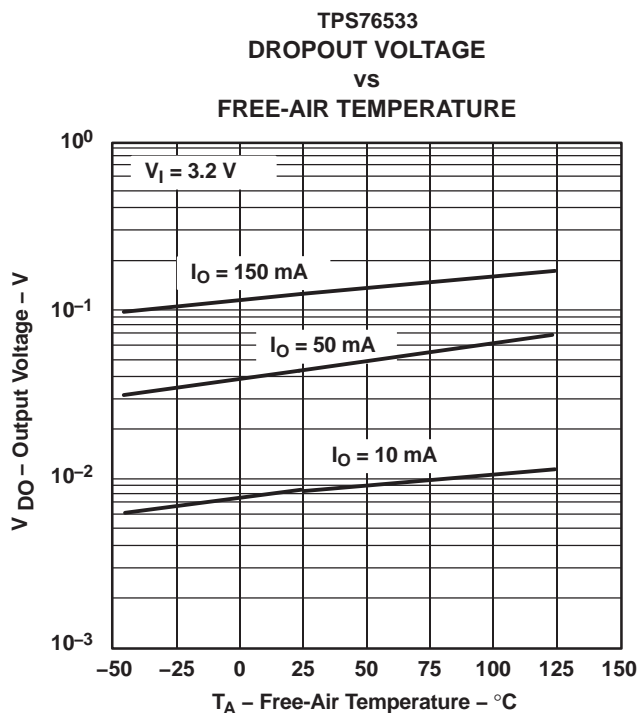


## DESCRIPTION/ORDERING INFORMATION

This device is designed to have an ultra-low quiescent current and be stable with a 4.7- $\mu$ F capacitor. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 85 mV at an output current of 150 mA for the TPS76550) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 35  $\mu$ A over the full range of output current, 0 mA to 150 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to less than 1  $\mu$ A (typ).

Power good (PG) is an active-high output, which can be used to implement a power-on reset or a low-battery indicator.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





# TPS76501-Q1

## ULTRALOW QUIESCENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATOR

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### ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		VALUE	
$V_I$	Input voltage range	–0.3 V to 13.5 V	
	Voltage range at $\overline{EN}$	–0.3 V to 16.5 V	
	Maximum PG voltage	16.5 V	
$I_O$	Peak output current	Internally limited	
$P_D$	Continuous total power dissipation	See <i>Dissipation Ratings</i>	
$V_O$	Output voltage (OUT, FB)	7 V	
$T_J$	Operating virtual junction temperature range	–40°C to 125°C	
$T_{stg}$	Storage temperature range	–65°C to 150°C	
ESD	Electrostatic discharge rating	Human-Body Model	2000 V
		Machine Model	200 V
		Charged-Device Model	1500 V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network terminal ground.

### DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	POWER RATING $T_A < 25^\circ\text{C}$	DERATING FACTOR $T_A \geq 25^\circ\text{C}$	POWER RATING $T_A = 70^\circ\text{C}$	POWER RATING $T_A = 85^\circ\text{C}$
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

### RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_I$	Input voltage <sup>(1)</sup>	2.7	10	V
$V_O$	Output voltage	1.2	5.5	V
$I_O$	Output current <sup>(2)</sup>	0	150	mA
$T_J$	Operating virtual junction temperature	–40	125	°C

- (1) To calculate the minimum input voltage for your maximum output current, use the following equation:  $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$ .
- (2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

**ELECTRICAL CHARACTERISTICS**
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$ ,  $I_O = 10 \text{ } \mu\text{A}$ ,  $\overline{\text{EN}} = 0 \text{ V}$ ,  $C_O = 4.7 \text{ } \mu\text{F}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>J</sub>	MIN	TYP	MAX	UNIT
Output voltage <sup>(1)</sup>	TPS76501	5.5 V ≥ V <sub>O</sub> ≥ 1.25 V	25°C	V <sub>O</sub>			V
			–40°C to 125°C	0.97V <sub>O</sub>	1.03V <sub>O</sub>		
	TPS76515	2.7 V < V <sub>IN</sub> < 10 V	25°C	1.5			
			–40°C to 125°C	1.455	1.545		
	TPS76518	2.8 V < V <sub>IN</sub> < 10 V	25°C	1.8			
			–40°C to 125°C	1.746	1.854		
	TPS76525	3.5 V < V <sub>IN</sub> < 10 V	25°C	2.5			
			–40°C to 125°C	2.425	2.575		
	TPS76527	3.7 V < V <sub>IN</sub> < 10 V	25°C	2.7			
			–40°C to 125°C	2.619	2.781		
	TPS76528	3.8 V < V <sub>IN</sub> < 10 V	25°C	2.8			
			–40°C to 125°C	2.716	2.884		
	TPS76530	4 V < V <sub>IN</sub> < 10 V	25°C	3			
			–40°C to 125°C	2.910	3.090		
TPS76533	4.3 V < V <sub>IN</sub> < 10 V	25°C	3.3				
		–40°C to 125°C	3.201	3.399			
TPS76550	6 V < V <sub>IN</sub> < 10 V	25°C	5				
		–40°C to 125°C	4.850	5.150			
Quiescent current (GND current) <sup>(1)</sup>		10 μA < I <sub>O</sub> < 150 mA	25°C	35			μA
		I <sub>O</sub> = 150 mA	–40°C to 125°C	50			
Output voltage line regulation <sup>(1)(2)</sup> (ΔV <sub>O</sub> /V <sub>O</sub> )		V <sub>O</sub> + 1 V < V <sub>I</sub> ≤ 10 V	25°C	0.01			%/V
Load regulation		I <sub>O</sub> = 10 μA to 150 mA	–40°C to 125°C	0.3			%
Output noise voltage		BW = 300 Hz to 50 kHz, C <sub>O</sub> = 4.7 μF	25°C	200			μVrms
Output current limit		V <sub>O</sub> = 0 V	–40°C to 125°C	0.8		1.2	A
Thermal shutdown junction temperature				150			°C
Standby current		$\overline{\text{EN}} = V_I$ , 2.7 V < V <sub>I</sub> < 10 V	25°C	1			μA
			–40°C to 125°C	10			
FB input current	TPS76501	FB = 1.5 V	–40°C to 125°C	2			nA
High-level $\overline{\text{EN}}$ input voltage			–40°C to 125°C	2			V
Low-level $\overline{\text{EN}}$ input voltage			–40°C to 125°C	0.8			V
Power-supply ripple rejection <sup>(1)</sup>		f = 1 kHz, C <sub>O</sub> = 4.7 μF, I <sub>O</sub> = 10 mA	25°C	63			dB
PG	Minimum input voltage for valid PG	I <sub>O(PG)</sub> = 300 μA	–40°C to 125°C	1.1			V
	Trip threshold voltage	V <sub>O</sub> decreasing	–40°C to 125°C	92	98		%V <sub>O</sub>
	Hysteresis voltage	Measured at V <sub>O</sub>	–40°C to 125°C	0.5			%V <sub>O</sub>
	Output low voltage	V <sub>I</sub> = 2.7 V, I <sub>O(PG)</sub> = 1 mA	–40°C to 125°C	0.15	0.4		V
	Leakage current	V <sub>(PG)</sub> = 5 V	–40°C to 125°C			1	μA
$\overline{\text{EN}}$ input current		$\overline{\text{EN}} = 0 \text{ V}$	–40°C to 125°C	–1	0	1	μA
		$\overline{\text{EN}} = V_I$		–1		1	

(1) Minimum IN operating voltage is 2.7 V or V<sub>O(typ)</sub> + 1 V, whichever is greater. Maximum IN voltage 10 V.

(2) If V<sub>O</sub> ≤ 1.8 V then V<sub>I(min)</sub> = 2.7 V, V<sub>I(max)</sub> = 10 V:

$$\text{Line Regulation (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I(\text{max})} - 2.7 \text{ V})}{100} \times 1000$$

If V<sub>O</sub> ≥ 2.5 V then V<sub>I(min)</sub> = V<sub>O</sub> + 1 V, V<sub>I(max)</sub> = 10 V:

$$\text{Line Regulation (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I(\text{max})} - (V_O + 1 \text{ V}))}{100} \times 1000$$

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**ELECTRICAL CHARACTERISTICS (continued)**

$V_I = V_{O(\text{typ})} + 1 \text{ V}$ ,  $I_O = 10 \mu\text{A}$ ,  $\overline{\text{EN}} = 0 \text{ V}$ ,  $C_O = 4.7 \mu\text{F}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>J</sub>	MIN	TYP	MAX	UNIT
Dropout voltage <sup>(3)</sup>	TPS76528	$I_O = 150 \text{ mA}$	25°C		190		mV
			–40°C to 125°C			330	
	TPS76530		25°C		160		
			–40°C to 125°C			280	
	TPS76533		25°C		140		
			–40°C to 125°C			240	
	TPS76550		25°C		85		
			–40°C to 125°C			150	

(3) IN voltage equals  $V_{O(\text{typ})} - 100 \text{ mV}$  with output voltage set to 3.3 V nominal with external resistor divider. TPS76515, TPS76518, TPS76525, and TPS76527 dropout voltage limited by input voltage range limitations (i.e., TPS76530 input voltage must drop to 2.9 V for purpose of this test).

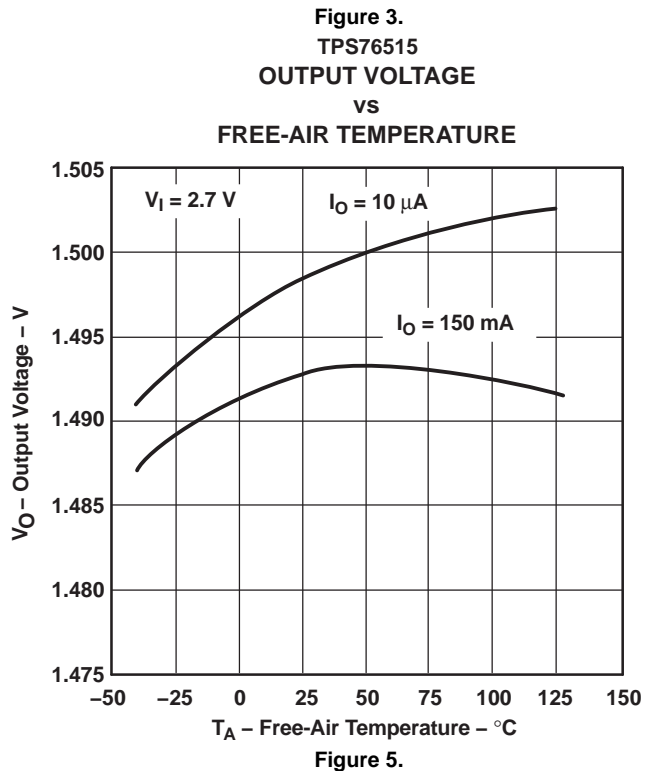
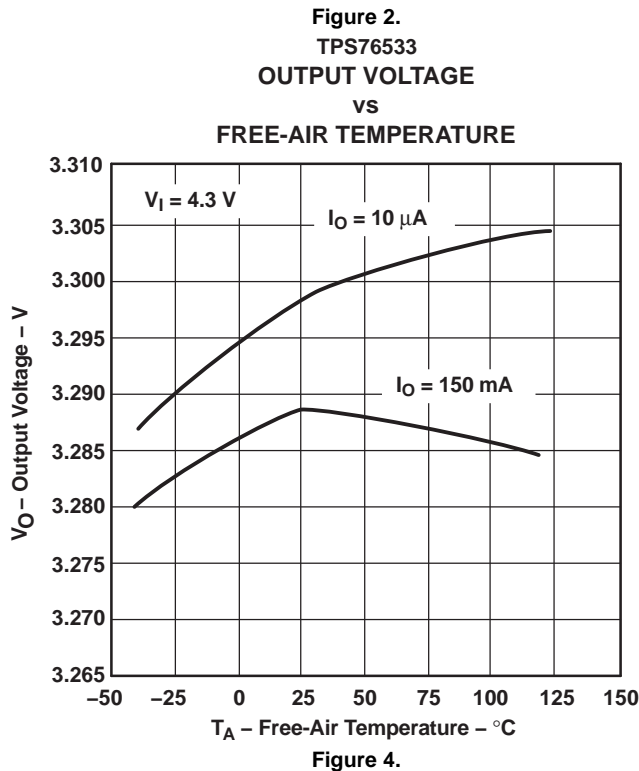
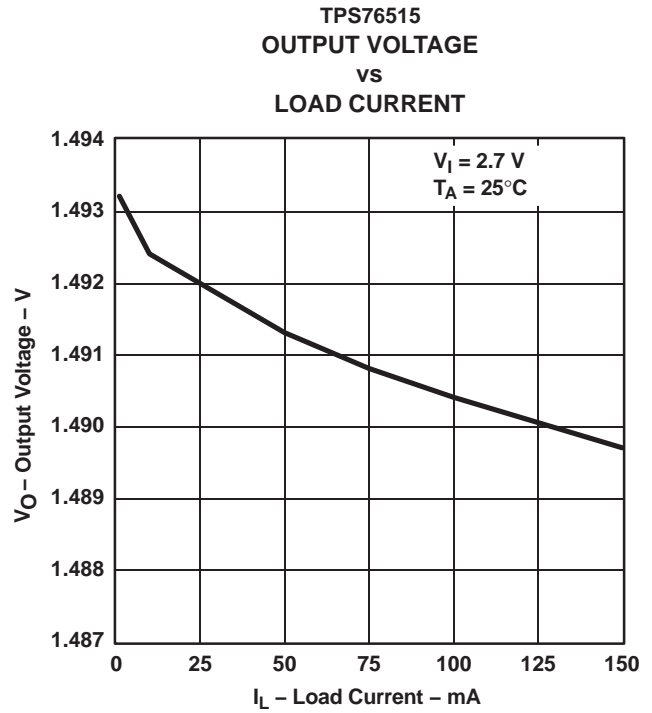
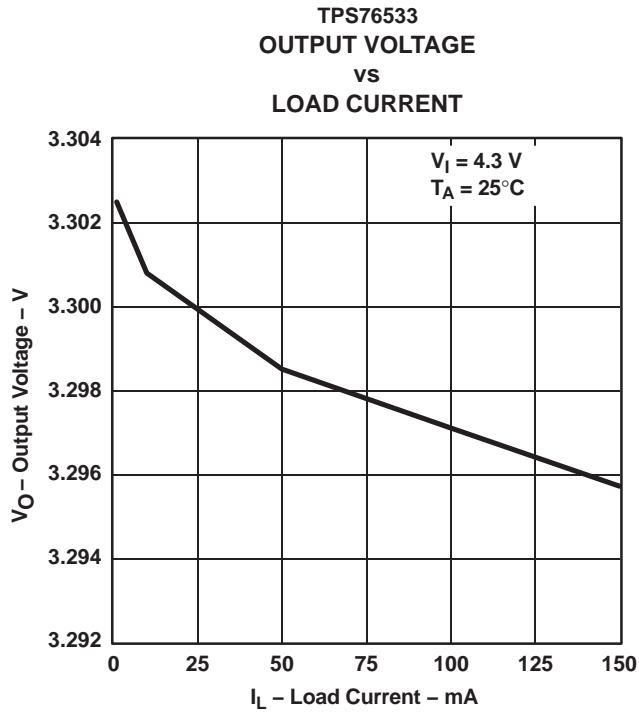
**TYPICAL CHARACTERISTICS**
**Table of Graphs**

		<b>FIGURE</b>
Output voltage	vs Load current	2, 3
	vs Free-air temperature	4, 5
Ground current	vs Load current	6, 7
	vs Free-air temperature	8, 9
Power-supply ripple rejection	vs Frequency	10
Output spectral noise density	vs Frequency	11
Output impedance	vs Frequency	12
Dropout voltage	vs Free-air temperature	13, 14
Line transient response		15, 17
Load transient response		16, 18
Output voltage	vs Time	19
Dropout voltage	vs Input voltage	20
Equivalent series resistance (ESR) <sup>(1)</sup>	vs Output current	21 through 24
Equivalent series resistance (ESR) <sup>(1)</sup>	vs Added ceramic capacitance	25, 26

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

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**TPS76533**  
**GROUND CURRENT**  
**vs**  
**LOAD CURRENT**

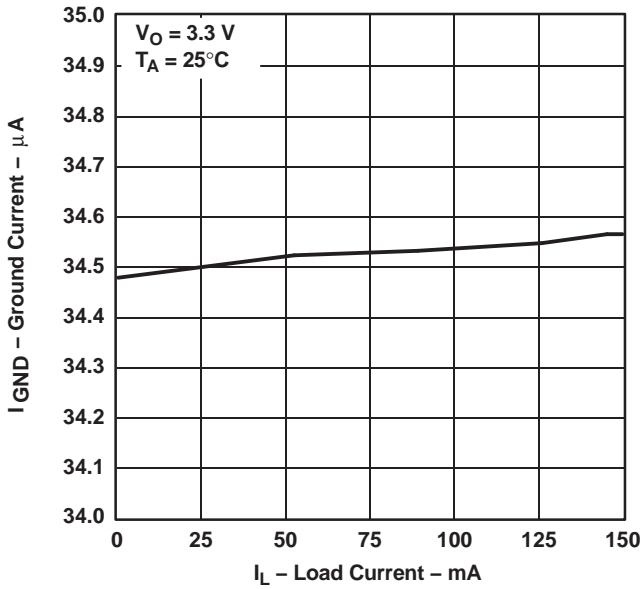


Figure 6.

**TPS76533**  
**GROUND CURRENT**  
**vs**  
**FREE-AIR TEMPERATURE**

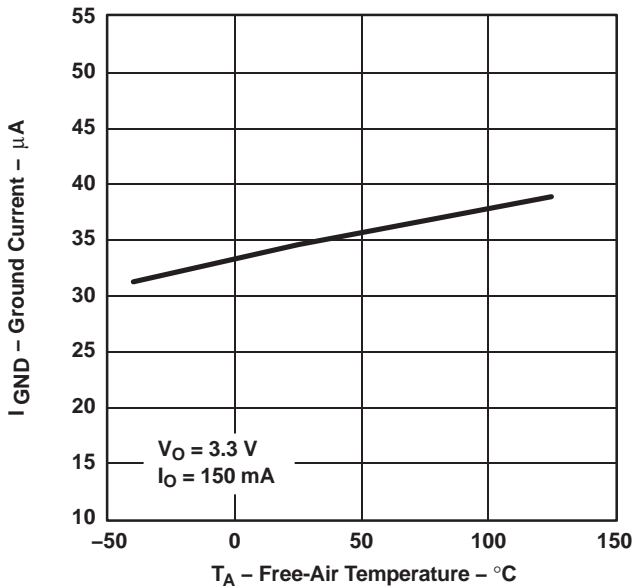


Figure 8.

**TPS76515**  
**GROUND CURRENT**  
**vs**  
**LOAD CURRENT**

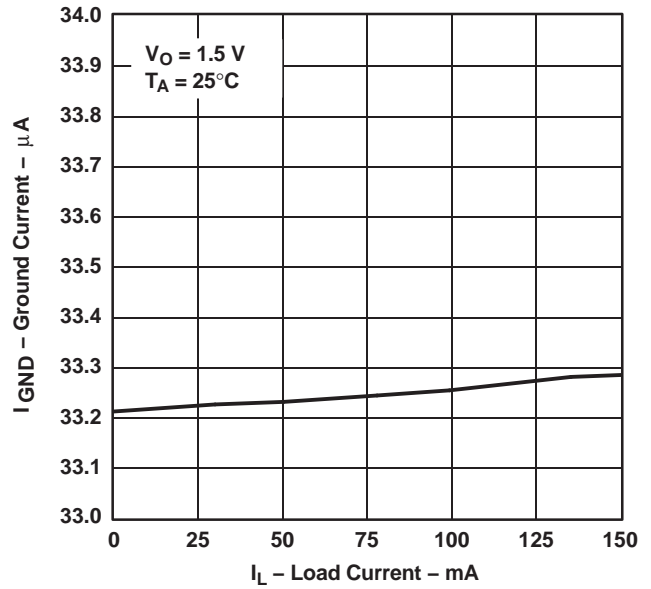


Figure 7.

**TPS76515**  
**GROUND CURRENT**  
**vs**  
**FREE-AIR TEMPERATURE**

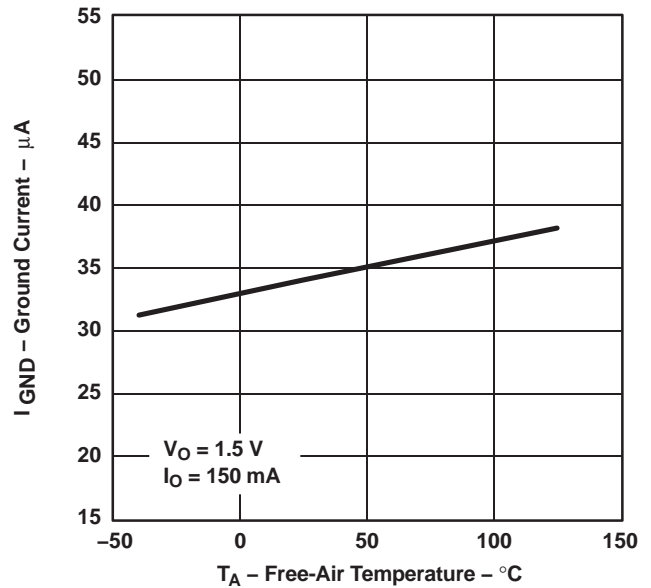
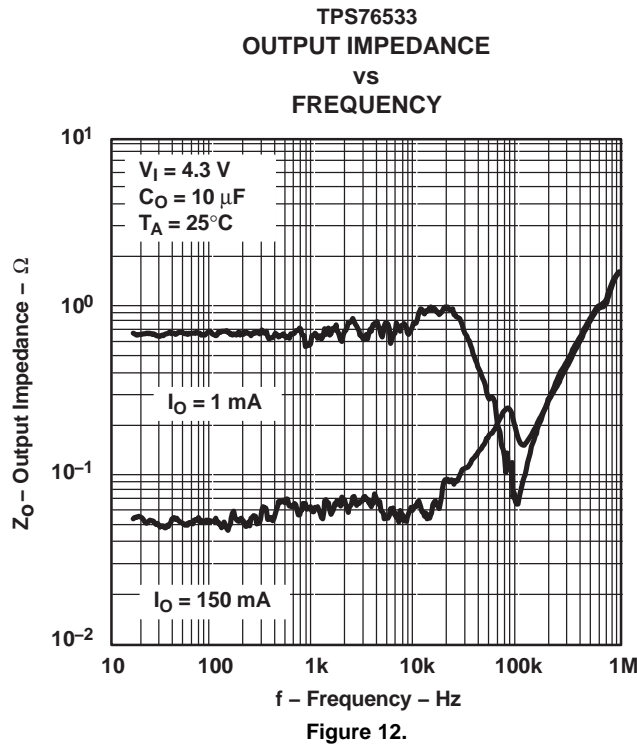
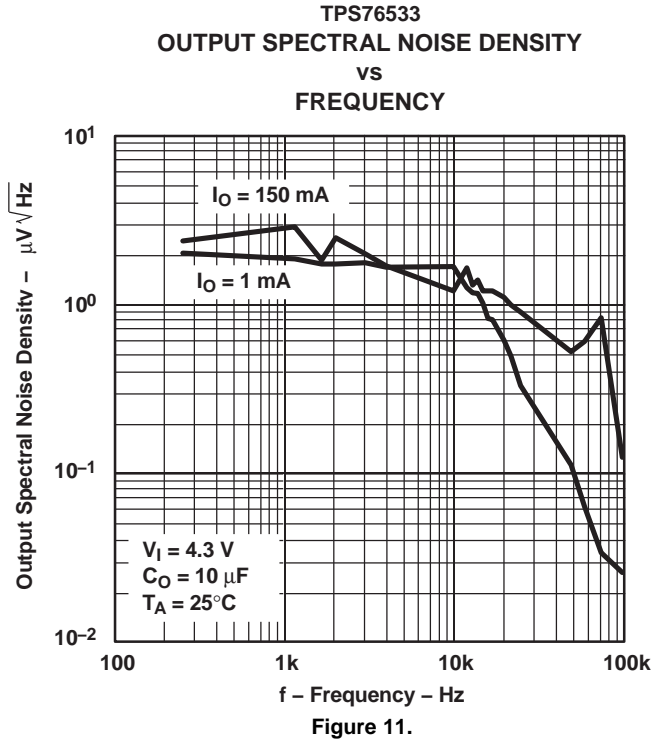
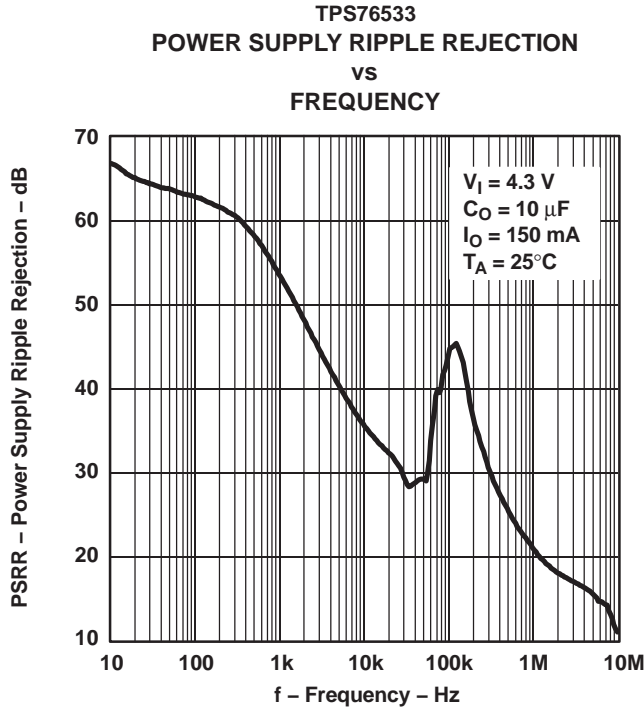


Figure 9.

**TPS76501-Q1**  
**ULTRALOW QUIESCENT CURRENT 150-mA LOW-DROPOUT**  
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**TPS76550**  
**DROPOUT VOLTAGE**  
**vs**  
**FREE-AIR TEMPERATURE**

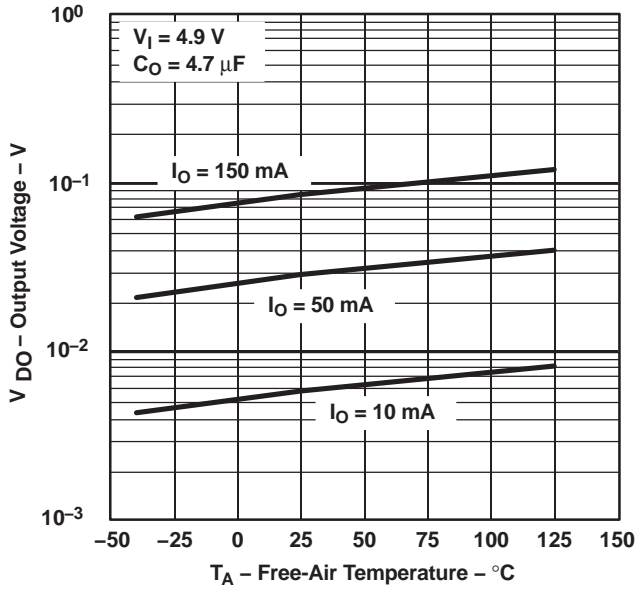


Figure 13.

TPS76515

**TPS76533**  
**DROPOUT VOLTAGE**  
**vs**  
**FREE-AIR TEMPERATURE**

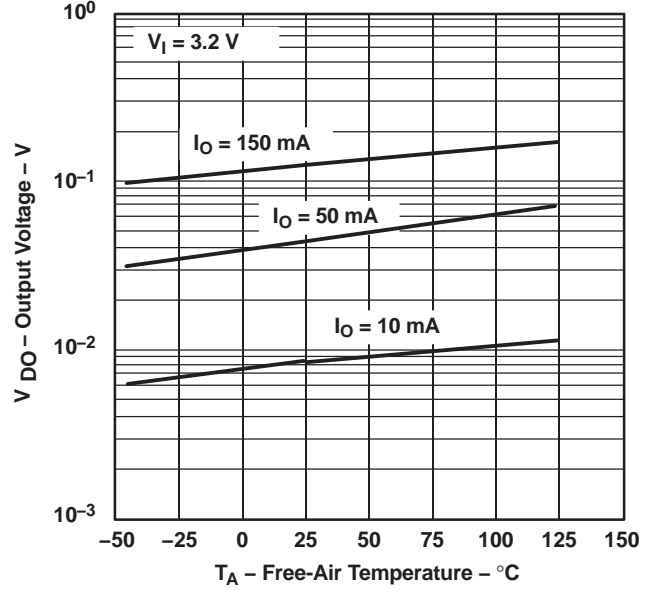


Figure 14.

TPS76515

**LINE TRANSIENT RESPONSE**

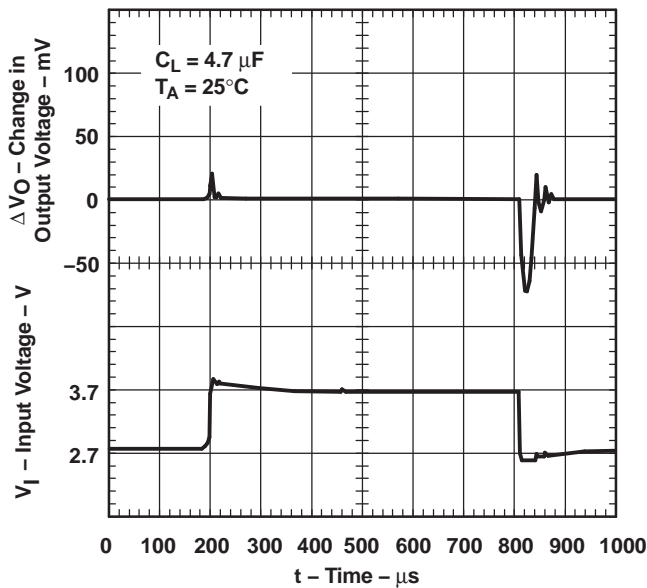


Figure 15.

**LOAD TRANSIENT RESPONSE**

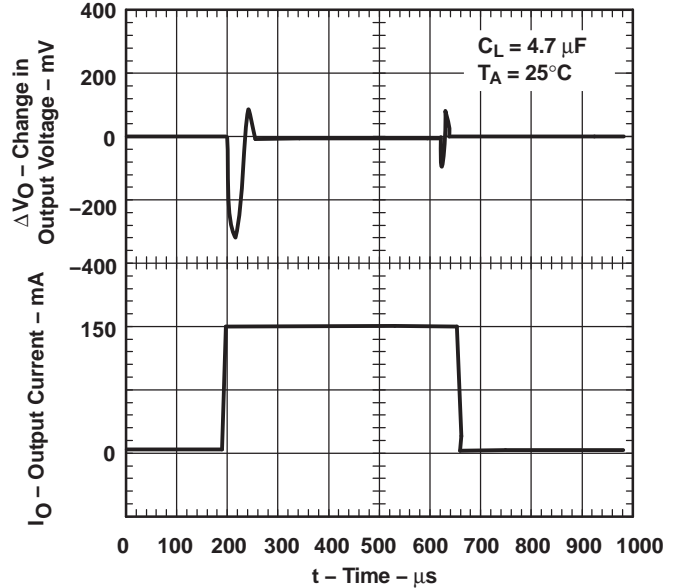


Figure 16.

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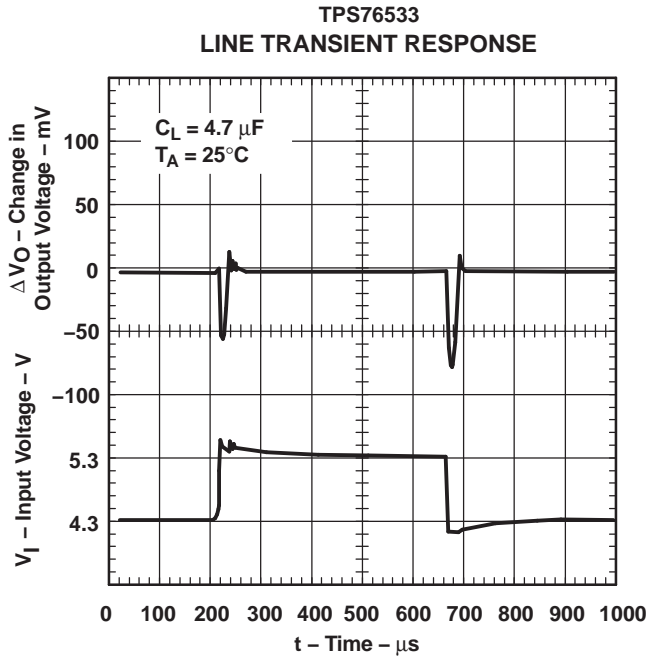


Figure 17.

TPS76533

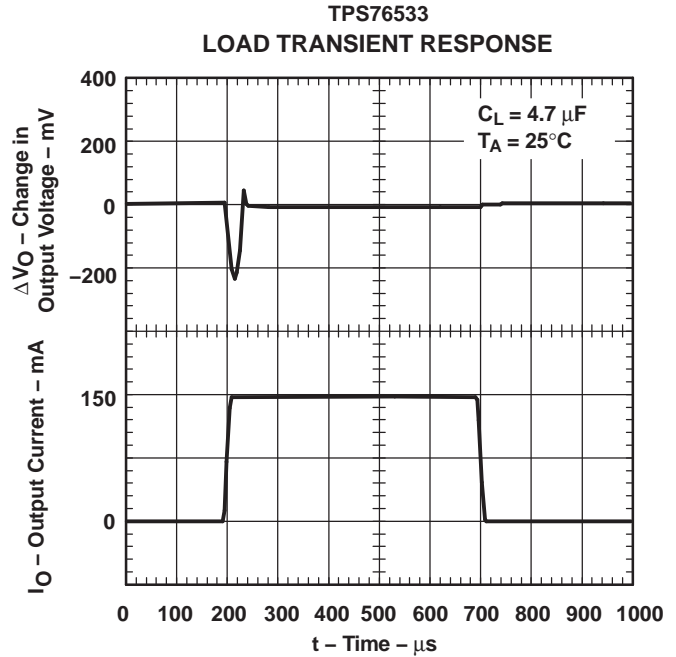


Figure 18.

TPS76501

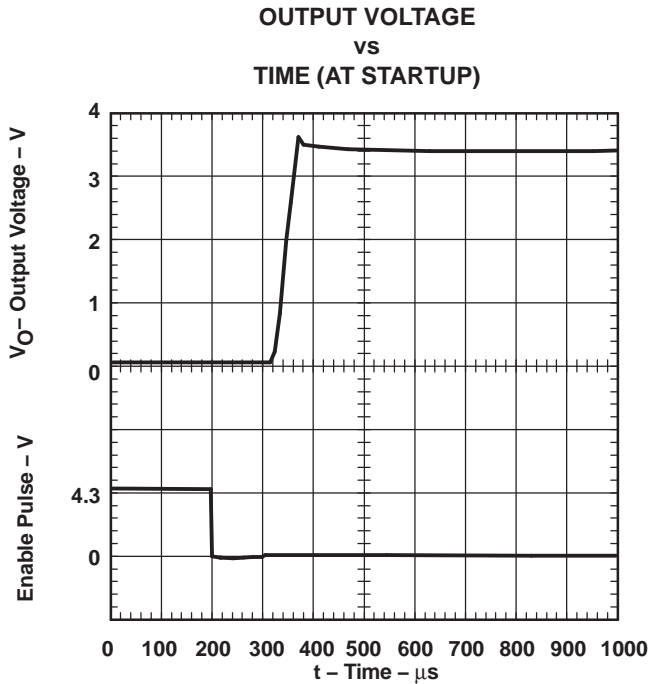


Figure 19.

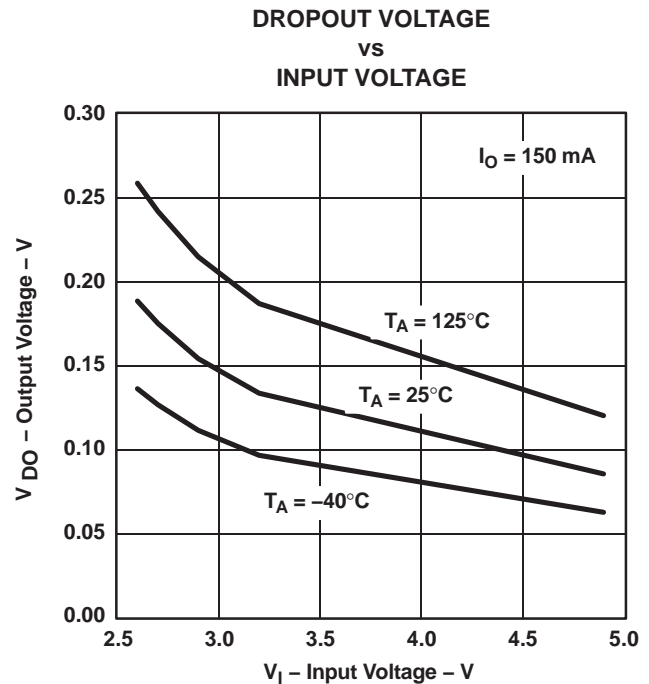


Figure 20.

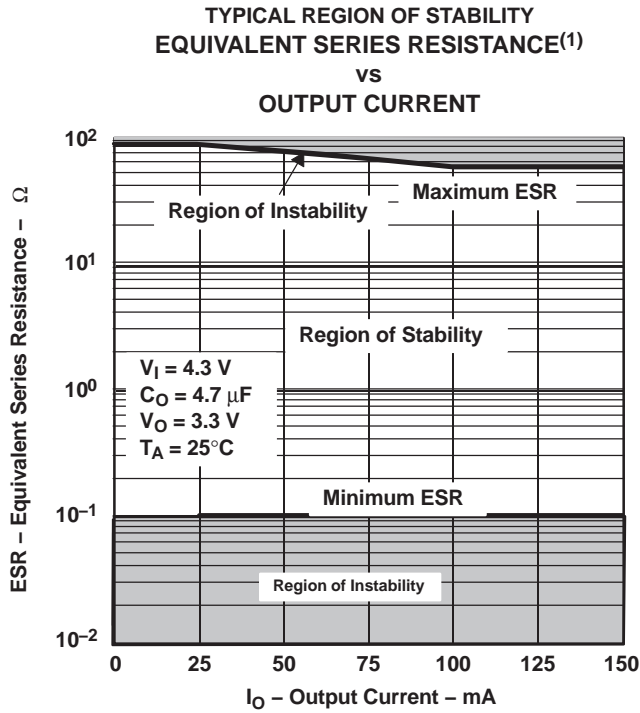


Figure 21.

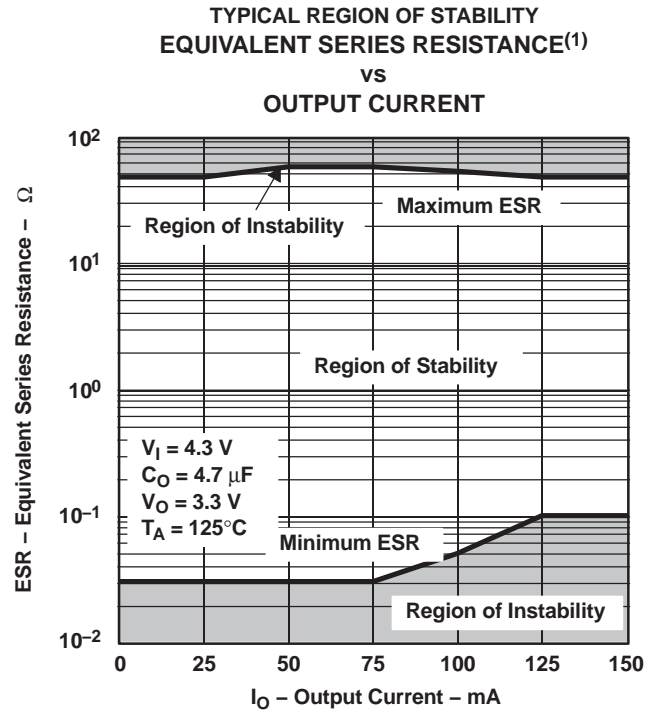


Figure 22.

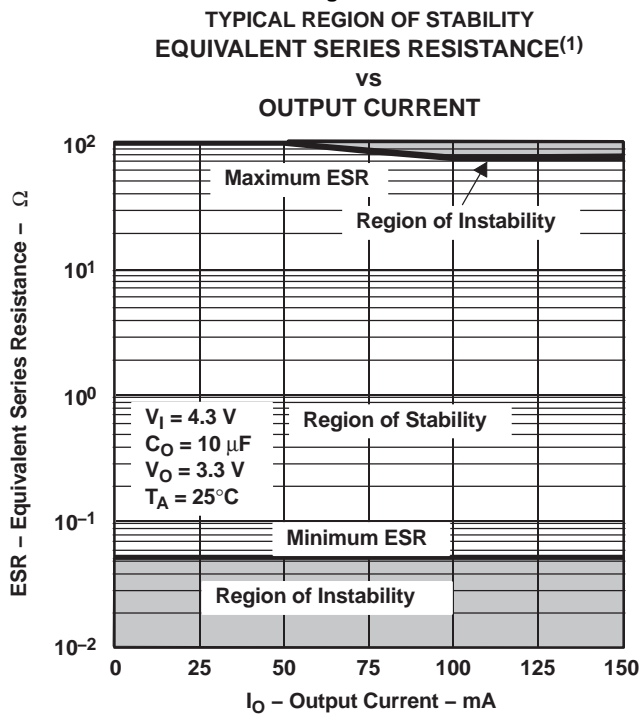


Figure 23.

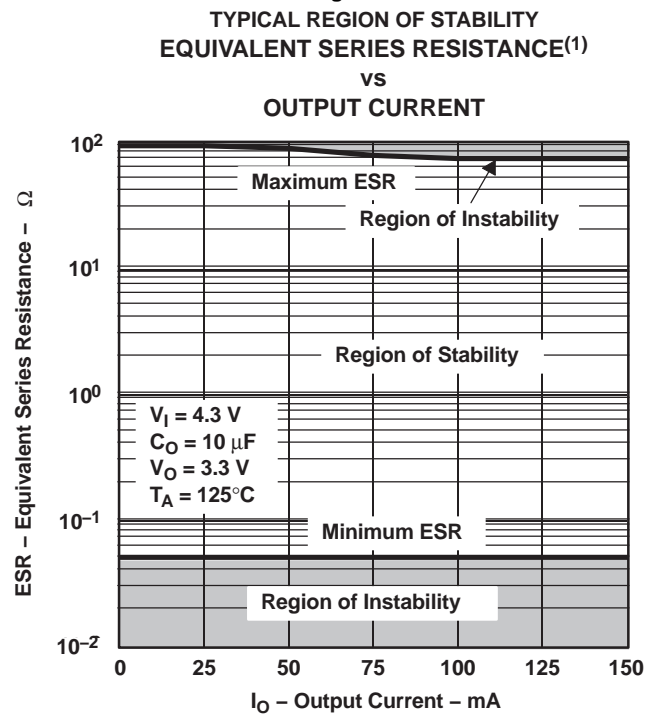
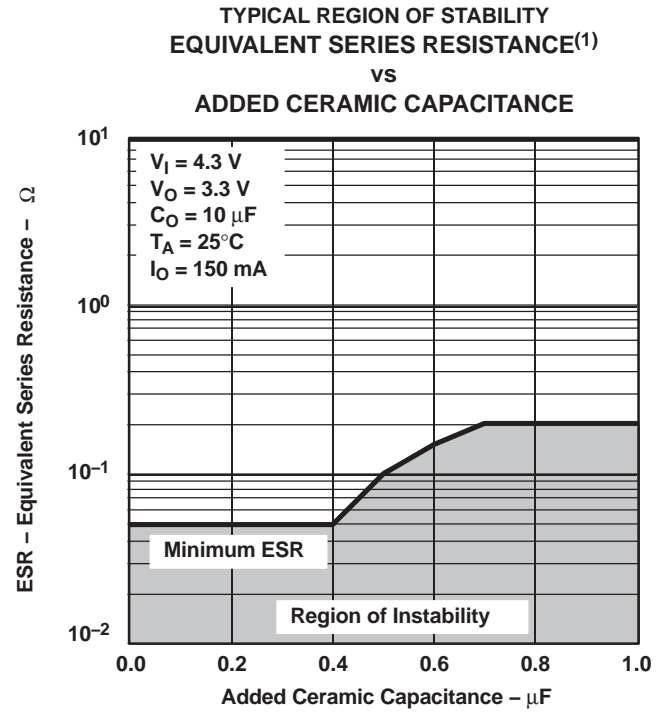
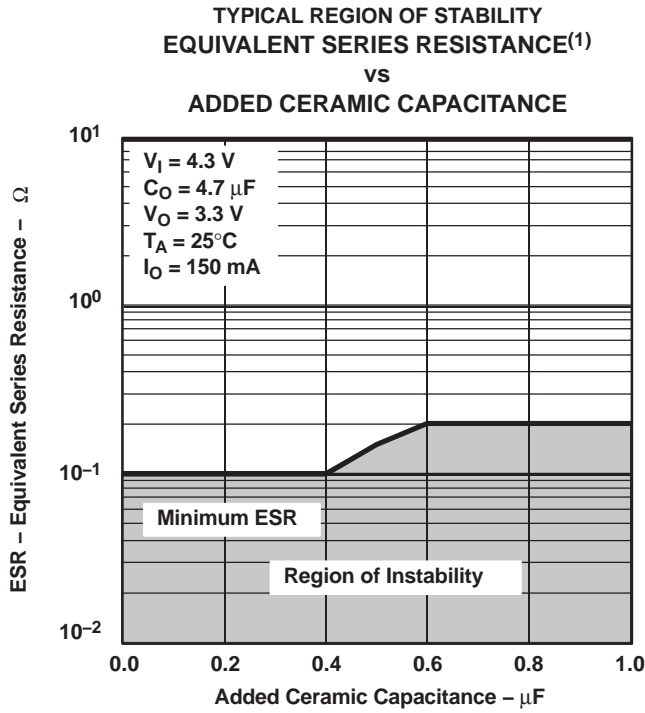


Figure 24.

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

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(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

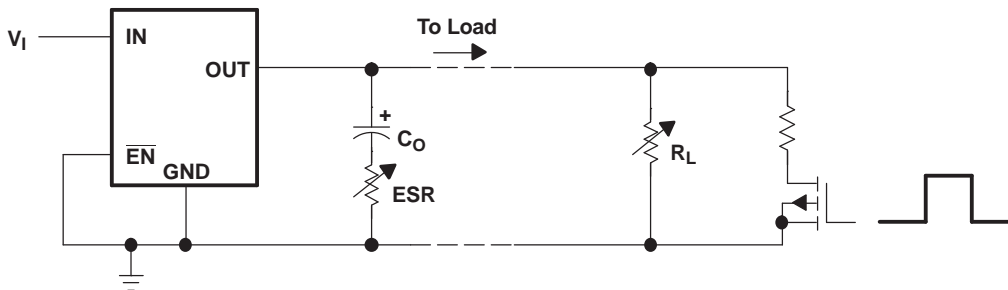


Figure 27. Test Circuit for Typical Regions of Stability (Figure 21 through Figure 24)  
(Fixed-Output Options)

## APPLICATION INFORMATION

The TPS765xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3 V, 3.3 V, and 5 V), and an adjustable regulator, the TPS76501 (adjustable from 1.25 V to 5.5 V).

### Device Operation

The TPS765xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ( $I_B = I_C/\beta$ ). The TPS765xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in  $\beta$  forces an increase in  $I_B$  to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS765xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS765xx also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 1  $\mu$ A (typ). If the shutdown feature is not used,  $\overline{EN}$  should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 160  $\mu$ s.

### Minimum Load Requirements

The TPS765xx is stable even at zero load; no minimum load is required for operation.

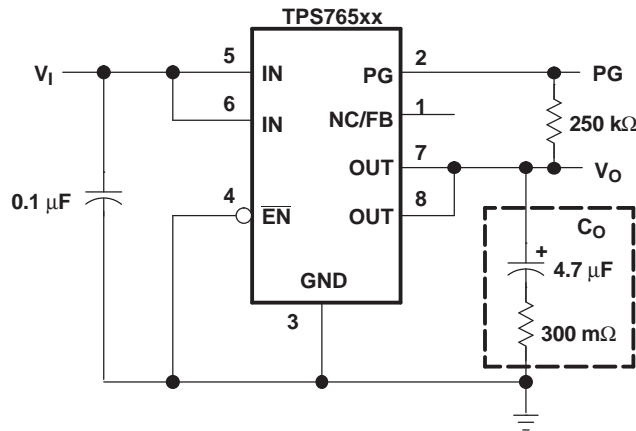
### FB Pin Connection

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable voltage. The output voltage is sensed through a resistor divider network to close the loop as it is shown in [Figure 29](#). Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

### External Capacitor Requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047  $\mu$ F or larger) improves load transient response and noise rejection if the TPS765xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all LDO regulators, the TPS765xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 4.7  $\mu$ F and the ESR must be between 300 m $\Omega$  and 20  $\Omega$ . Capacitor values 4.7  $\mu$ F or larger are acceptable, provided the ESR is less than 20  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.



**Figure 28. Typical Application Circuit (Fixed Versions)**

**Programming the TPS76501 Adjustable LDO Regulator**

The output voltage of the TPS76501 adjustable regulator is programmed using an external resistor divider as shown in Figure 29. The output voltage is calculated using Equation 1:

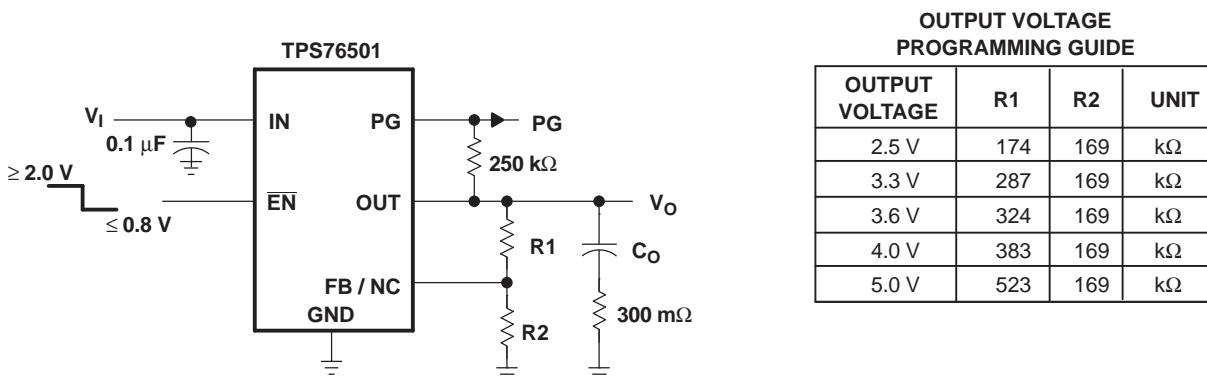
$$V_O = V_{ref} \times \left( 1 + \frac{R1}{R2} \right) \tag{1}$$

Where

$$V_{ref} = 1.224 \text{ V (typ) (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. Lower-value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 μA and then calculate R1 using Equation 2:

$$R1 = \left( \frac{V_O}{V_{ref}} - 1 \right) \times R2 \tag{2}$$



**Figure 29. TPS76501 Adjustable LDO Regulator Programming**

## Power-Good Indicator (PG)

The TPS765xx features a power-good output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

## Regulator Protection

The TPS765xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS765xx also features internal current limiting and thermal protection. During normal operation, the TPS765xx limits output current to approximately 0.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typical), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typical), regulator operation resumes.

## Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

$T_{Jmax}$  is the maximum allowable junction temperature.

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76501QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	76501Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS76501-Q1 :**

- Catalog: [TPS76501](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76501QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

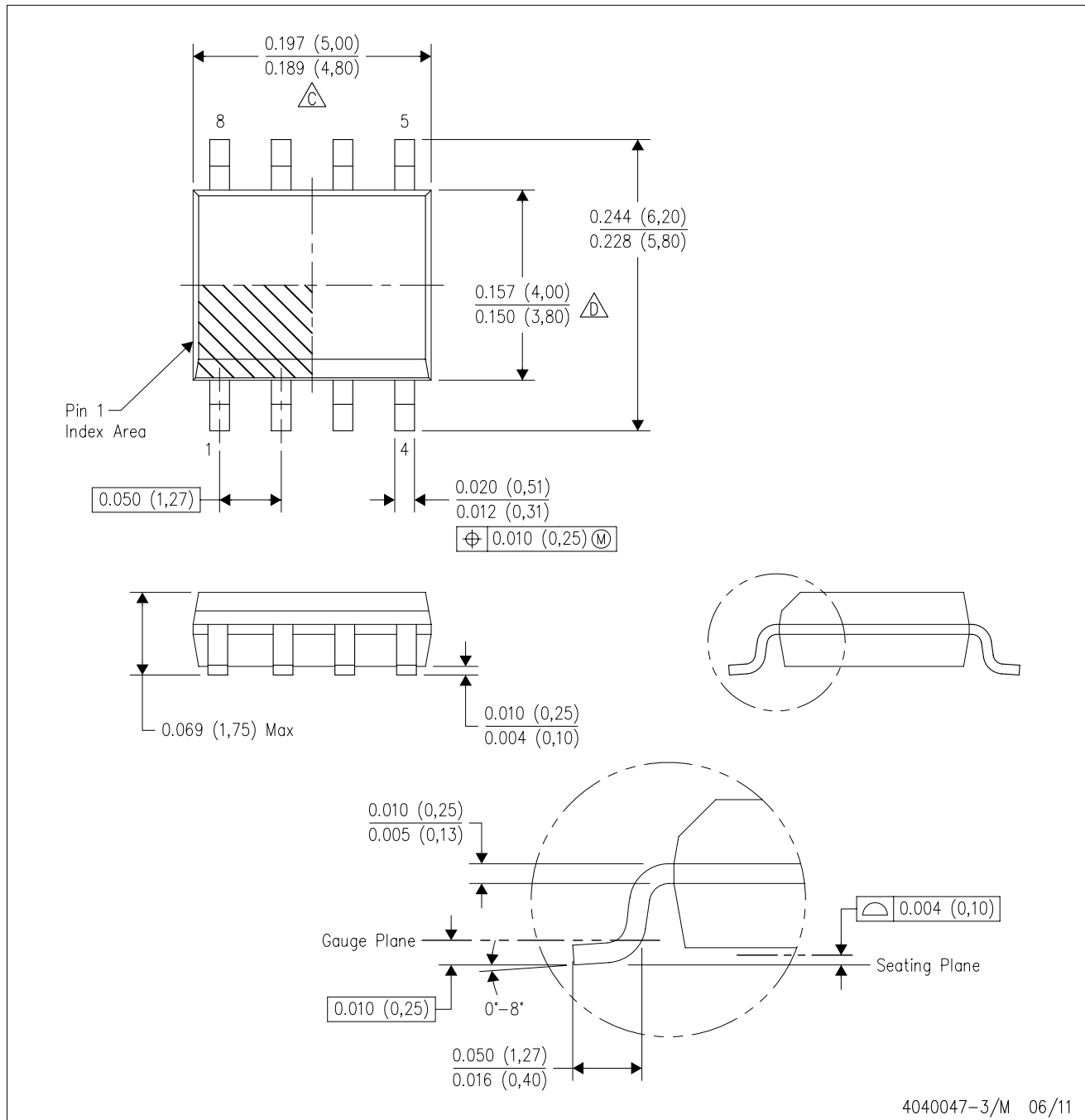


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76501QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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