TPS7A7001 Very Low Input, Very Low Dropout, 2-Amp Regulator With Enable

1 Features

- Input Voltage as low as 1.425 V
- 380 mV Dropout Maximum at 2 A
- Adjustable Output from 0.5 V
- Protections: Current Limit and Thermal Shutdown
- Enable Pin
- 1-µA Quiescent Current in Shutdown Mode
- Full Industrial Temperature Range
- Available in SO-8, Fully RoHS-Compliant Package

2 Applications

- Telecom and Networking Cards
- Motherboards and Peripheral Cards
- Industrial
- Wireless Infrastructure
- Set-Top Boxes
- Medical Equipment
- Notebook Computers
- Battery-Powered Systems

3 Description

The TPS7A7001 is a high-performance, positive-voltage, low-dropout (LDO) regulator designed for applications requiring very low input voltage and very low dropout voltage at up to 2 A. The device operates with a single input voltage as low as 1.425 V, and with an output voltage programmable to as low as 0.5 V. The output voltage can be set with an external resister divider.

The TPS7A7001 features ultra-low dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, the TPS7A7001 has an enable pin for further reduced power dissipation while in Shutdown mode. The TPS7A7001 provides excellent regulation over variations in line, load, and temperature.

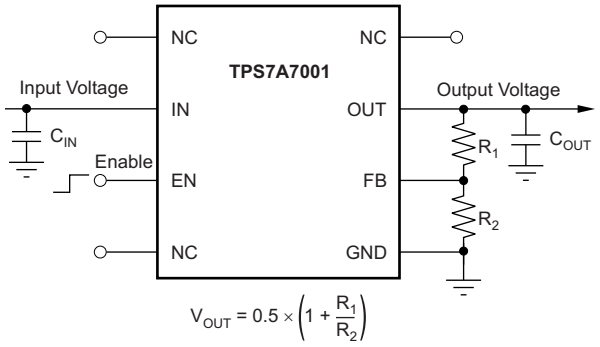
The TPS7A7001 is available in an SO-8 PowerPAD™ package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A7001	SO PowerPAD (8)	3.90 mm × 4.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2013) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision C (January 2013) to Revision D — **Page**

- Added new text to *Internal Current Limit* section ... 7

Changes from Revision B (July 2012) to Revision C — **Page**

- Deleted maximum value for Output Current Limit parameter in Electrical Characteristics table ... 5

Changes from Revision A (June 2012) to Revision B — **Page**

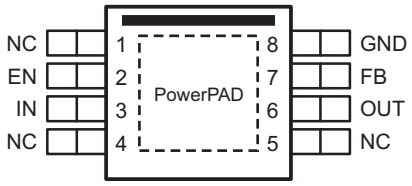
- Changed Output Voltage, I_{LIM} parameter test conditions in Electrical Characteristics table ... 5

Changes from Original (January 2012) to Revision A — **Page**

- Changed *Adjustable Output* feature bullet ... 1
- Changed output voltage minimum value in first paragraph of *Description* section ... 1
- Changed Electrical Characteristics condition line ... 5
- Changed *Output Voltage Accuracy* parameter in Electrical Characteristics ... 5
- Changed test conditions for *Dropout Voltage* parameter in Electrical Characteristics ... 5
- Changed note 1 in Electrical Characteristics ... 5
- Added new note 4 to Electrical Characteristics ... 5

5 Pin Configuration and Functions

DDA Package
SO-8
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable input. Pulling this pin below 0.5 V turns the regulator off. Connect to V_{IN} if not being used.
FB	7	I	This pin is the output voltage feedback input through voltage dividers. See the recommended feedback resistor table for more details.
GND	8	–	Ground pin
IN	3	I	Unregulated supply voltage pin. It is recommended to connect an input capacitor to this pin.
NC	1, 4, 5	–	Not internally connected. The NC pins are not connected to any electrical node. It is recommended to connect the NC pins to large-area planes.
OUT	6	O	Regulated output pin. A 4.7-µF or larger capacitor of any type is required for stability.
PowerPAD			TI strongly recommends connecting the thermal pad to a large-area ground plane. If an electrically floating, dedicated thermal plane is available, the thermal pad can also be connected to it.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	IN, OUT	–0.3	7	V
	EN, FB	–0.3	V_{IN} + 0.3(2)	V
Current	OUT		Internally limited	A
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or +7.0 V, whichever is smaller.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.425		6.5	V
V_{EN}	Enable pin voltage	0		V_{IN}	V
C_{IN}	Input capacitor	1		10	µF
C_{OUT}	Output capacitor(1)	4.7	10	47	µF
I_{OUT}	Output current	0		2	A
T_A	Ambient temperature range	–40		105	°C
T_J	Junction temperature range	–40		125	°C

(1) See Figure 1 and Figure 2 for additional output capacitor requirements.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A7001 SO PowerPAD 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (4)	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter (6)	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(7)	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Over the full operating temperature range (see *Recommended Operating Conditions*), V_{EN} = 1.1 V, $V_{FB} = V_{OUT}$(1), 1.425 V ≤ V_{IN} ≤ 6.5 V, 10 µA ≤ I_{OUT} ≤ 2 A, C_{OUT} = 10 µF, unless otherwise noted. Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
I_{GND}	GND pin current (small)	V_{IN} = 3.3 V, 50-Ω load resistor between OUT and GND			3	mA
	GND pin current (shutdown)	V_{IN} = 6.5 V, V_{EN} = 0 V			5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage accuracy(2)(3)	$V_{IN} = V_{OUT}$ + 0.5 V(4), I_{OUT} = 10 mA	–2%		2%	
		V_{IN} = 1.8 V, I_{OUT} = 0.8 A, 0°C ≤ $T_J = T_A$ ≤ +85°C	–2%		2%	
		I_{OUT} = 10 mA	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 10 mA		0.2	0.4	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation(3)	10 mA ≤ I_{OUT} ≤ 2 A		0.25	0.75	%/A
V_{DO}	Dropout voltage (5)	I_{OUT} = 1.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			200	mV
		I_{OUT} = 1.5 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			300	
		I_{OUT} = 2.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			380	
I_{LIM}	Output current limit	V_{IN} = 1.425 V, V_{OUT} = 0.9 × $V_{OUT(NOM)}$	2.1			A
FEEDBACK						
V_{REF}	Reference voltage accuracy	V_{IN} = 3.3 V, $V_{FB} = V_{OUT}$, I_{OUT} = 10 mA	0.490	0.500	0.510	V
I_{FB}	FB pin current	V_{FB} = 0.5 V			1	µA
ENABLE						
I_{EN}	EN pin current	V_{EN} = 0 V, V_{IN} = 3.3 V			0.2	µA
VIL_{EN}	EN pin input low (disable)	V_{IN} = 3.3 V	0		0.5	V
VIH_{EN}	EN pin input high (enable)	V_{IN} = 3.3 V	1.1		V_{IN}	V
TEMPERATURE						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		°C

(1) When setting V_{OUT} to a value other than 0.5 V, connect R_1 and R_2 to the FB pin using 10 kΩ ≤ R_2 ≤ 50 kΩ resistors. See Functional Block Diagram for details of R_1 and R_2.
(2) Accuracy does not include error on feedback resistors R_1 and R_2.
(3) TPS7A7001 is not tested at V_{OUT} = 0.5 V, 2.3 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 2 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply to any application condition that exceeds the power dissipation limit of the package.
(4) $V_{IN} = V_{OUT}$ + 0.5 V or 1.425 V, whichever is greater.
(5) $V_{DO} = V_{IN} - V_{OUT}$ with V_{FB} = GND configuration.

6.6 Typical Characteristics

For all fixed voltage versions and an adjustable version at T_J = +25°C, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, and using the component values in Table 2, unless otherwise noted.

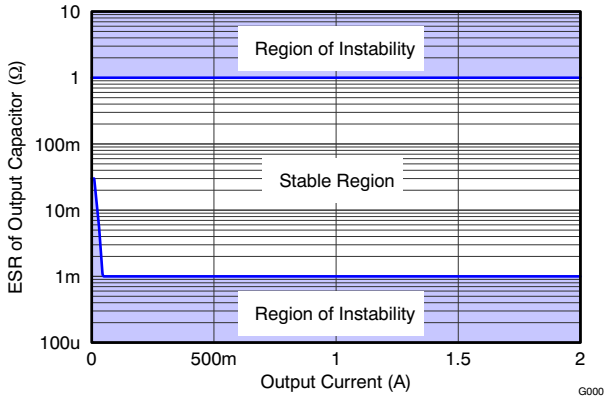


Figure 1. Stability Curve (C_{OUT} = 10 µF)

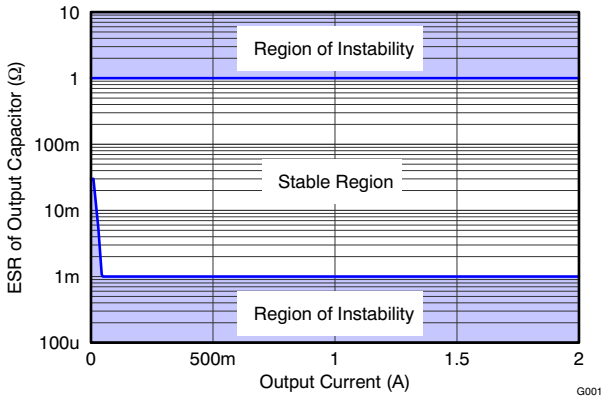


Figure 2. Stability Curve (C_{OUT} = 100 µF)

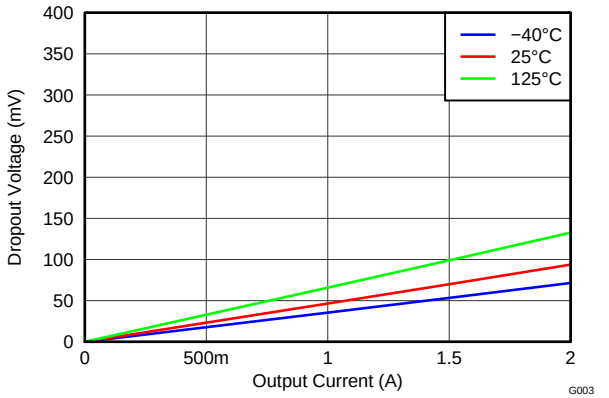


Figure 3. Dropout Voltage vs Output Current (V_{OUT} = 3.3 V)

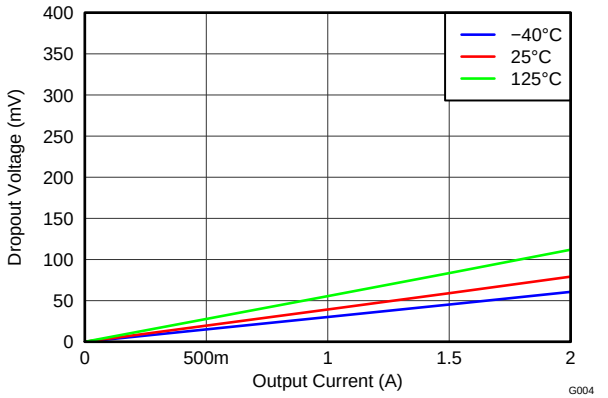


Figure 4. Dropout Voltage vs Output Current (V_{OUT} = 1.6 V)

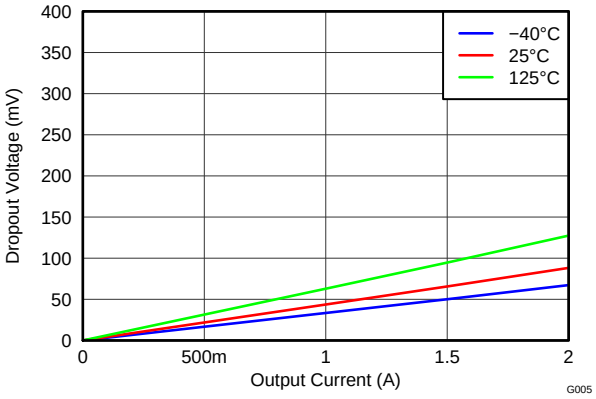


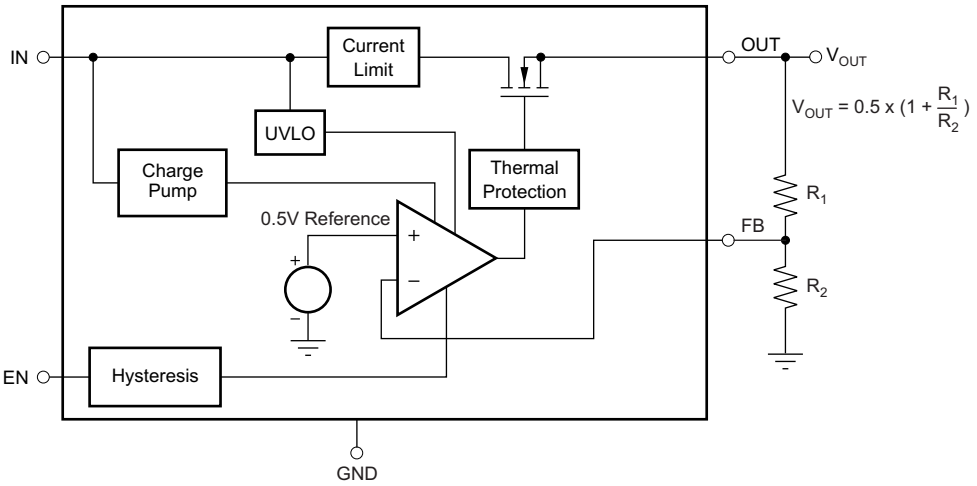
Figure 5. Dropout Voltage vs Output Current (V_{OUT} = 1.4 V)

7 Detailed Description

7.1 Overview

The TPS7A7001 offers a high current supply with very low dropout voltage. The TPS7A7001 is designed to minimize the required component count for a simple, small-size, and low-cost solution.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable pin (EN) is an active high logic input. When it is logic low, the device turns off and its consumption current is less than 1 µA. When it is logic high, the device turns on. The EN pin is required to be connected to a logic high or logic low level.

When the enable function is not required, connect EN to VIN.

7.3.2 Internal Current Limit

The TPS7A7001 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Capacitor (IN)

Although an input capacitor is not required for stability, it is recommended to connect a 1-µF to 10-µF low equivalent series resistance (ESR) capacitor across IN and GND near the device.

8.1.2 Output Capacitor (OUT)

The device is designed to be stable with output capacitance 4.7 µF or larger. For a good load transient response, a 10-µF to 47-µF ceramic capacitor is recommended. Connect the output capacitor across OUT and GND near the device.

8.1.3 Feedback Resistors (FB)

The voltage on the FB pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 1:

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Table 2 shows the recommended resistor values for the best performance of the TPS7A7001. If the values in Table 2 are not used, keep the value of R2 between 27 kΩ and 33 kΩ. In Table 2, E96 series resistors are used. For the actual design, pay attention to any resistor error factors.

Table 2. Sample Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.0 V	30.1 kΩ	30.1 kΩ
1.2 V	42.2 kΩ	30.1 kΩ
1.5 V	60.4 kΩ	30.1 kΩ
1.8 V	78.7 kΩ	30.1 kΩ
2.5 V	121 kΩ	30.1 kΩ
3.0 V	150 kΩ	30.1 kΩ
3.3 V	169 kΩ	30.1 kΩ
5.0 V	274 kΩ	30.1 kΩ

8.2 Typical Application

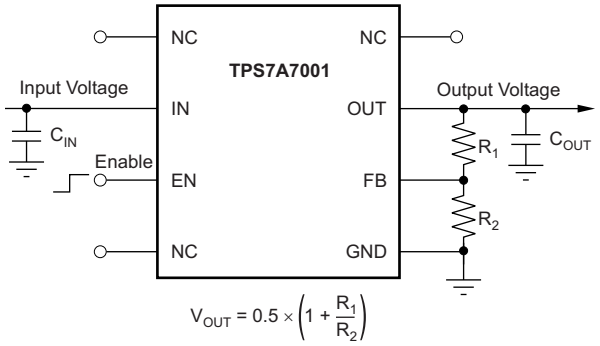


Figure 6. Typical Application

8.2.1 Design Requirements

Table 3 lists the design parameters.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	2.5 V
Maximum output current	1.2 A

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.3 Application Curve

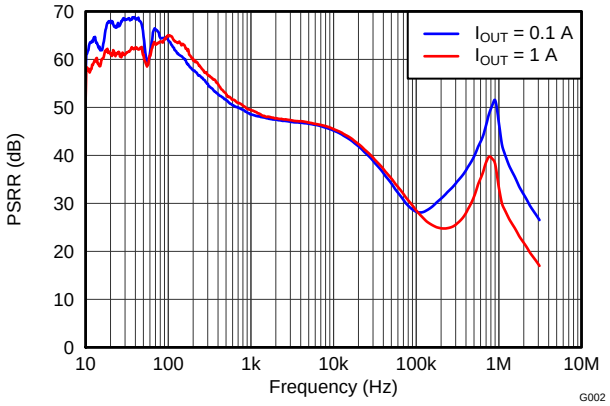


Figure 7. Power-Supply Ripple Rejection vs Frequency (V_{IN} = 5.0 V, V_{OUT} = 3.3 V)

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.425 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, it is recommended that the board be designed as shown in the below layout example.

10.2 Layout Example

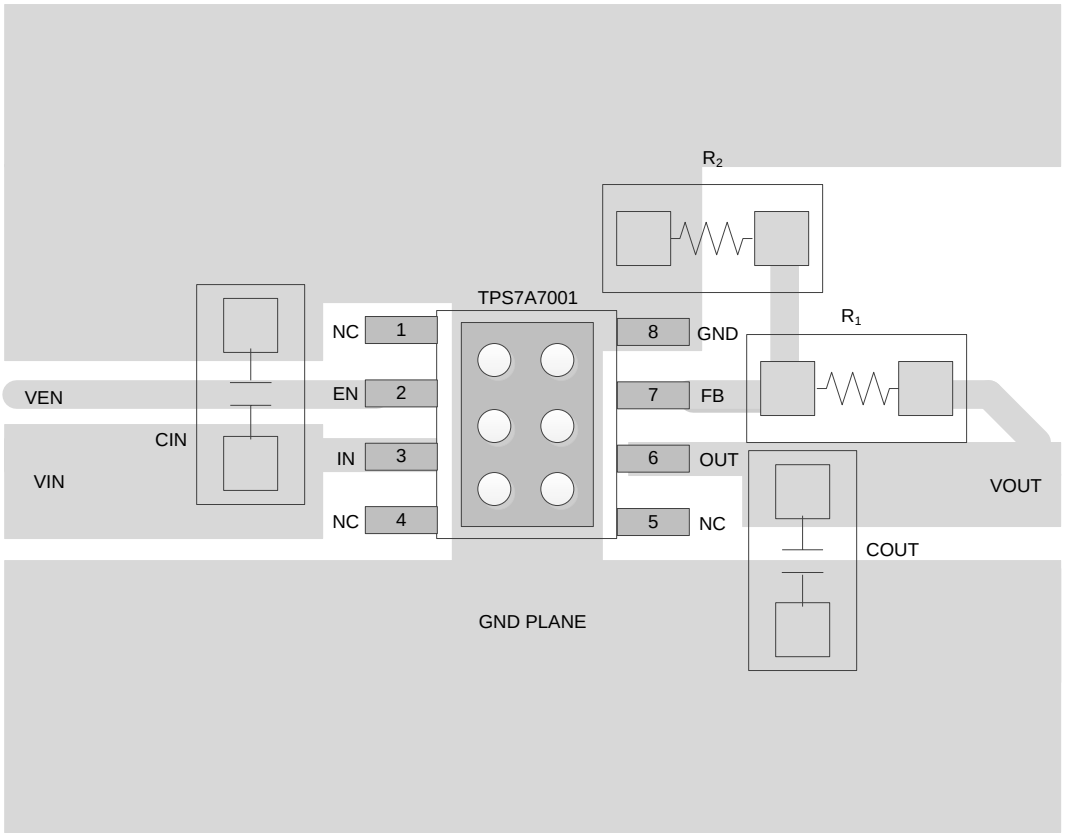


Figure 8. Layout Example

10.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled again.

The internal protection circuitry of the TPS7A7001 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS7A7001 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Power dissipation of the device depends on the input voltage and load conditions and can be calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SO (DDA) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 3:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \quad (3)$$

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A7001DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH	Samples
TPS7A7001DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

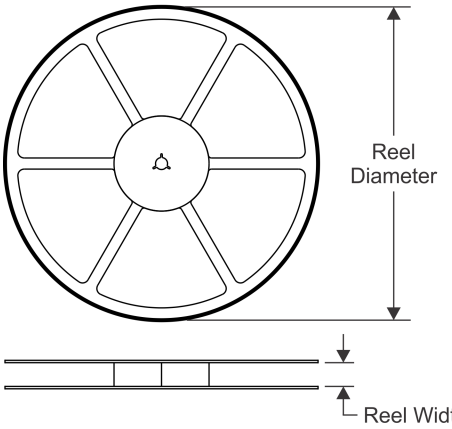
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

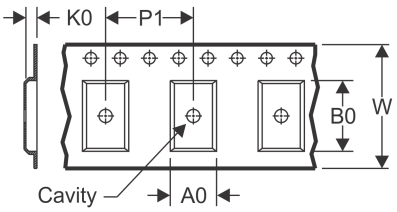
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

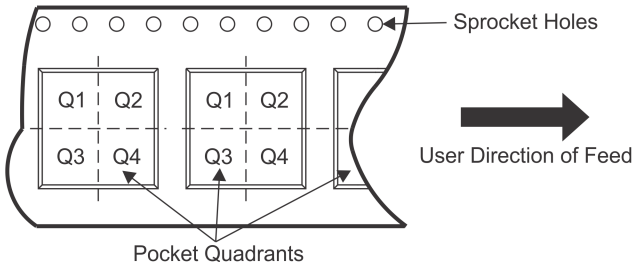


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

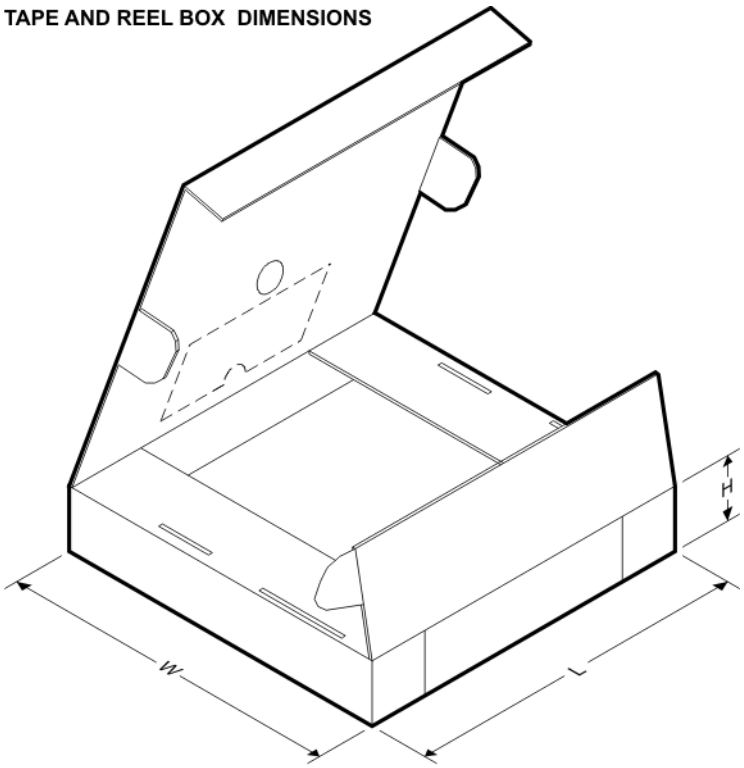
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7001DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

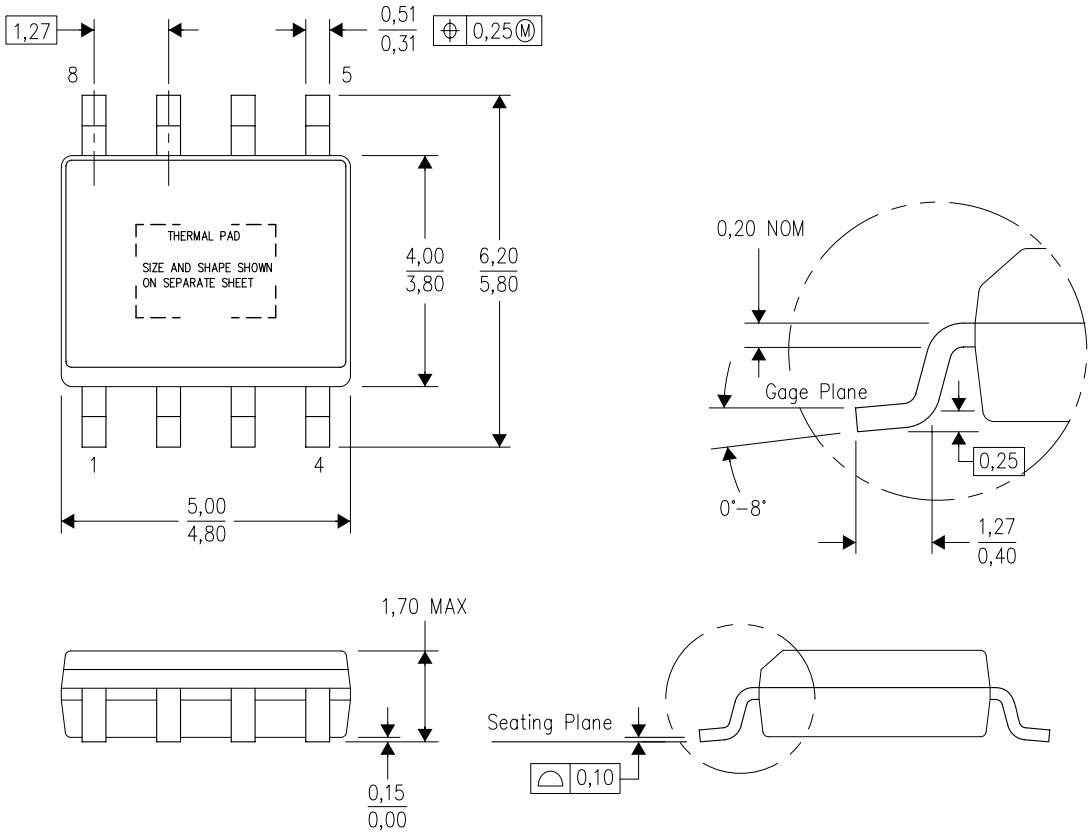
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7001DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

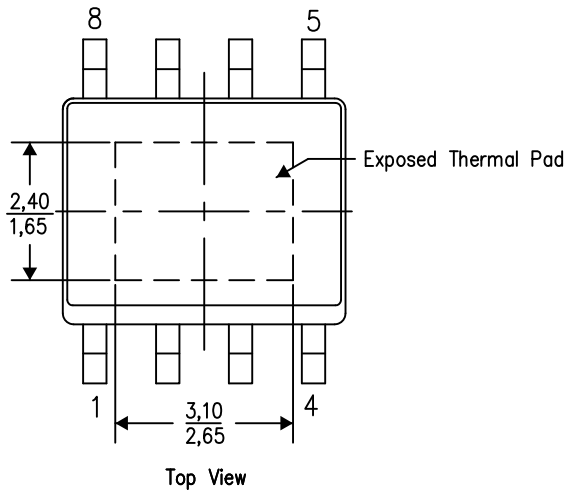
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



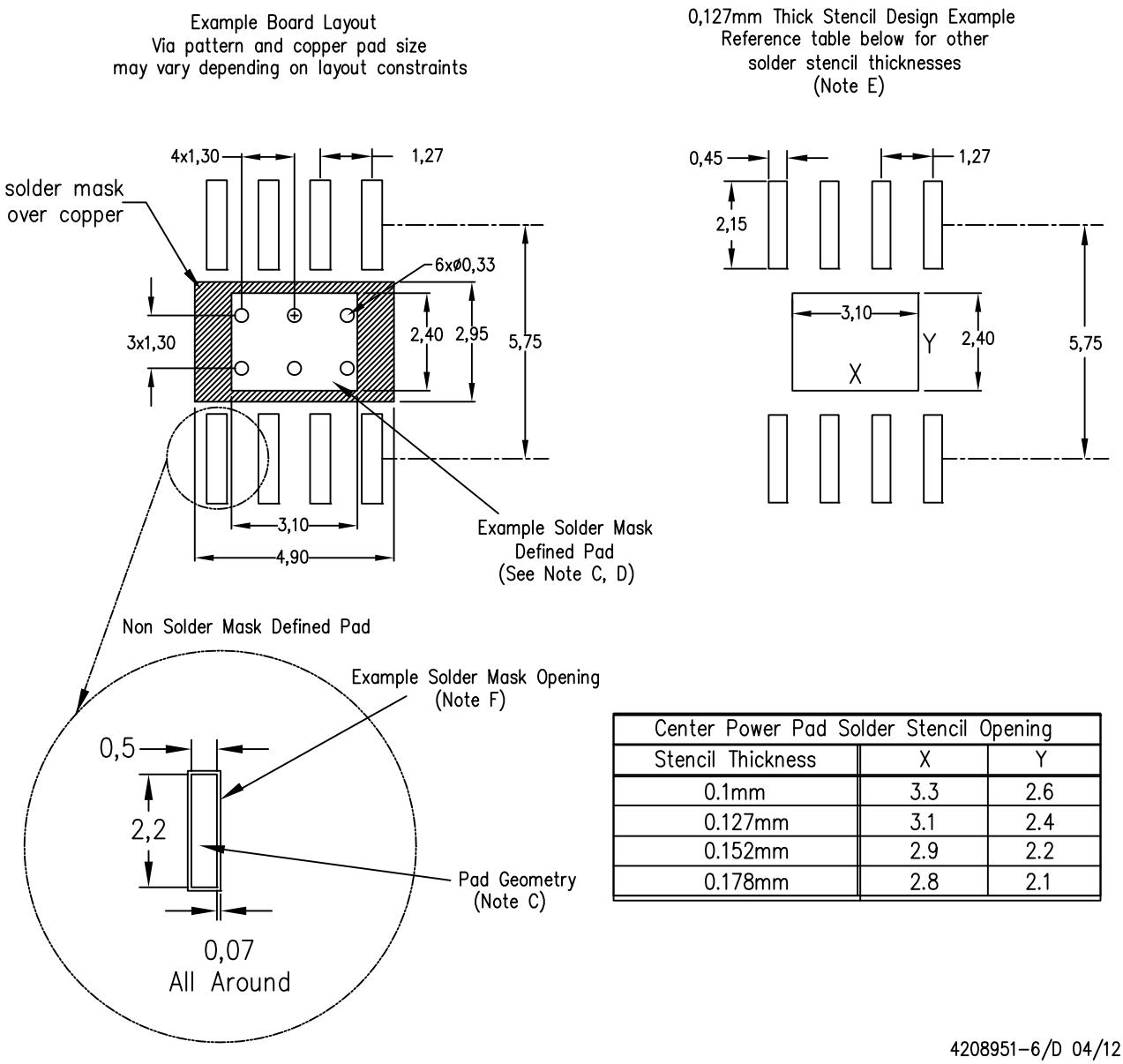
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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