

FEATURES

- ESD Protection for RS-232 Pins
 - ±15-kV Human-Body Model (HBM)
 - ±8-kV IEC 61000-4-2 Contact Discharge
 - ±15-kV IEC 61000-4-2 Air-Gap Discharge
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 1 Mbit/s
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using HBM
- Auto-Powerdown Feature Automatically Disables Drivers for Power Savings

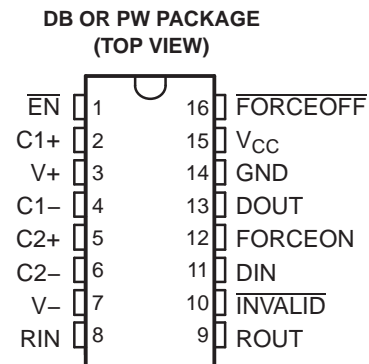
APPLICATIONS

- Battery-Powered, Hand-Held, and Portable Equipment
- PDAs and Palmtop PCs
- Notebooks, Sub-Notebooks, and Laptops
- Digital Cameras
- Mobile Phones and Wireless Devices

DESCRIPTION/ORDERING INFORMATION

The TRSF3221E consists of one line driver, one line receiver, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The TRSF3221E provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3221E operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ μ s to 150 V/ μ s.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the TRSF3221E does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If FORCEOFF is set low and the enable (\overline{EN}) input is high, both the driver and receiver are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The INVALID output notifies the user if an RS-232 signal is present at the receiver input. INVALID is high (valid data) if the receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30 μ s. See Figure 5 for receiver input levels.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TRSF3221E
3-V TO 5.5-V SINGLE-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER
WITH ±15-kV IEC ESD PROTECTION

SLLS822–JULY 2007

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SSOP – DB	Reel of 2000	TRSF3221ECDBR	RT21EC
	TSSOP – PW	Tube of 90	TRSF3221ECPW	RT21EC
		Reel of 2000	TRSF3221ECPWR	
–40°C to 85°C	SSOP – DB	Reel of 2000	TRSF3221EIDBR	RT21EI
	TSSOP – PW	Tube of 90	TRSF3221EIPW	RT21EI
		Reel of 2000	TRSF3221EIPWR	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

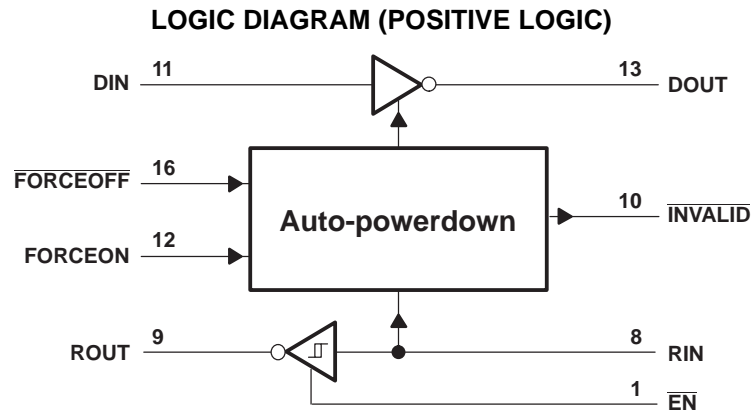
INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

- (1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver⁽¹⁾

INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

- (1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off



TRSF3221E
3-V TO 5.5-V SINGLE-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER
WITH ± 15 -kV IEC ESD PROTECTION

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Table 1. 1-Mbit/s RS-232 Parts

PART NO.	TEMPERATURE RANGE	DRIVER NO.	RECEIVER NO.	ESD	SUPPLY V_{CC} (V)	FEATURE	PIN/PACKAGE
TRSF3221E	0°C to 70°C	1	1	± 15 -kV Air-Gap, ± 8 -kV Contact, ± 15 -kV HBM	3.3 or 5	Auto-powerdown	16-pin SOIC, SSOP, TSSOP
TRSF3232E		2	2	± 15 -kV Air-Gap, ± 8 -kV Contact, ± 15 -kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
TRS3227		1	1	± 8 -kV Air-Gap, ± 8 -kV Contact, ± 15 -kV HBM	3.3 or 5	Auto-powerdown plus, ready signal	16-pin SSOP
TRSF3221		1	1	± 15 -kV HBM	3.3 or 5	Auto-powerdown	16-pin SOIC, SSOP, TSSOP
TRSF3223		2	2	± 15 -kV HBM	3.5 or 5	Auto-powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
TRSF3222		2	2	± 15 -kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
TRSF3232		2	2	± 15 -kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
TRSF3238		5	3	± 15 -kV HBM	3.3 or 5	Auto-powerdown plus	28-pin SOIC, SSOP, TSSOP
TRSF3243		3	5	± 15 -kV HBM	3.3 or 5	Auto-powerdown	28-pin SOIC, SSOP, TSSOP
TRSF3221E		–40°C to 85°C	1	1	± 15 -kV Air-Gap, ± 8 -kV Contact, ± 15 -kV HBM	3.3 or 5	Auto-powerdown
TRSF3232E	2		2	± 15 -kV Air-Gap, ± 8 -kV Contact, ± 15 -kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
TRS3227	1		1	± 8 -kV Air-Gap, ± 8 -k V Contact, ± 15 -kV HBM	3.3 or 5	Auto-powerdown plus, ready signal	16-pin SSOP
TRSF3221	1		1	± 15 -kV HBM	3.3 or 5	Auto-powerdown	16-pin SOIC, SSOP, TSSOP
TRSF3223	2		2	± 15 -kV HBM	3.3 or 5	Auto-powerdown, enable signal	20-pin SOIC, SSOP, TSSOP
TRSF3222	2		2	± 15 -kV HBM	3.3 or 5	Enable, powerdown signal	20-pin SOIC, SSOP, TSSOP
TRSF3232	2		2	± 15 -kV HBM	3.3 or 5	Low pin count	16-pin SOIC, SSOP, TSSOP
TRSF3238	5		3	± 15 -kV HBM	3.3 or 5	Auto-powerdown plus	28-pin SOIC, SSOP, TSSOP
TRSF3243	3		5	± 15 -kV HBM	3.3 or 5	Auto-powerdown	28-pin SOIC, SSOP, TSSOP

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	−0.3	6	V
V+	Positive output supply voltage range ⁽²⁾	−0.3	7	V
V−	Negative output supply voltage range ⁽²⁾	0.3	−7	V
V+ − V−	Supply voltage difference ⁽²⁾		13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)		V
		Receiver		
V _O	Output voltage range	Driver		V
		Receiver (INVALID)		
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DB package		°C/W
		PW package		
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) − T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

See [Figure 6](#)

		MIN	NOM	MAX	UNIT	
Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V	
	V _{CC} = 5 V	4.5	5	5.5		
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, EN		V		
		V _{CC} = 3.3 V	2			
	V _{CC} = 5 V	2.4				
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, EN		0.8	V	
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON		0	5.5	V
V _I	Receiver input voltage	−25		25	V	
T _A	Operating free-air temperature	TRSF3221EI	−40	85	°C	
		TRSF3221EC	0	70		

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON, EN		±0.01	±1	μA
I _{CC}	Supply current (T _A = 25°C)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V _{CC}	0.3	1	mA
		Powered off	No load, FORCEOFF at GND	1	10	
		Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded	1	10	μA

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
- (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

TRSF3221E

3-V TO 5.5-V SINGLE-CHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER

WITH ± 15 -kV IEC ESD PROTECTION

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DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage DOUT at R _L = 3 k Ω to GND, DIN = GND	5	5.4		V
V _{OL}	Low-level output voltage DOUT at R _L = 3 k Ω to GND, DIN = V _{CC}	–5	–5.4		V
I _{IH}	High-level input current V _I = V _{CC}		± 0.01	± 1	μ A
I _{IL}	Low-level input current V _I at GND		± 0.01	± 1	μ A
I _{OS}	Short-circuit output current ⁽³⁾ V _{CC} = 3.6 V, V _O = 0 V		± 35	± 60	mA
	V _{CC} = 5.5 V, V _O = 0 V		± 35	± 90	
r _o	Output resistance V _{CC} , V+, and V– = 0 V, V _O = ± 2 V	300	10M		Ω
I _{off}	Output leakage current FORCEOFF = GND			± 25	μ A
	V _O = ± 12 V, V _{CC} = 3 V to 3.6 V			± 25	
	V _O = ± 10 V, V _{CC} = 4.5 V to 5.5 V			± 25	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate (see Figure 1)	R _L = 3 k Ω	C _L = 1000 pF	250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V	1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V	1000		
t _{sk(p)}	Pulse skew ⁽³⁾ C _L = 150 pF to 2500 pF, R _L = 3 k Ω to 7 k Ω , See Figure 2		100		ns
SR(tr)	Slew rate, transition region (see Figure 1) V _{CC} = 3.3 V, R _L = 3 k Ω to 7 k Ω , C _L = 150 pF to 1000 pF	18		150	V/ μ s

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

ESD Protection

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
DOUT	13	HBM	± 15	kV
		IEC 61000-4-2 Contact Discharge	± 8	
		IEC 61000-4-2 Air-Gap Discharge	± 15	

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6 V	V _{CC} – 0.1 V		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.5		V
I _{off}	Output leakage current	FORCEOFF = 0 V		±0.05	±10	µA
r _i	Input resistance	V _i = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	150	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 3	150	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4	200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4	200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

ESD Protection

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
RIN	8	HBM	±15	kV
		IEC 61000-4-2 Contact Discharge	±8	
		IEC 61000-4-2 Air-Gap Discharge	±15	

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+} (valid)	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		2.7	V
V_{T-} (valid)	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-2.7		V
V_{T} (invalid)	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-0.3	0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	$I_{OH} = -1$ mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	$V_{CC} - 0.6$		V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	$I_{OL} = 1.6$ mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		0.4	V

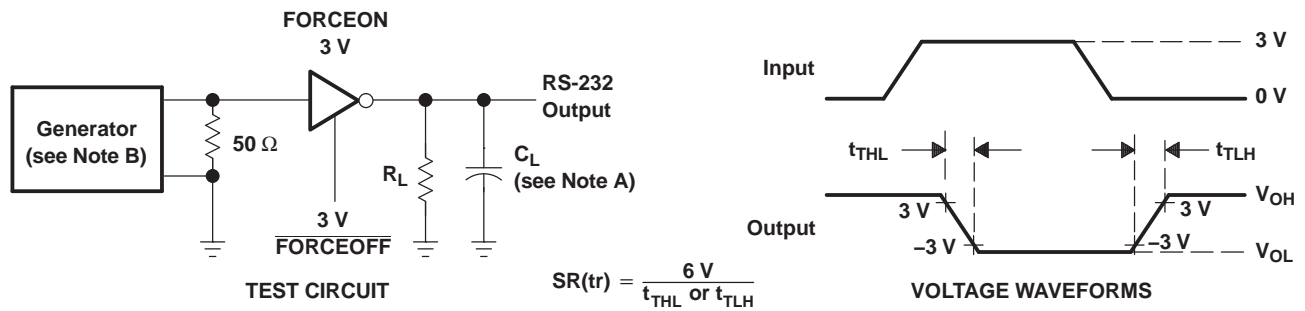
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
t_{invalid}	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

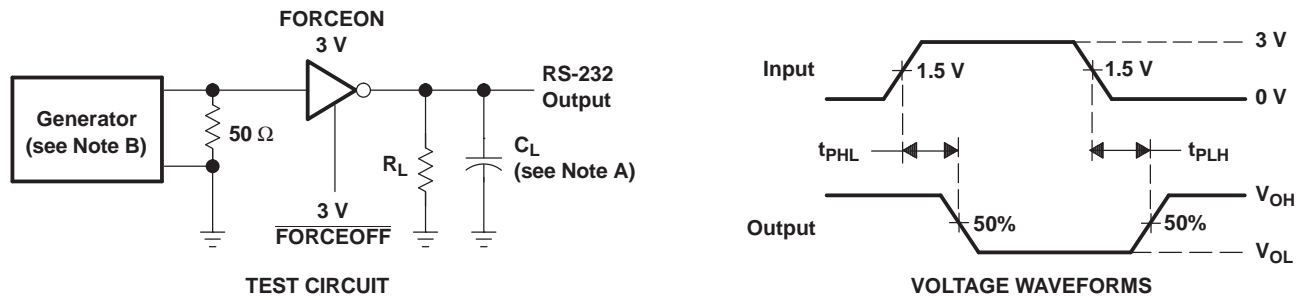
(1) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



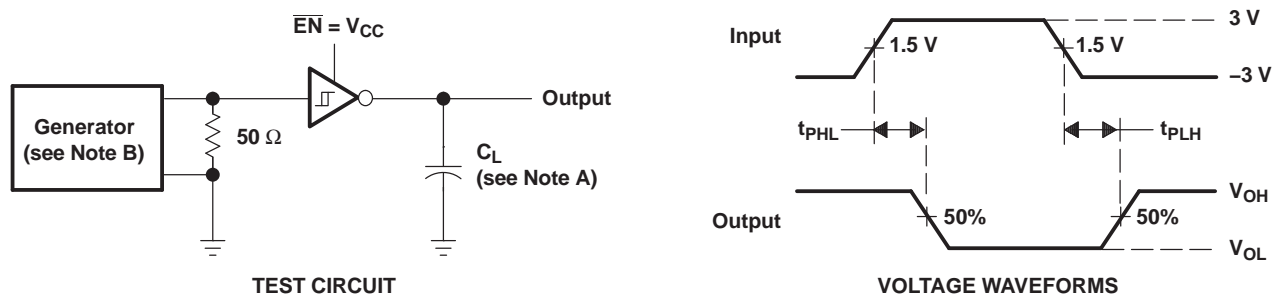
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

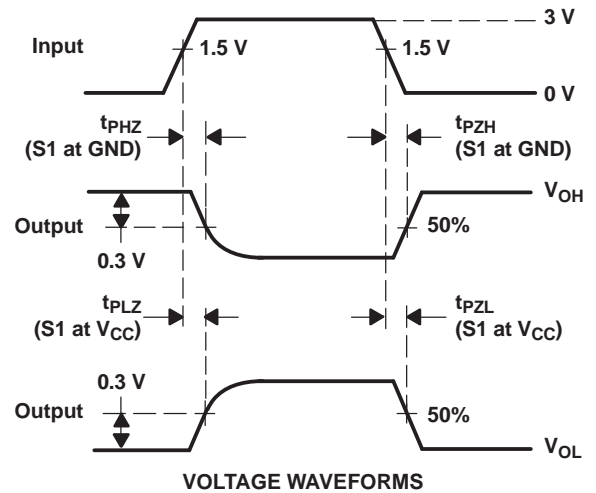
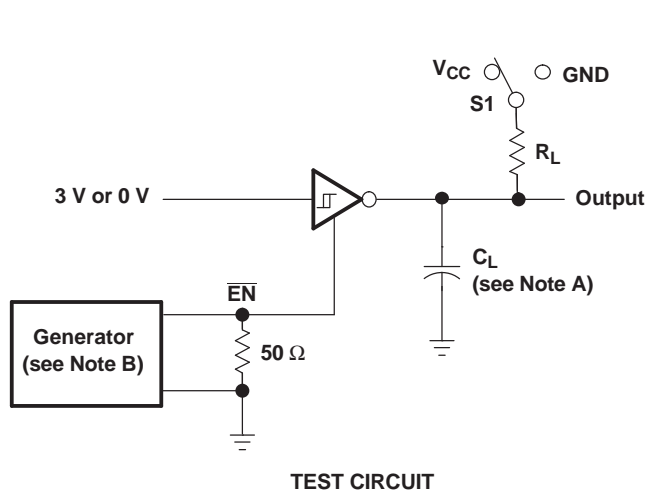
Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_0 = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

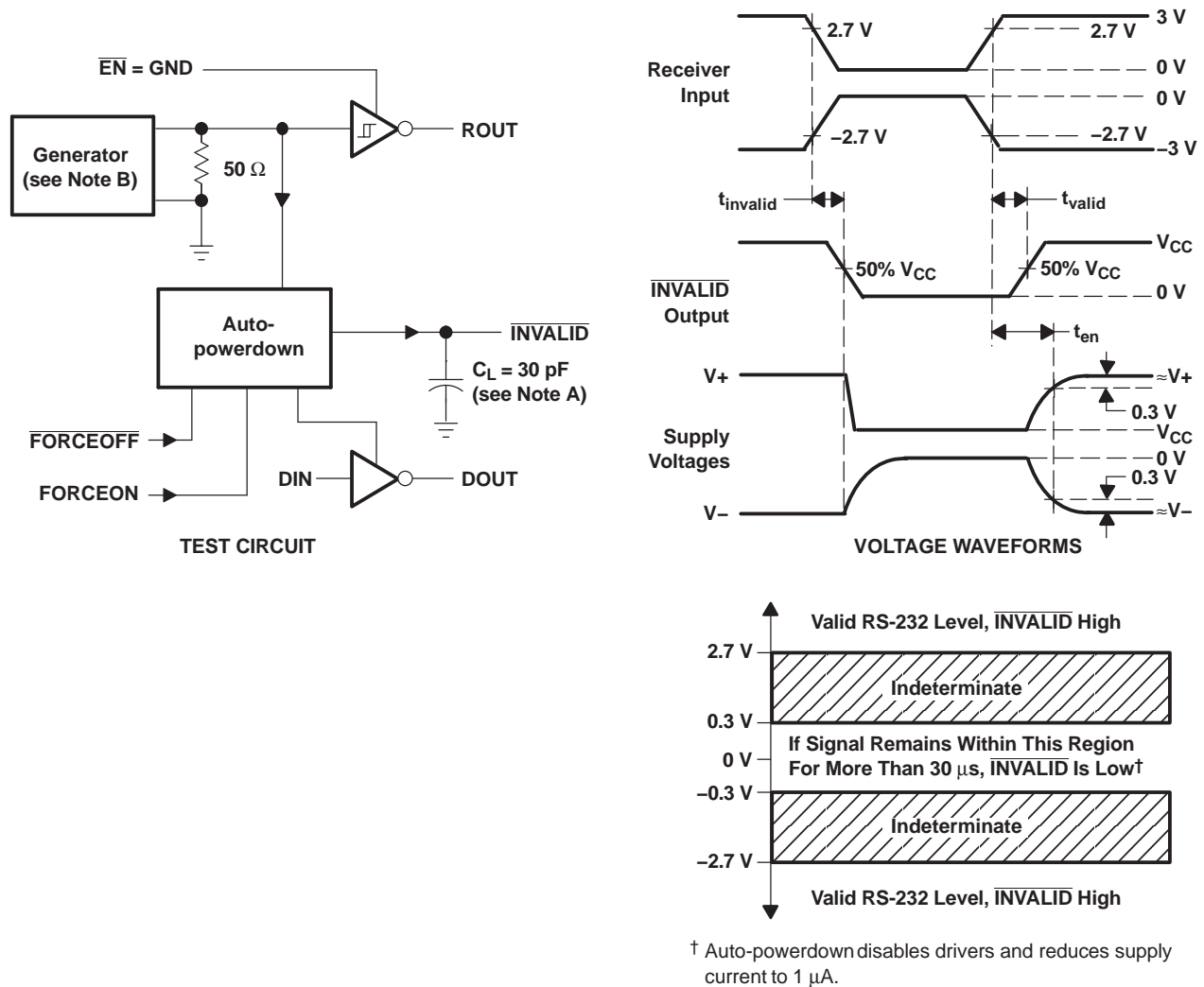
PARAMETER MEASUREMENT INFORMATION (continued)



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
 C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION (continued)

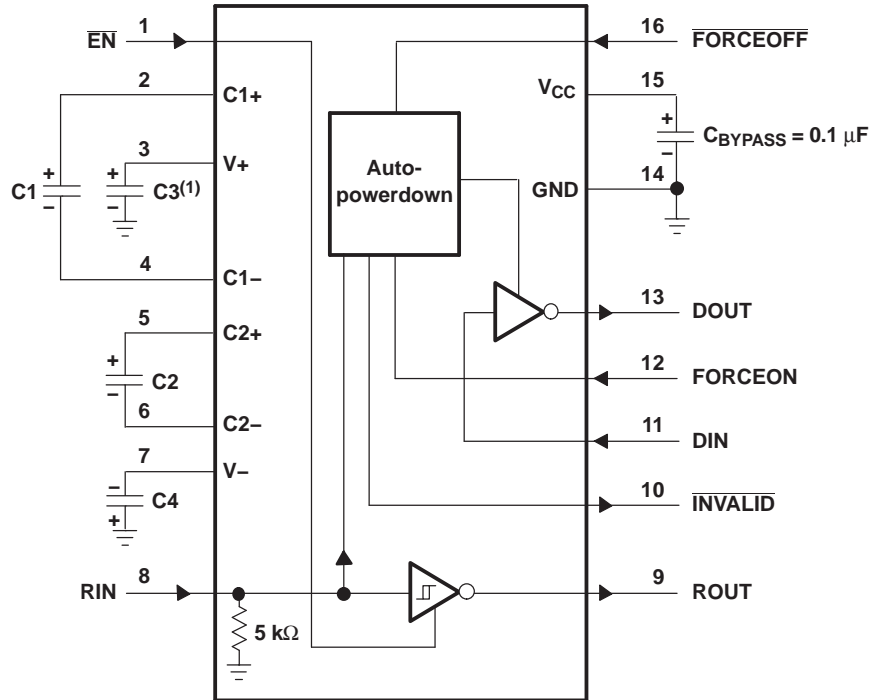


NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50$ Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

APPLICATION INFORMATION



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3221ECDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221EIDB	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85		
TRSF3221EIDBG4	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85		
TRSF3221EIDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRSF3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

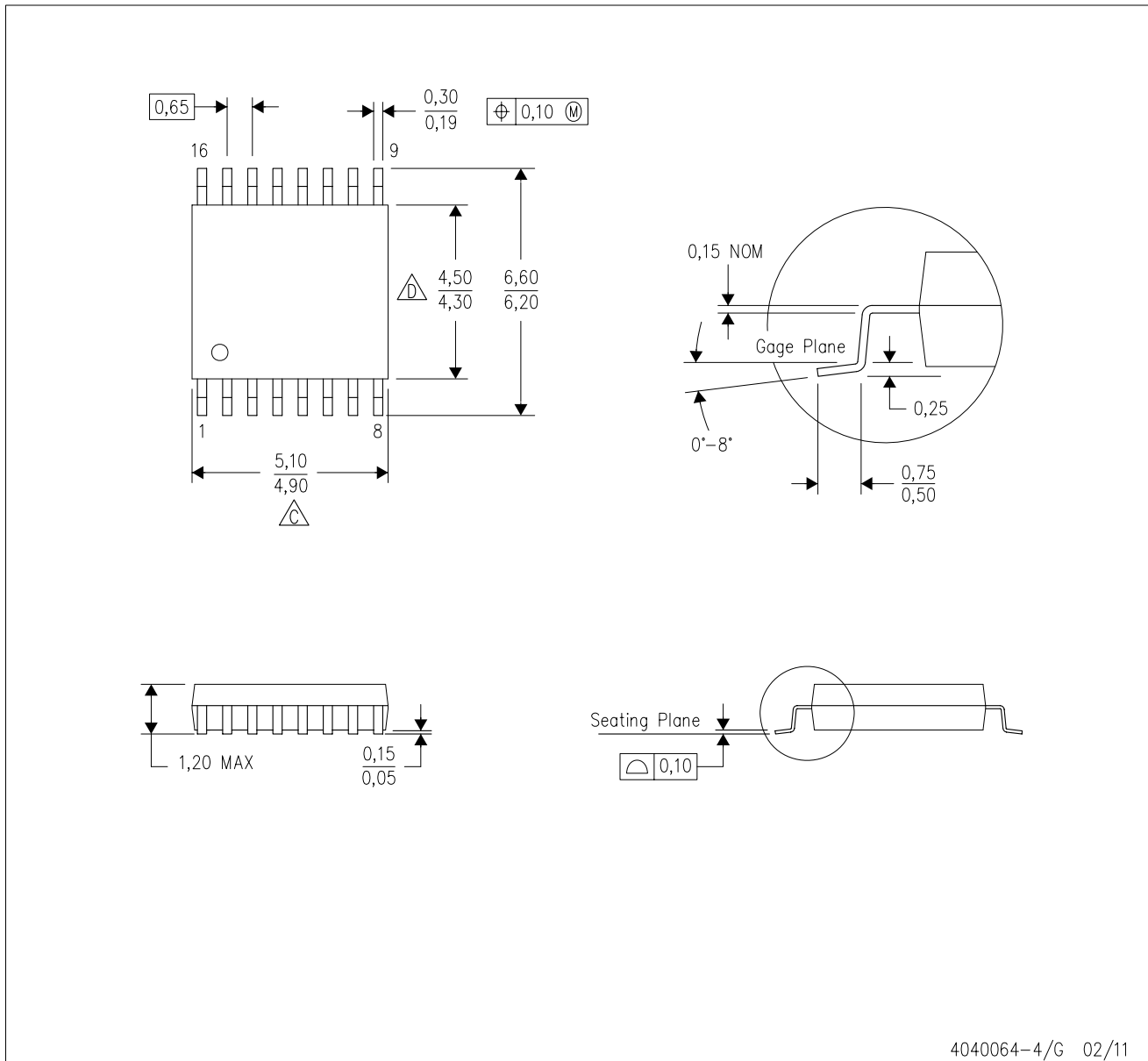

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3221ECDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TRSF3221ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRSF3221EIDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TRSF3221EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

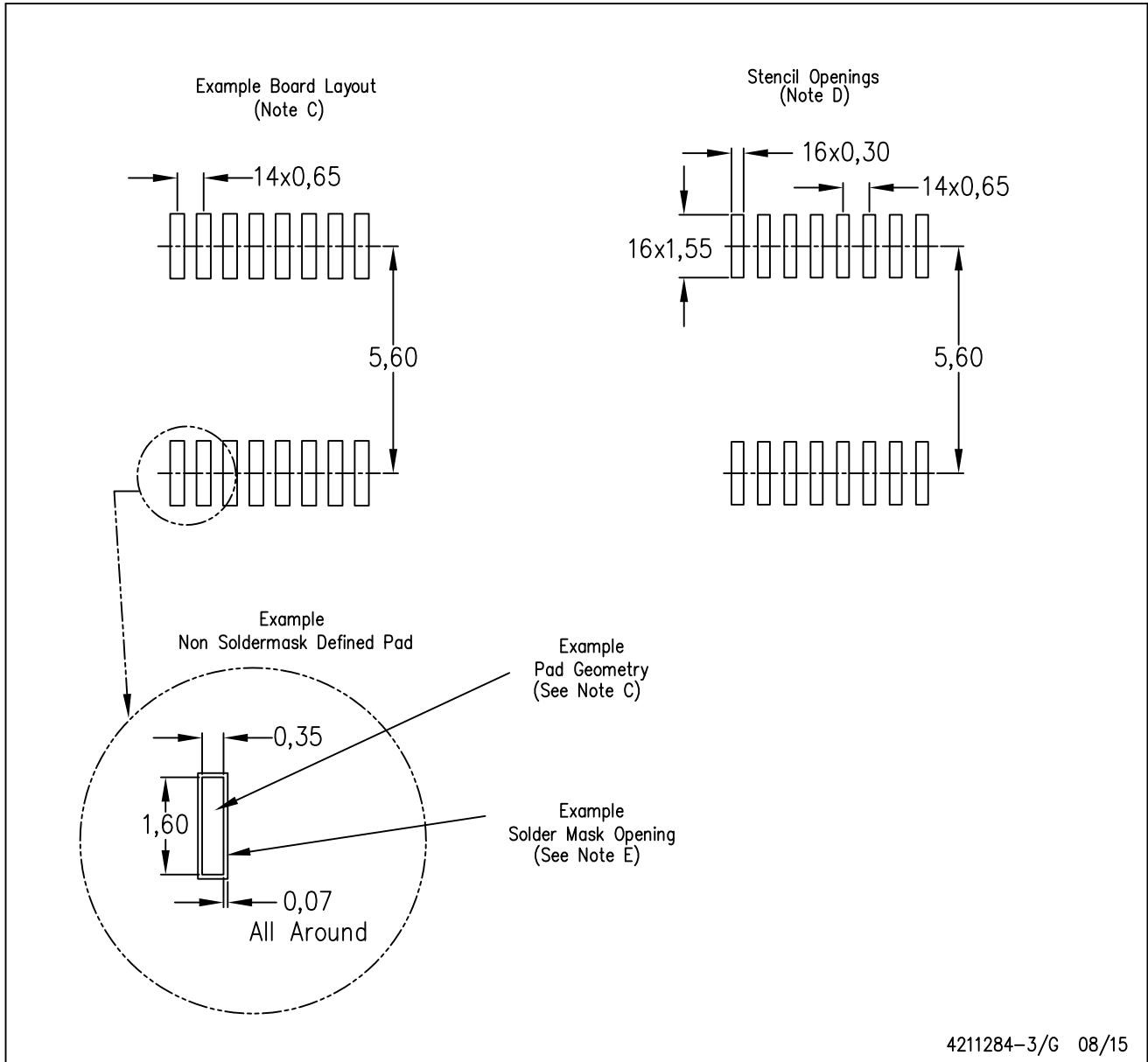


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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