TUSB9261 USB 3.0 to SATA Bridge

1 Features

- Universal Serial Bus (USB)
  - SuperSpeed USB 3.0 Compliant – TID 340730020
    - Integrated Transceiver Supports SS/HS/FS Signaling
  - Best-in-Class Adaptive Equalizer
    - Allows for Greater Jitter Tolerance in the Receiver
  - USB Class Support
    - USB Attached SCSI Protocol (UASP)
    - USB Mass Storage Class Bulk-Only Transport (BOT)
    - Support for Error Conditions Per the 13 Cases (Defined in the BOT Specification)
    - USB Bootability Support
    - USB Human Interface Device (HID)
  - Supports Firmware Update Via USB, Using a TI Provided Application
- SATA Interface
  - Serial ATA Specification Revision 2.6
    - Gen1i, Gen1m, Gen2i, and Gen2m
  - Support for Mass-Storage Devices Compatible With the ATA/ATAPI-8 Specification
- Integrated ARM Cortex M3 Core
  - Customizable Application Code Loaded from EEPROM by SPI Interface
  - Two Additional SPI Port Chip Selects for Peripheral Connection
  - Up to 12 GPIOs for End-User Configuration
    - Two GPIOs have PWM Functionality for LED Blink Speed Control
  - Serial Communications Interface for Debug (UART)
- General Features
  - Integrated Spread Spectrum Clock Generation Enables Operation from a Single Low-Cost Crystal or Clock Oscillator
    - Supports 40 MHz
  - A JTAG Interface is Used for IEEE1149.1 and IEEE1149.6 Boundary Scan
  - Available in a Fully RoHS-Compliant Package

2 Applications

- External HDD/SSD
- External DVD
- External CD
- HDD-Based Portable Media Player

3 Description

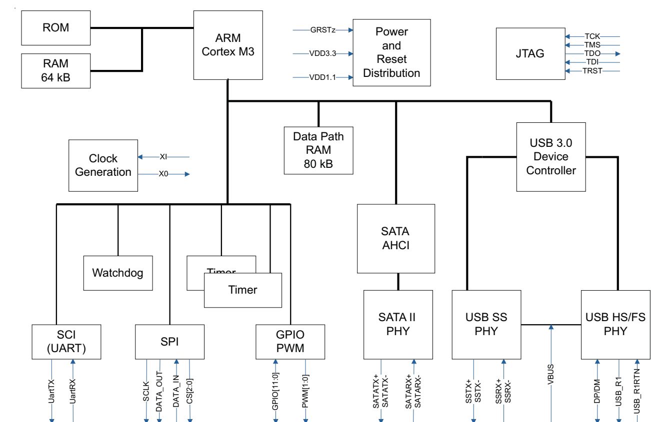
The TUSB9261 is an ARM® Cortex® M3 microcontroller based USB 3.0 to serial ATA bridge. It provides the necessary hardware and firmware to implement a USB attached SCSI protocol (UASP)-compliant mass storage device suitable for bridging hard disk drives (HDD), solid state disk drives (SSD), optical drives, and other compatible SATA 1.5-Gbps or SATA 3.0-Gbps devices to a USB 3.0 bus. In addition to UASP support, the firmware implements the mass storage class BOT and USB HID interfaces.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB9261	HTQFP (64)	7.00 × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 **Features** ... 1
2 **Applications** ... 1
3 **Description** ... 1
4 **Revision History** ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 7
- 6.1 Absolute Maximum Ratings ... 7
- 6.2 ESD Ratings ... 7
- 6.3 Recommended Operating Conditions ... 7
- 6.4 Thermal Information ... 7
- 6.5 DC Electrical Characteristics for 3.3-V Digital I/O ... 8
- 6.6 SuperSpeed USB Power Consumption ... 8
- 6.7 High-Speed USB Power Consumption ... 8
- 6.8 Oscillator Specification ... 9
- 6.9 Crystal Specification ... 9

7 **Detailed Description** ... 10
- 7.1 Overview ... 10
- 7.2 Functional Block Diagram ... 10
- 7.3 Feature Description ... 10
- 7.4 Device Functional Modes ... 13

8 **Application and Implementation** ... 15
- 8.1 Application Information ... 15
- 8.2 Typical Application ... 15

9 **Power Supply Recommendations** ... 19
- 9.1 Digital Supplies 1.1-V and 3.3-V ... 19
- 9.2 Analog Supplies 1.1-V and 3.3-V ... 19

10 **Layout** ... 19
- 10.1 Layout Guidelines ... 19
- 10.2 Layout Examples ... 20

11 **Device and Documentation Support** ... 22
- 11.1 Community Resources ... 22
- 11.2 Trademarks ... 22
- 11.3 Electrostatic Discharge Caution ... 22
- 11.4 Glossary ... 22

12 **Mechanical, Packaging, and Orderable Information** ... 22

4 Revision History

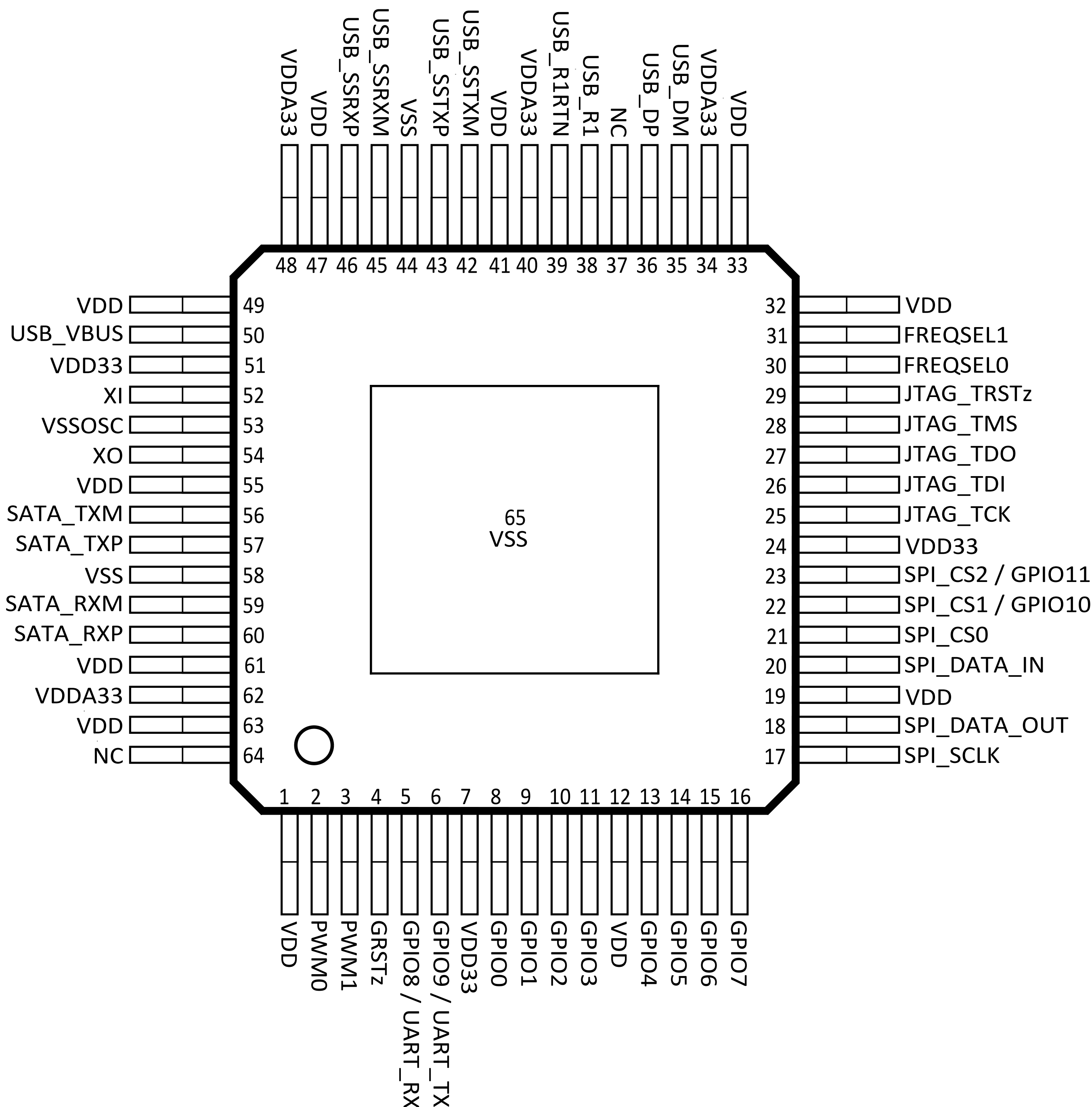
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (October 2014) to Revision H	Page
• Moved T_{stg} from *Handling Ratings* table to *Absolute Maximum Ratings* and renamed *Handling Ratings* to *ESD Ratings*	7
• Updated the frequency for the USB2 and USB3 to 5 Hz and 10 Hz, respectively	16

Changes from Revision F (March 2014) to Revision G	Page
• Updated supported frequency to 40 MHz	1
• Updated supported frequency in *Clock and Reset Signals* table	4
• Updated the frequency for the clock to 40 MHz	9
• Updated the frequency for the crystal to 40 MHz	9
• Updated oscillation frequency and ESR equivalent series resistance	9
• Updated Table 1	12

Copyright © 2011–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions



Signal Descriptions – I/O Definitions

I/O TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input/output
PU	Internal pullup resistor
PD	Internal pulldown resistor
PWR	Power signal

Clock and Reset Signals

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">I/O</th><th colspan="3" rowspan="2">DESCRIPTION</th></tr>
<tr><th>NAME</th><th>NO.</th></tr>
<tr><td>GRSTz</td><td>4</td><td>I
PU</td><td colspan="3">Global power reset. This reset brings all of the TUSB9261 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.</td></tr>
<tr><td>XI</td><td>52</td><td>I</td><td colspan="3">Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal, a 1-MΩ feedback resistor is required between X1 and XO.</td></tr>
<tr><td>XO</td><td>54</td><td>O</td><td colspan="3">Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator, this pin may be left unconnected. When using a crystal, a 1-MΩ feedback resistor is required between X1 and XO.</td></tr>
<tr><td rowspan="3">FREQSEL[1:0]</td><td rowspan="3">31, 30</td><td rowspan="3">I
PU</td><td colspan="3">Frequency select. These terminals indicate the oscillator input frequency and are used to configure the correct PLL multiplier. The field encoding is as follows:</td></tr>
<tr><th>FREQSEL[1]</th><th>FREQSEL[0]</th><th>INPUT CLOCK FREQUENCY</th></tr>
<tr><td>1</td><td>1</td><td>40 MHz</td></tr>
</table>

SATA Interface Signals(1)

PIN		I/O	DESCRIPTION
NAME	NO.		
SATA_TXP	57	O	Serial ATA transmitter differential pair (positive)
SATA_TXM	56	O	Serial ATA transmitter differential pair (negative)
SATA_RXP	60	I	Serial ATA receiver differential pair (positive)
SATA_RXM	59	I	Serial ATA receiver differential pair (negative)

(1) Note that the default firmware and reference design for the TUSB9261 have the SATA TXP/TXM swapped for ease of routing in the reference design. If you plan to use the TI default firmware please review the reference design in the *TUSB9261 DEMO User's Guide* (SLLU139) for proper SATA connection.

USB Interface Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
USB_SSTXP	43	O	SuperSpeed USB transmitter differential pair (positive)
USB_SSTXM	42	O	SuperSpeed USB transmitter differential pair (negative)
USB_SSRXP	46	I	SuperSpeed USB receiver differential pair (positive)
USB_SSRXM	45	I	SuperSpeed USB receiver differential pair (negative)
USB_DP	36	I/O	USB high-speed differential transceiver (positive)
USB_DM	35	I/O	USB high-speed differential transceiver (negative)
USB_VBUS	50	I	USB bus power
USB_R1	38	O	Precision resistor reference. A 10-kΩ ±1% resistor should be connected between R1 and R1RTN.
USB_R1RTN	39	I	Precision resistor reference return

Copyright © 2011–2015, Texas Instruments Incorporated

Serial Peripheral Interface (SPI) Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
SPI_SCLK	17	O PU	SPI clock
SPI_DATA_OUT	18	O PU	SPI master data out
SPI_DATA_IN	20	I PU	SPI master data in
SPI_CS0	21	O PU	Primary SPI chip select for flash RAM
SPI_CS2/ GPIO11	23	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.
SPI_CS1/ GPIO10	22	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.

JTAG, GPIO, and PWM Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
JTAG_TCK	25	I PD	JTAG test clock
JTAG_TDI	26	I PU	JTAG test data in
JTAG_TDO	27	O PD	JTAG test data out
JTAG_TMS	28	I PU	JTAG test mode select
JTAG_TRSTz	29	I PD	JTAG test reset
GPIO9/UART_TX	6	I/O PU	GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. This pin defaults to a general-purpose output.
GPIO8/UART_RX	5	I/O PU	GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. This pin defaults to a general-purpose output.
GPIO7	16	I/O PD	Configurable as general-purpose input/outputs
GPIO6	15	I/O PD	
GPIO5	14	I/O PD	
GPIO4	13	I/O PD	
GPIO3	11	I/O PD	
GPIO2	10	I/O PD	
GPIO1	9	I/O PD	
GPIO0	8	I/O PD	
PWM0	2	O PD[(1)]	Pulse-width modulation (PWM). Can be used to drive status LEDs.
PWM1	3	O PD[(1)]	

(1) PWM pulldown resistors are disabled by default. A firmware modification is required to turn them on. All other internal pull up/down resistors are enabled by default.

Power and Ground Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1 12 19 32 33 41 47 49 55 61 63	PWR	1.1-V power rail
VDD33	7 24 51	PWR	3.3-V power rail
VDDA33	34 40 48 62	PWR	3.3-V analog power rail
VSSOSC	53	PWR	Oscillator ground. If using a crystal, this should not be connected to a PCB ground plane. If using an oscillator, this should be connected to PCB ground. See *Clock Source Requirements* for more details.
VSS	44 58	PWR	Ground
VSS	65	PWR	Ground – Thermal pad
NC	37 64	—	No connect, leave floating

Copyright © 2011–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Steady-state supply voltage	–0.3	1.4	V
V_{DD33}/ V_{DDA33}	Steady-state supply voltage	–0.3	3.8	V
T_{stg}	Storage temperature	–55	150	°C

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 [1]	2000	V
		Charged device model (CDM), per JESD22-C101 [2]	5000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Digital 1.1-V supply voltage		1.045	1.1	1.155	V
V_{DD33}	Digital 3.3-V supply voltage		3	3.3	3.6	V
V_{DDA33}	Analog 3.3-V supply voltage		3	3.3	3.6	V
V_{BUS}	Voltage at VBUS PAD		0		1.155	V
T_A	Operating free-air temperature range		0		70	°C
		Industrial version	–40		85	
T_J	Operating junction temperature range		–40		100	°C

6.4 Thermal Information

THERMAL METRIC [1]		TUSB9261	UNIT
		PVP (HTQFP)	
		64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.1	°C/W
$R_{J\theta C(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics for 3.3-V Digital I/O

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
T_R	Rise time	5 pF			1.5	ns
T_F	Fall time	5 pF			1.53	ns
I_{OL}	Low-level output current	V_{DD33} = 3.3 V, T_J = 25°C		6		mA
I_{OH}	High-level output current	V_{DD33} = 3.3 V, T_J = 25°C		–6		mA
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	I_{OL} = –2 mA	2.4			V
V_O	Output voltage		0		VDD33	V
RECEIVER						
V_I	Input voltage		0		VDD33	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Input hysteresis		200			mV
t_T	Input transition time (T_R and T_F)				10	ns
I_I	Input current	V_I = 0 V to V_{DD33}			5	µA
C_I	Input capacitance	V_{DD33} = 3.3 V, T_J = 25°C		0.384		pF

6.6 SuperSpeed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)[1]	TYPICAL SUSPEND CURRENT (mA)[2]
VDD11	291	153
VDD33[3]	65	28

(1) Transferring data by SS USB to a SSD SATA Gen II device. No SATA power management, U0 only.
(2) SATA Gen II SSD attached no active transfer. No SATA power management, U3 only.
(3) All 3.3-V power rails connected together.

6.7 High-Speed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)[1]	TYPICAL SUSPEND CURRENT (mA)[2]
VDD11	172	153
VDD33[3]	56	28

(1) Transferring data via HS USB to a SSD SATA Gen II device. No SATA power management.
(2) SATA Gen II SSD attached no active transfer. No SATA power management.
(3) All 3.3-V power rails connected together.

Copyright © 2011–2015, Texas Instruments Incorporated

6.8 Oscillator Specification

XI should be tied to the 1.8-V clock source and XO should be left floating. VSSOSC should be connected to the PCB ground plane. A 40-MHz clock can be used.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XI}	XI input capacitance	T_J = 25°C		0.414		pF
V_{IL}	Low-level input voltage				0.7	V
V_{IH}	High-level input voltage		1.05			V
T_{tosc_i}	Frequency tolerance	Operational temperature	–50		50	ppm
T_{duty}	Duty cycle		45%	50%	55%	
T_R/T_F	Rise/fall time	20% to 80%			6	ns
R_J	Reference clock	JTF (1 sigma) [1][2]			0.8	ps
T_J	Reference clock	JTF (total p-p) [2][3]			25	ps
T_{p-p}	Reference clock jitter	(Absolute p-p) [4]			50	ps

(1) Sigma value assuming Gaussian distribution
(2) After application of JTF
(3) Calculated as 14.1 × R_J + D_J
(4) Absolute phase jitter (p-p)

6.9 Crystal Specification

A parallel, 20-pF load capacitor should be used if a crystal source is used. VSSOSC should not be connected to the PCB ground plane. A 40-MHz crystal can be used.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Oscillation mode				Fundamental	
f_O	Oscillation frequency			40		MHz
ESR	Equivalent series resistance	40 MHz			50	Ω
T_{tosc_i}	Frequency tolerance	Operational temperature			±50	ppm
	Frequency stability	1 year aging			±50	ppm
C_L	Load capacitance		12	20	24	pF
C_{SHUNT}	Crystal and board stray capacitance				4.5	pF
	Drive level (max)				0.8	mW

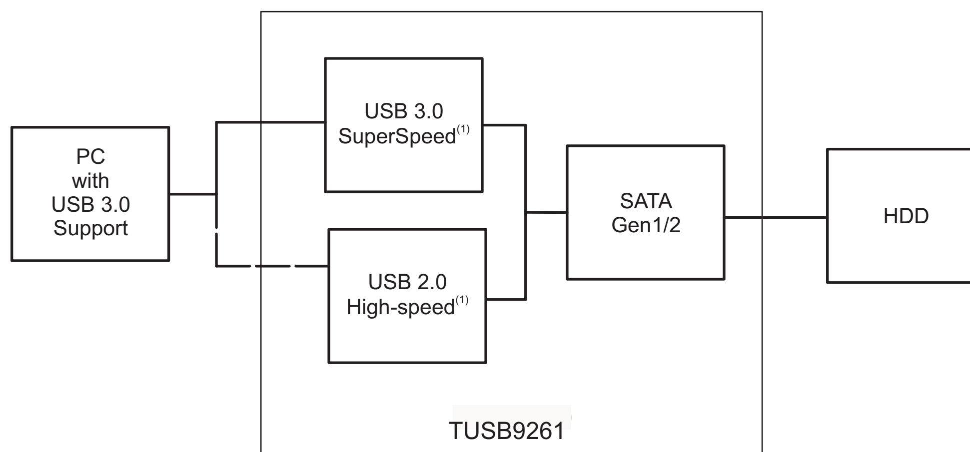
7 Detailed Description

7.1 Overview

The major functional blocks are as follows:

- Cortex M3 microcontroller subsystem including the following peripherals:
  - Time interrupt modules, including watchdog timer
  - Universal asynchronous receive/transmit (SCI)
  - SPI
  - General purpose input/output (GPIO)
  - PWM for support of PWM outputs (PWM)
- USB 3.0 core (endpoint controller) and integrated USB 3.0 PHY
- AHCI-compliant SATA controller and integrated SATA PHY
  - Supporting Gen1i, Gen1m, Gen2i, and Gen2m
- Chip level clock generation and distribution
- Support for JTAG 1149.1 and 1149.6

7.2 Functional Block Diagram



A. USB connection is made at either SuperSpeed or high speed, depending on the upstream connection support.

7.3 Feature Description

7.3.1 Operation

7.3.1.1 General Functionality

The TUSB9261 ROM contains boot code that executes after a global reset, which performs the initial configuration required to load a firmware image from an attached SPI flash memory to local RAM.

After the firmware is loaded, it configures the SATA advanced host controller interface host bus adapter (AHCI) and the USB device controller. In addition, the configuration of the AHCI includes a port reset, which initiates an out of band (OOB) TX sequence from the AHCI link layer to determine if a device is connected, and if so, negotiate the connection speed with the device (3.0 Gbps or 1.5 Gbps).

The configuration of the USB device controller includes creation of the descriptors, configuration of the device endpoints for support of UASP and USB mass storage class BOT, allocation of memory for the transmit request blocks (TRBs), and creation of the TRBs necessary to transmit and receive packet data over the USB. In addition, the firmware provides any other custom configuration required for application-specific implementation, for example, a HID interface for user initiated backup.

Copyright © 2011–2015, Texas Instruments Incorporated

Feature Description (continued)

After the USB device controller configuration is complete, if a SATA device was detected during the AHCI configuration, the firmware connects the device to the USB bus when VBUS is detected. According to the USB 3.0 specification, the TUSB9261 initially tries to connect at SuperSpeed USB. If successful, it enters U0; otherwise, after the training time out, it enables the DP pullup and connects as a USB 2.0 high-speed or full-speed device depending on the speed supported by host or hub port.

When connected, the firmware presents the BOT interface as the primary interface and the UASP interface as the secondary interface. If the host stack is UASP aware, it can enable the UASP interface using a SET_INTERFACE request for alternate interface 1.

Following speed negotiation, the device should transmit a device to host (D2H) FIS with the device signature. This first D2H FIS is received by the link layer and copied to the port signature register. When firmware is notified of the device connection, it queries the device for capabilities using the IDENTIFY DEVICE command. Firmware then configures the device as appropriate for its interface and features supported, for example, an HDD that supports native command queuing (NCQ).

7.3.1.2 Firmware Support

Default firmware support is provided for the following:

- SuperSpeed USB and USB 2.0 high speed and full speed
- USB attached SCSI protocol (UASP)
- USB mass storage class (MSC) bulk-only transport (BOT)
  - Including the 13 error cases
- USB mass storage specification for bootability
- USB device class definition for HID
  - Firmware update and custom functionality (for example, one-touch backup)
- Serial ATA advanced host controller interface (AHCI)
- GPIO
  - LED control and custom functions (for example, one-touch backup control)
- PWM
  - LED dimming control
- SPI
  - Firmware storage and storing custom device descriptors
- Serial communications interface (SCI)
  - Debug output only

Copyright © 2011–2015, Texas Instruments Incorporated

Feature Description (continued)

7.3.1.3 GPIO/PWM LED Designations

The default firmware provided by TI drives the GPIO and PWM outputs as listed in Table 1.

Table 1. GPIO/PWM LED Designations

<table>
<tr><th>GPIO</th><th colspan="2">DESCRIPTION</th><th>DEFAULT SETUP</th></tr>
<tr><td>GPIO0</td><td colspan="2">Undefined. Can use HID commands to change to output low or high. [internal 100-μA PD]</td><td>Input</td></tr>
<tr><td>GPIO1</td><td colspan="2">USB 3.0 Link State if U1/U2 enabled, otherwise [input with 100-μA PD]</td><td>Output</td></tr>
<tr><td>GPIO5</td><td colspan="2">USB 3.0 Link State if U1/U2 enabled, otherwise [input with 100-μA PD]</td><td>Output</td></tr>
<tr><td rowspan="5">GPIO1/ GPIO5</td><td rowspan="5">USB3 power state (U0 to U3)</td><td>U0: Off/Off</td><td rowspan="5">Output</td></tr>
<tr><td>U1: On/Off</td></tr>
<tr><td>U2: Off/On</td></tr>
<tr><td>U3: On/On</td></tr>
<tr><td>Other: Off/Off</td></tr>
<tr><td>GPIO2</td><td colspan="2">HS/FS suspend</td><td>Output</td></tr>
<tr><td>GPIO3</td><td colspan="2">[INPUT with 100-μA PD] momentary push button</td><td>Input</td></tr>
<tr><td>GPIO4</td><td colspan="2">Bus- or self-powered indicator. (GPIO level should be HIGH when self-powered). [internal 100-μA PD]</td><td>Input</td></tr>
<tr><td>GPIO6</td><td colspan="2">Undefined. Can use HID commands to change to output low or high. [internal 100-μA PD]</td><td>Input</td></tr>
<tr><td>GPIO7</td><td colspan="2">SS connection</td><td>Output</td></tr>
<tr><td>GPIO10</td><td colspan="2">Undefined. Can use HID commands to change to output low or high. Compile option to configure as SATA drive power enable output. [internal 100-μA PU]</td><td>Input</td></tr>
<tr><td>GPIO11</td><td colspan="2">Power fault indicator. [internal 100-μA PU]</td><td>Input</td></tr>
<tr><td>PWM0</td><td colspan="2">Disk activity (LED blink rate is faster when connected at USB SuperSpeed), USB connection (LED on), and USB suspend (fading LED).</td><td>Output</td></tr>
<tr><td>PWM1</td><td colspan="2">SW heartbeat</td><td>Output</td></tr>
</table>

The LEDs on the TUSB9261 product development kit (PDK) board are connected as in Table 1. See the TUSB9261 PDK Guide for more information on GPIO LED connection and usage. This EVM is available for purchase. Contact TI for ordering information.

7.3.1.4 Power-Up and Reset Sequence

The core power (VDD) must be present and at its minimum high level prior to, or at the same time that, the I/O power (VDD33).

In addition, meet the following constraints:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected lifetime of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 2 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the deassertion of GRSTz.

Copyright © 2011–2015, Texas Instruments Incorporated

7.3.2 Clock Connections

7.3.2.1 Clock Source Requirements

The TUSB9261 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow these guidelines.

Because XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. TI also recommends to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

Load capacitance (C_{load}) of the crystal (varies with the crystal vendor) is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors, CL1 and CL2, in Figure 1. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB9261 must be minimized. TI also recommends that the trace length from the capacitor pad to the power or ground plane be minimized.

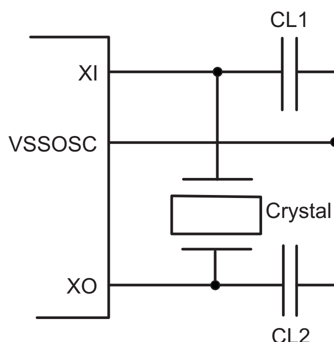


Figure 1. Typical Crystal Connections

7.3.2.2 Clock Source Selection Guide

Reference clock jitter is an important parameter. Jitter on the reference clock degrades both the transmit eye and receiver jitter tolerance no matter how clean the rest of the PLL is, thereby impairing system performance. Additionally, a particularly jittery reference clock may interfere with the PLL lock detection mechanism, forcing the lock detector to issue an Unlock signal. A good-quality, low-jitter reference clock is required to achieve compliance with supported USB3.0 standards. For example, USB3.0 specification requires the random jitter (RJ) component of either RX or TX to be 2.42 ps (random phase jitter calculated after applying jitter transfer function (JTF)). As the PLL typically has a number of additional jitter components, the reference clock jitter must be considerably below the overall jitter budget.

7.4 Device Functional Modes

7.4.1 VBUS Power

Power can be supplied by a USB cable on the terminal VBUS. When using power from VBUS, both the TUSB9261 and the SATA device are allowed to draw only up to 500 mA from VBUS when operating.

7.4.2 External Power

Power can be supplied from an external power source. When using an external power source, both the TUSB9261 and the SATA interface can draw all their current from the external supply.

Copyright © 2011–2015, Texas Instruments Incorporated

Device Functional Modes (continued)

7.4.3 External Voltage Regulator

Because the TUSB9261 requires two voltage supplies (1.1 V and 3.3 V), TI recommends a multi-channel voltage regulator. The TPS650061 or TPS65024x are good choices. The TPS650061 uses a DC-DC converter and two LDO regulators in a single package. The DC-DC converter can supply 1-A nominal current while the two LDOs can supply 300-mA nominal current. Because the 1.1-V supply can consume upwards of 340 mA of current, the DC-DC converter is ideal for supplying the 1.1-V current while the two LDOs can be used to supply 3.3-V current. Likewise the TPS65024x uses three DC-DC converters and three LDOs. Both devices also have a built-in supervisor circuit that can be connected to $\overline{GRST}$ on the TUSB9261.

Copyright © 2011–2015, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device serves as a bridge between a downstream USB 3.0 host port and a SATA device such as a hard disk drive. A crystal or oscillator supplies the required clock source. A SPI flash device contains the firmware that is loaded into the TUSB9261 after the deassertion of RESET. Push buttons or any other desired logic can be connected to the TUSB9261 GPIO pins. The TUSB9261 can also output a pulse-width modulated signal that can be used to drive an activity LED.

8.2 Typical Application

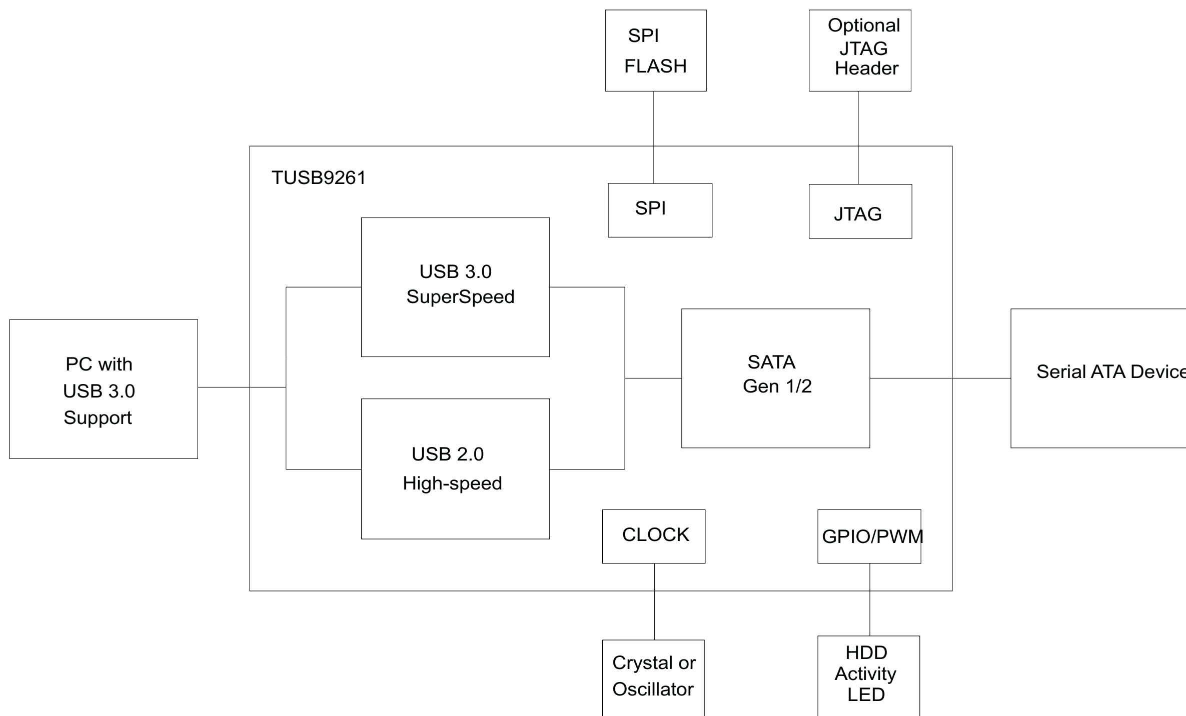


Figure 2. Typical Application Schematic

8.2.1 Design Requirements

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD supply	1.1 V
VDD33 supply	3.3 V
Upstream port USB support	SS, HS, FS
Main supply	VBUS
USB_VBUS resistor values	90.9 kΩ, 10 kΩ
Crystal frequency	40 MHz
SATA device	SSD

8.2.2 Detailed Design Procedure

8.2.2.1 PWM Terminals

The TUSB9261 has two pulse-width modulated output terminals.

Table 3 shows the default firmware configuration of PWMs.

Table 3. Default Firmware Configuration of PWMs

PWM	USAGE
0	Primary Indicator LED: ON when there is a USB connection. OFF when there is no connection. Blinks during disk activity (Frequency: 5 Hz for USB2 or 10 Hz for USB3). Fades when USB is in Suspend or U3 state.
1	Power indicator LED

PWM duty cycle will be 0% when the LED should be fully ON.

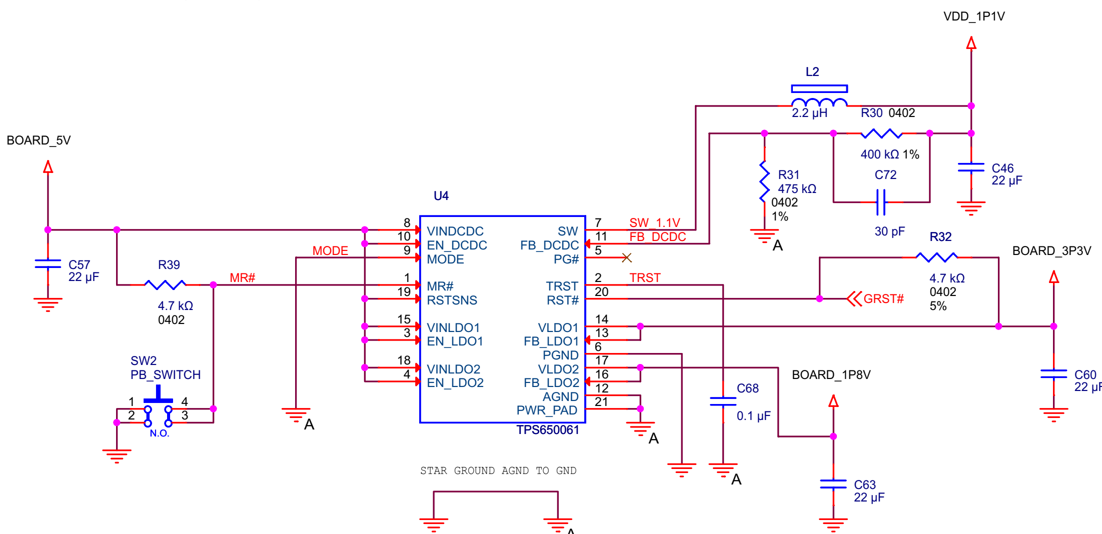
8.2.2.2 JTAG Interface

The TUSB9261 supports JTAG for board-level test and debug support. Typically, these terminals are left unconnected or routed to a header to plug in an external JTAG controller. Table 4 shows the JTAG terminal names and internal resistor connection. The JTAG interface should be left unconnected if JTAG support is not required.

Table 4. Internal JTAG Resistor Termination

NAME	PULL UP OR PULL DOWN	DESCRIPTION
JTAG_TCK	Pull down	JTAG test clock
JTAG_TDI	Pull up	JTAG test data in
JTAG_TDO	Pull down	JTAG test data out
JTAG_TMS	Pull up	JTAG test mode select
JTAG_RSTZ	Pull down	JTAG reset

8.2.2.3 Voltage Regulator Schematic



8.2.2.4 SPI

A SPI system consists of one master device and one or more slave devices. The TUSB9261 is a SPI master providing the SPI clock, data-in, data-out, and up to three chip-select terminals.

Copyright © 2011–2015, Texas Instruments Incorporated

The SPI has a 4-wire synchronous serial interface. Data communication is enabled with an active-low chip select terminal (SPI_CS[2:0]#). Data is transmitted with a 3-terminal interface consisting of terminals for serial data input (SPI_DATA_IN), serial data output (SPI_DATA_OUT) and serial clock (SPI_SCLK).

All SPI terminals have integrated pullup resistors. No external components are required to connect the SPI interface to an external SPI flash device. See Figure 3 for an example implementation of the SPI interface using one SPI slave device.

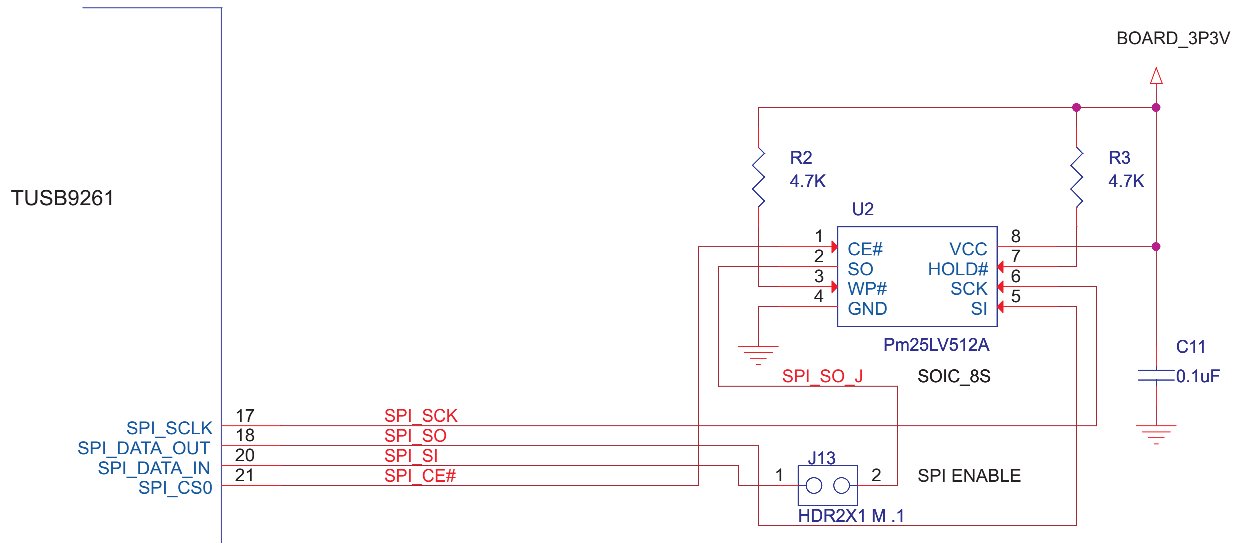


Figure 3. SPI Connection

The SPI_CLK is running at a fixed frequency of 18.75 MHz and its clocking mode is configured with a POLARITY of 0 and a PHASE of 1, this means that the SPI sends the data output one half-cycle before the first rising edges of SPI_CLK and on subsequent falling edges. Meanwhile, the input data is latched on the rising edge of SPI_CLK (see Figure 4 and Table 5 for a detailed timing description).

The flash memory is erased by the bootloader prior to programming and must use a word size of 8 bits with an address length of 24 bits and its program instruction must allow 256 bytes to be written in one operation. TI recommends a minimum flash size of 512 kb (64 k × 8). Table 5 shows SPI flash devices that have been tested with the TUSB9261.

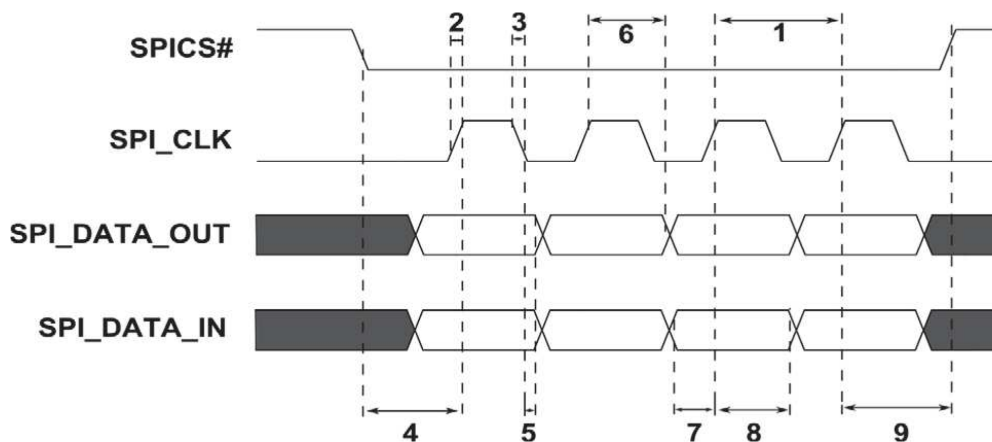


Figure 4. SPI Characterization

Table 5. SPI Characterization Time

NO.	TIME REFERENCE	THEORETICAL VALUE
1	Cycle time SPICLK	53.3 ns
2	Positive SPI_CLK slope	2 ns
3	Negative SPI_CLK slope	3 ns
4	SPISCS – SPICLK edge(PHASE = 1)	MIN: 53.3 ns TYP: 80 ns MAX: 93.3 ns
5	Output delay time, SPICLK TX edge to SPISIMO valid	260 ps
6	Output hold time, SPICLK RX edge to SPISIMO valid	26.7 ns
7	Setup time	22 ns
8	Hold time	500 ps
9	"SPICLK -SPISCS Phase = 1, Master"	13.3 ns

Copyright © 2011–2015, Texas Instruments Incorporated

9 Power Supply Recommendations

9.1 Digital Supplies 1.1-V and 3.3-V

The TUSB9261 requires a 1.1-V and 3.3-V digital power source.

The 1.1-V terminals are named VDD11. These terminals supply power to the digital core. The 1.1-V core allows for a significant reduction in both power consumption and logic switching noise.

The 3.3-V terminals are named VDD33 and supply power to most of the input and output cells. Both VDD11 and VDD33 supplies must have 0.1-µF bypass capacitors to VSS (ground) to ensure proper operation. One capacitor per power terminal is sufficient and should be placed as close to the terminal as possible to minimize trace length. TI also recommends smaller value capacitors like 0.01-µF on the digital supply terminals.

When placing and connecting all bypass capacitors, follow high-speed board design rules.

9.2 Analog Supplies 1.1-V and 3.3-V

TI recommends a Pi filter on all analog power terminals to minimize circuit noise. These filters can be combined on a per-rail basis for a total of two (VDDA11 / VDDA11_USB2) + (VDDA33).

Analog power terminals must have a 1-µF and a 10-µF bypass capacitor connected to VSSA (ground) to ensure proper operation. Place the capacitor as close as possible to the associated terminal to minimize trace length. TI also recommends smaller value capacitors such as 0.1-µF and 0.01-µF on the analog supply terminals.

10 Layout

10.1 Layout Guidelines

10.1.1 High-Speed Differential Routing

The high-speed differential pair (USB_DM and USB_DP) is connected to a USB type B connector. The differential pair traces should be routed with 90-Ω, ±15% differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between high-speed USB signal pairs should be no greater than 150 mils. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. No termination or coupling capacitors are required. If a common-mode choke is required, then place the choke as close as possible to the USB connector signal pins. Likewise, ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).

To minimize crosstalk on the USB2/3 differential signal pairs, TI recommends that the spacing between the two interfaces be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs and the DP/DM differential pair. If this 5W rule cannot be implemented, then the space between the TX/RX differential pairs and DP/DM differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

10.1.2 SuperSpeed Differential Routing

SuperSpeed consists of two differential routing pairs, a transmit pair (USB_SSTXM and USB_SSTXP) and a receive pair (USB_SSRXM and USB_SSRXP). Each differential pair's traces should be routed with 90-Ω, ±15% differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between SuperSpeed USB signal pairs should be no greater than 2.5 mils. The transmit differential pair does not have to be the same length as the receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. The transmitter differential pair requires 0.1-uF coupling capacitors for proper operation. The package/case size of these capacitors should be no bigger than 0402. C-packs are not allowed. The capacitors should be placed symmetrically as close as possible to the USB connector signal pins. If a common mode choke is required, then place the choke as close as possible to the USB connector signal pins (closer than the transmitter capacitors). Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter capacitors).

Copyright © 2011–2015, Texas Instruments Incorporated

Layout Guidelines (continued)

It is permissible to swap the plus and minus on either or both of the SuperSpeed differential pairs. This may be necessary to prevent the differential traces from crossing over one another. However, it is not permissible to swap the transmitter differential pair with receive differential pair. To minimize crosstalk on the SS USB differential signal pairs, TI recommends that the spacing between the TX and RX signal pairs be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

10.1.3 SATA Differential Routing

The SATA traces (SATA_TXP and SATA_TXM) should be routed with 100-Ω, ±15% differential impedance. Maximum trace length mismatch between SATA signal pairs should be no greater than 2.5 mils. The transmit differential pair does not have to be the same length as receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. Each SATA trace requires a coupling capacitor be placed inline. The package/case size of these capacitors should be no bigger than 0402. C-packs are not allowed. The capacitors should be placed symmetrically as close as possible to the SATA connector signal pins.

It is permissible to swap the plus and minus on the SATA differential pair. This may be necessary to prevent the differential traces from crossing over one another. However, it is not permissible to swap the transmitter differential pair with the receive differential pair.

To minimize crosstalk on the SATA differential signal pairs, TI recommends that the spacing between the TX and RX signal pairs for each interface be five times the width of the trace (5W rule). For instance, if the SATA TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs. If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

10.2 Layout Examples

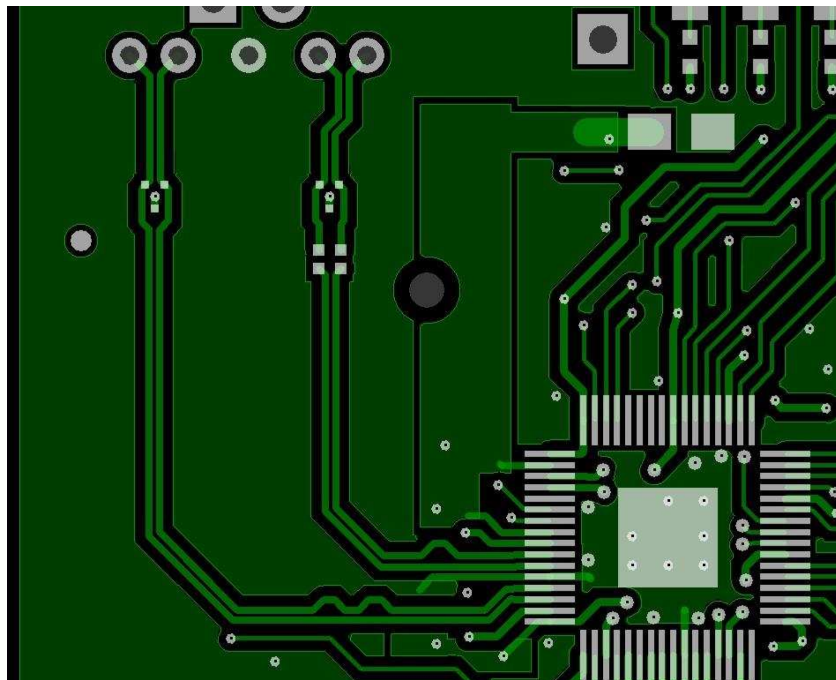


Figure 5. SuperSpeed Differential Routing

Copyright © 2011–2015, Texas Instruments Incorporated

Layout Examples (continued)

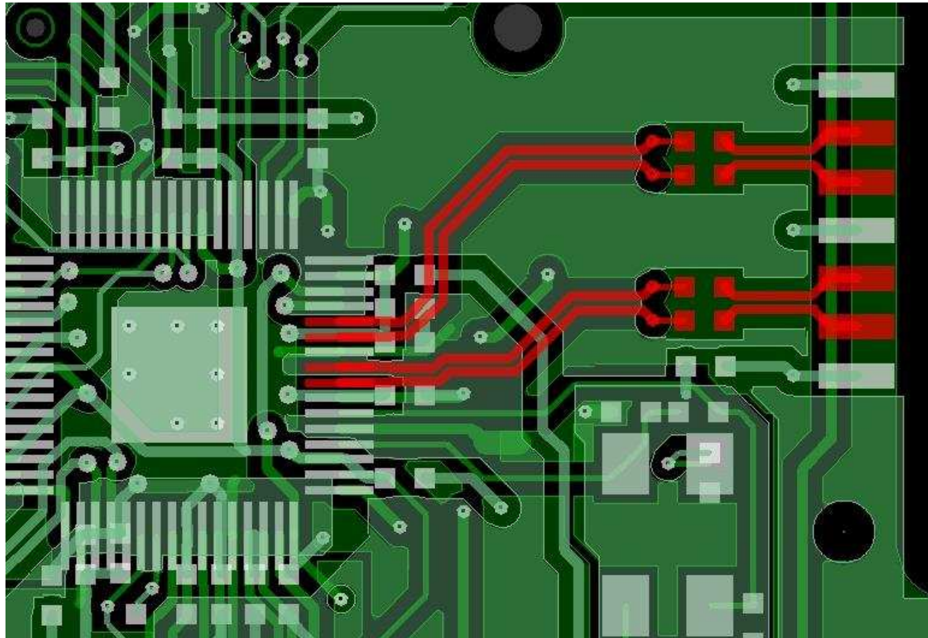


Figure 6. SATA Differential Routing

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
ARM, Cortex are registered trademarks of ARM Ltd.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

 Copyright © 2011–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB9261IPVP	ACTIVE	HTQFP	PVP	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB9261I	Samples
TUSB9261PVP	ACTIVE	HTQFP	PVP	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB9261	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

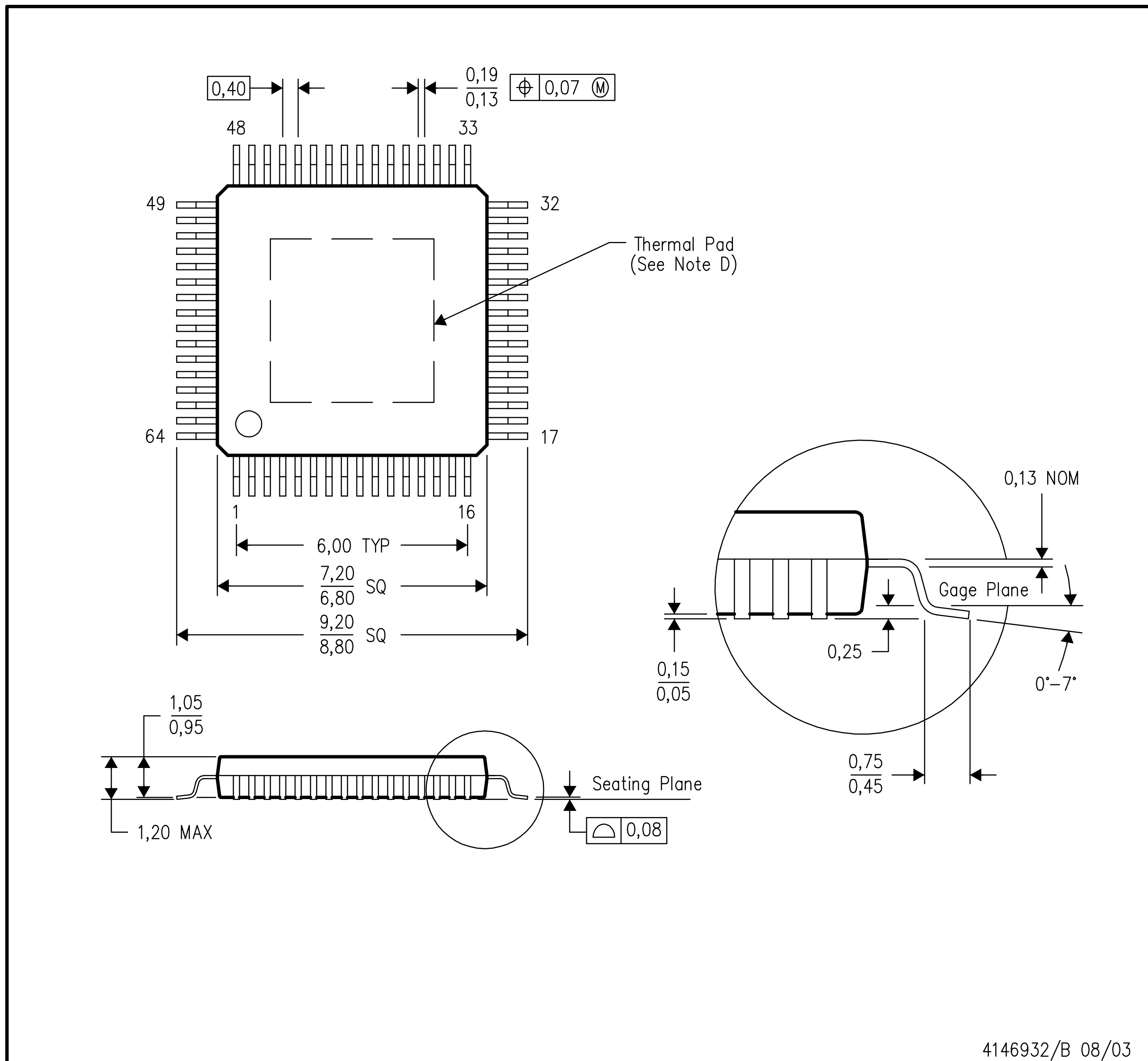
OTHER QUALIFIED VERSIONS OF TUSB9261 :

- Automotive: TUSB9261-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PVP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

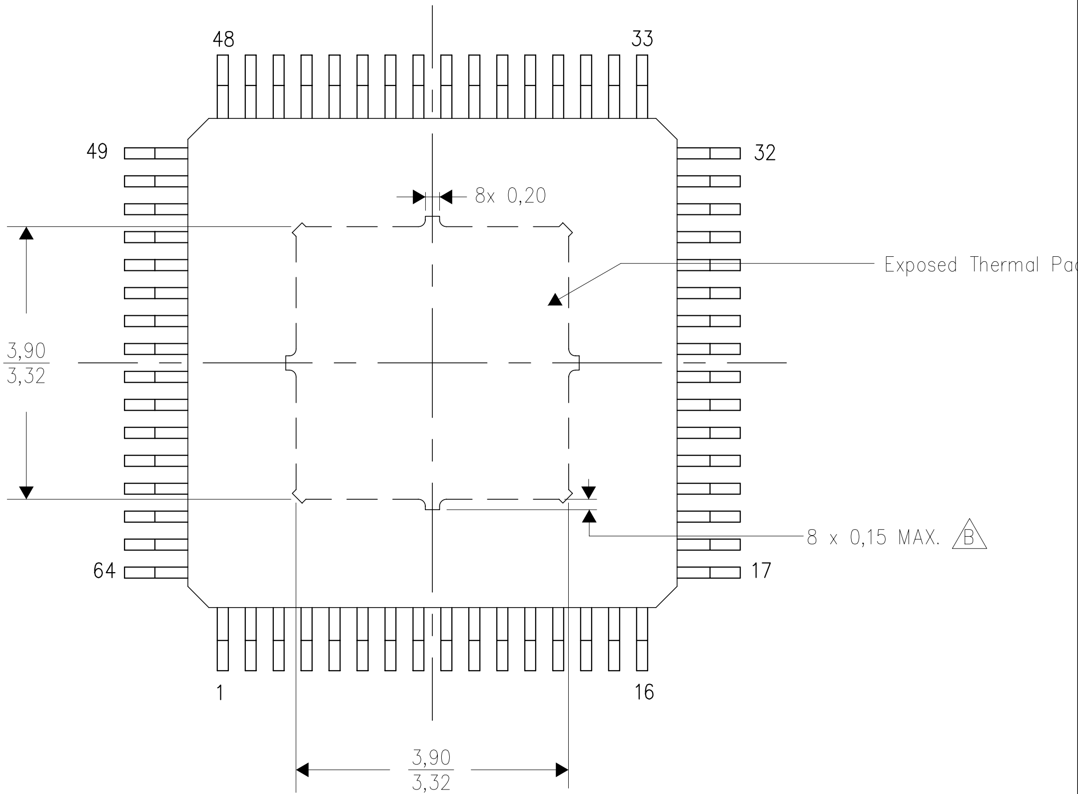
PVP (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4211213/B 09/10

NOTES: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2015, Texas Instruments Incorporated