# DUAL CHANNEL POWER DRIVER

## FEATURES

- **Two Independent Drivers**
- **1.5 A Totem Pole Outputs**
- **Inverting and Non-Inverting Inputs**
- **40 ns Rise and Fall Into 1000 pF**
- **High-Speed, Power MOSFET Compatible**
- **Low Cross-Conduction Current Spike**
- **Analog Shutdown With Optional Latch**
- **Low Quiescent Current**
- **5 V to 40 V Operation**
- **Thermal Shutdown Protection**
- **16-Pin Dual-In-Line Package**
- **20-Pin PLCC and CLCC Package**

## DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices–particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5 A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both $V_{IN}$ and $V_C$ can independently range from 5 V to 40 V.

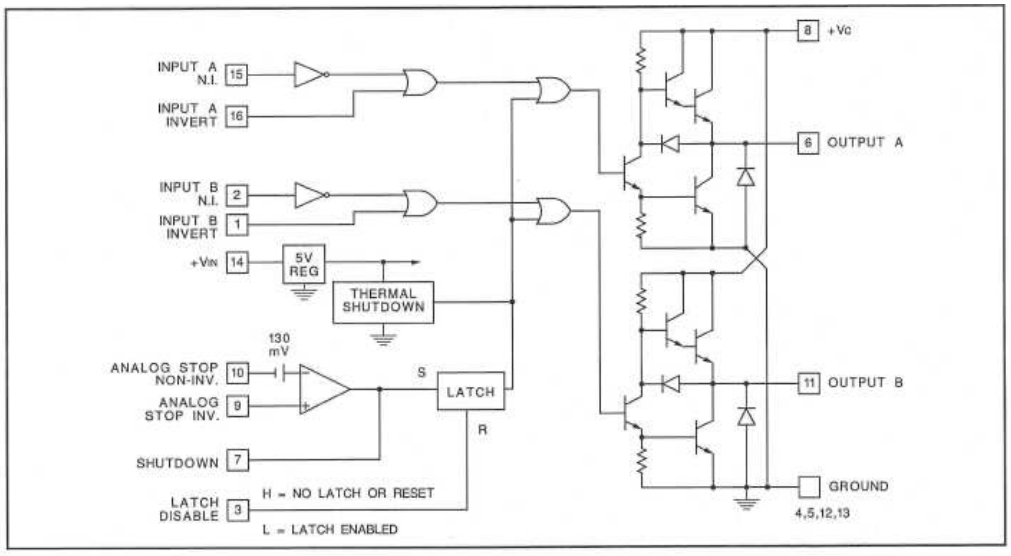
These devices are available in two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for –55°C to +125°C operation. Also available in surface mount DW, Q, L packages.

**TRUTH TABLE**
**(Each Channel)(1)**

| INV. | N.I. | OUT |
|---|---|---|
| H | H | L |
| L | H | H |
| H | L | L |
| L | L | L |

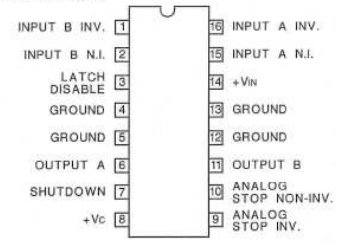
(1) $\underline{OUT} = \overline{INV}$ and N.I.
$\overline{OUT}$ = INV or N.I.

## BLOCK DIAGRAM



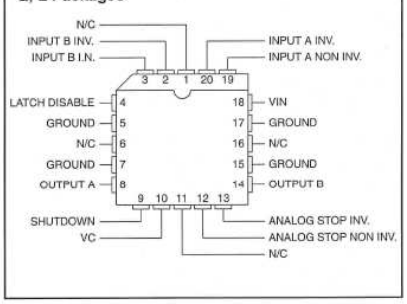

## CONNECTION DIAGRAMS

**DIL-16, SOIC-16 (TOP VIEW)**
**J or N Package,**




*Note: All four ground pins must be connected to a common ground.*

**PLCC-20, LCC-20 (TOP VIEW)**
**Q, L Packages**



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage | N/J package | | 40 | V |
| $V_C$ | Collector supply voltage | N/J package | | 40 | V |
| | Output current (each output, source or sink) steady-state | N/J package | | ±500 | mA |
| | Peak transient | N package | | ±1.5 | A |
| | | J package | | ±1.0 | |
| | Capacitive discharge energy | N package | | 20 | mJ |
| | | J package | | 15 | |
| | Digital inputs(1) | N/J-package | | 5.5 | V |
| | Analog stop inputs | N/J package | | $V_{IN}$ | |
| | Power dissipation at $T_A$ = 25°C | N package | | 2 | W |
| | | J package | | 1 | |
| | Power dissipation at T (leads/case) = 25°C(1) | N package | | 5 | W |
| | | J package | | 2 | |
| | Operating temperature range | | –55 | +125 | °C |
| | Storage temperature range | | –65 | +150 | °C |
| | Lead temperature (soldering, 10 seconds) | | | 300 | °C |

(1) All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Digital drive can exceed 5.5 V if input current is limited to 10 mA. Consult packaging section of databook for thermal limitations and considerations of package.

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $T_A$ = –55°C to +125°C for the UC1707, –25°C to +85°C for the UC2707, and 0°C to +70°C for the UC3707; $V_{IN}$ = $V_C$ = 20 V. $T_A$ = $T_J$.

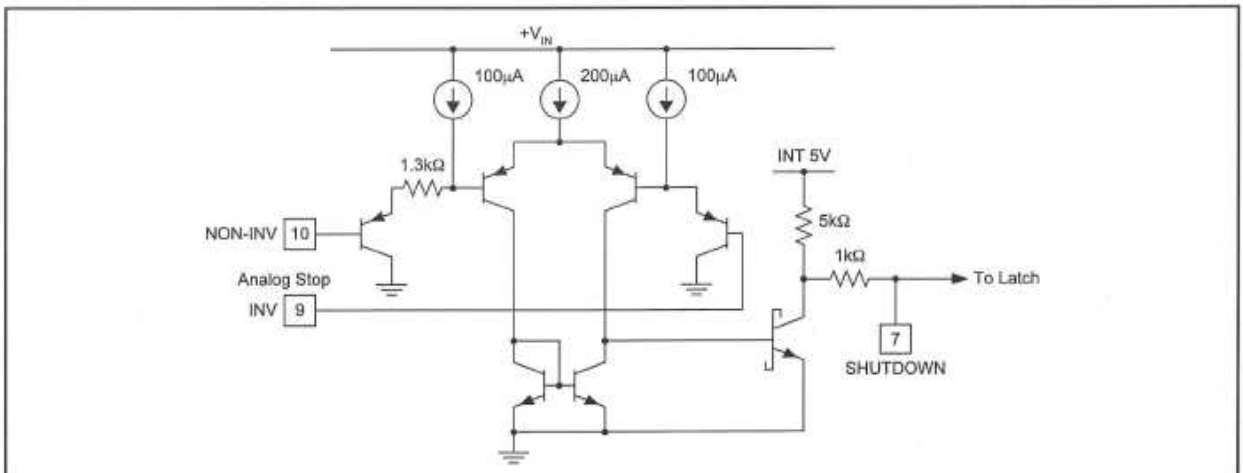
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Supply current | $V_{IN}$ = 40 V | | 12 | 15 | mA |
| $V_C$ | Supply current | $V_C$ = 40 V, outputs low | | 5.2 | 7.5 | mA |
| $V_C$ | Leakage current | $V_{IN}$ = 0, $V_C$ - 30 V, no load | | 0.05 | 0.1 | mA |
| | Digital input low level | | | | 0.8 | V |
| | Digital input high level | | 2.2 | | | V |
| | Input current | $V_I$ = 0 | | –0.06 | –1.0 | mA |
| | Input leakage | $V_I$ = 5 V | | 0.05 | 0.1 | mA |
| $V_C – V_O$ | Output high sat. | $I_O$ = –50 mA | | | 2.0 | V |
| | | $I_O$ = –500 mA | | | 2.5 | |
| $V_O$ | Output low sat. | $I_O$ = –50 mA | | | 0.4 | V |
| | | $I_O$ = –500 mA | | | 2.5 | |
| | Analog threshold | $V_{CM}$ = 0 to 15 V | 100 | 130 | 160 | mV |
| | Input bias current | $V_{CM}$ = 0 | | –10 | –20 | µA |
| | Thermal shutdown | | | 155 | | °C |
| | Shutdown threshold | Pin 7 input | 0.4 | 1.0 | 2.2 | V |
| | Latch disable threshold | Pin 3 input | 0.8 | 1.2 | 2.2 | V |

## TYPICAL SWITCHING CHARACTERISTICS

$V_{IN}$ = $V_C$ = 20 V, $T_A$ = 25°C. Delays measured to 10% output change.

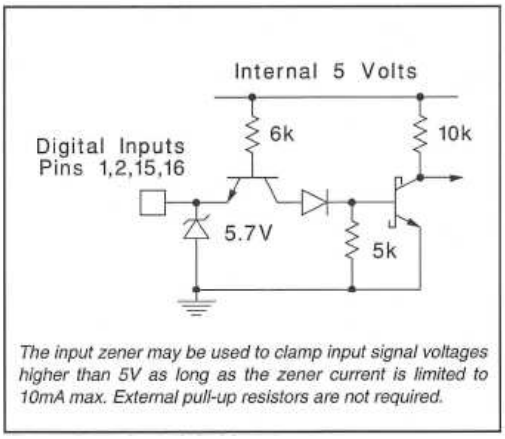
| PARAMETER | TEST CONDITIONS | OUTPUT CL = | | | UNIT |
|---|---|---|---|---|---|
| **From Inv. Input to Output** | | open | 1.0 | 2.2 | nF |
| Rise time delay | | 40 | 50 | 60 | ns |
| 10% to 90% rise | | 25 | 40 | 50 | ns |
| Fall time delay | | 30 | 40 | 50 | ns |
| 90% to 10% fall | | 25 | 40 | 50 | ns |
| **From N.I. Input to Output** | | | | | |
| Rise time delay | | 30 | 40 | 50 | ns |
| 10% to 90% rise | | 25 | 40 | 50 | ns |
| Fall time delay | | 45 | 55 | 65 | ns |
| 90% to 10% fall | | 25 | 40 | 50 | ns |
| $V_C$ cross-conduction current spike duration | Output rise | 25 | | | ns |
| | Output fall | 0 | | | ns |
| Analog shutdown delay | Stop non-Inv. = 0 V | 180 | | | ns |
| | Stop Inv. = 0 to 0.5 V | 180 | | | ns |
| Digital shutdown delay | 2 V input on Pin 7 | 50 | | | ns |

## SIMPLIFIED INTERNAL CIRCUITRY



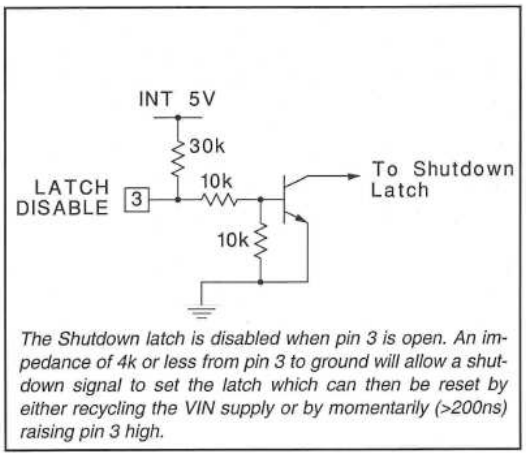

*The input common-mode voltage range is from ground to (VIN-3V). When not used both inputs shoul1d be grounded. Activate time is a function of overdrive with a typical value of 180ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low. Pulling shutdown low defeats the latch operation regardless of its status.*

**Figure 1. Typical Digital Input Gate**




*The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.*

**Figure 2. Typical Digital Input Gate**




*The Shutdown latch is disabled when pin 3 is open. An impedance of 4k or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the VIN supply or by momentarily (>200ns) raising pin 3 high.*

**Figure 3. Latch Disable**

## SIMPLIFIED INTERNAL CIRCUITRY (continued)

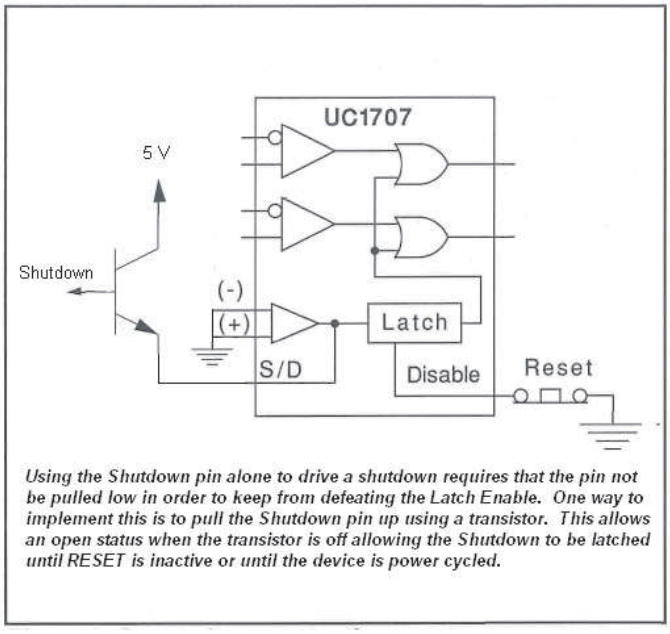



**Figure 4. Use of the Shutdown Pin**

### SHUTDOWN CIRCUIT DESCRIPTION

The function of the circuitry is to be able to provide a shutdown of the device. This is defined as functionality that will drive both outputs to the low state. There are three different inputs that govern this shutdown capability.

- Analog Stop Pins — The differential inputs to this comparator provide a way to execute a shutdown.
- Latch Disable Pin — Assuming that the Shutdown pin is left open, a high on this pin disables the latching functionality of the Analog Stop shutdown. A low on this pin enables the latching functionality of the Analog Stop shutdown. If a shutdown occurs through the Analog Stop circuit while Latch Disable is high, then the outputs will go low, but will return to normal operation as soon as the Analog Stop circuit allows it. If a shutdown occurs through the Analog Stop circuit while Latch Disable is low, then the outputs will go low and remain low even if the Analog Stop circuit no longer drives the shutdown. The outputs will remain "latched" low (in shutdown) until the Latch Disable goes high and the Analog Stop circuit allows it to return from shutdown or the VIN voltage is cycled to 0V and then returned above 5V.
- Shutdown Pin — This pin serves two purposes.
  1. It can be used as an output of the Analog Stop circuit.
  2. It can be used as an input to force a shutdown or to force the device out of shutdown. This pin can override both the Analog Stop circuit as well as the Latch Disable Pin. When driving hard logic levels into the Shutdown pin, the Latch Disable functionality will be overridden and the Latch Disable will not function as it does when used in conjunction with the Analog Stop circuit. When the Shutdown pin is high, the outputs will be in the low state (shutdown). When the Shutdown pin is low (hard logic low) the outputs will operate normally, regardless of the state of the Latch Disable pin or the Analog Stop pins.

In order to use the Shutdown Pin with the Latch Disable functional it is necessary to use either a diode in series with the Shutdown signal or to use an open collector pull-up so that the Shutdown pin is not pulled low. This configuration will allow the Latch Disable function to work with the Shutdown pin.

## SIMPLIFIED INTERNAL CIRCUITRY (continued)

### UG1707 SHUTDOWN TRUTH TABLE

| ANALOG STOP LOGIC | SHUTDOWN | LATCH DISABLE | PREVIOUS STATE OF OUTPUT | OUTPUT |
|---|---|---|---|---|
| X | 0 | X | X | Follows Input Logic |
| X | 1 | X | X | Low (Shutdown) |
| 1 | Open | X | X | Low (Shutdown) |
| 0 | Open | 0 | Shutdown | (1)Latched Shutdown |
| 0 | Open | 0 | Normal | Follows Input Logic |
| 0 | Open | 1 | X | Follows Input Logic |

(1) If the output was previously in Shutdown and Latch Disable was low and stays low, then even if the Analog Stop Logic is changed or the Shutdown pin is open, the outputs will remain in Shutdown.

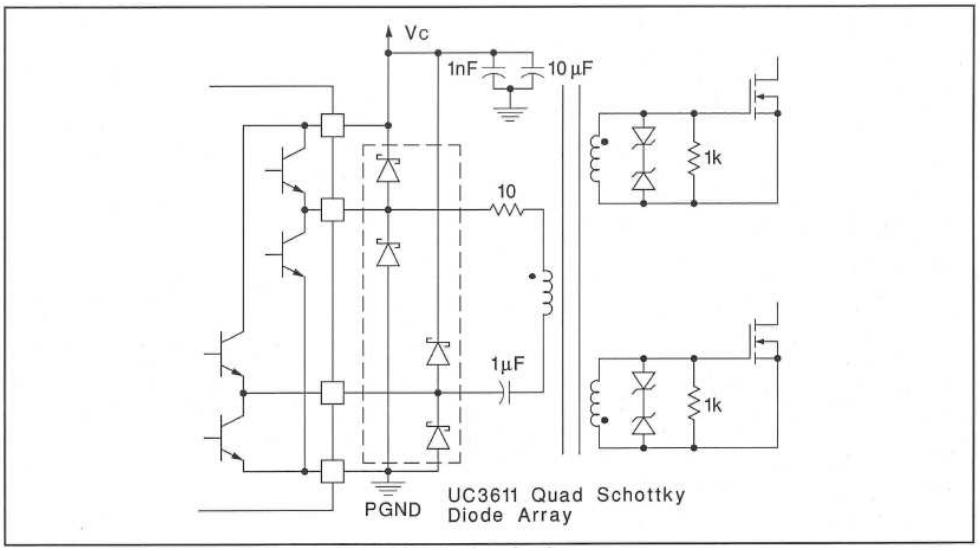



**Figure 5. Transformer Coupled Push-Pull MOSFET Drive Circuit**

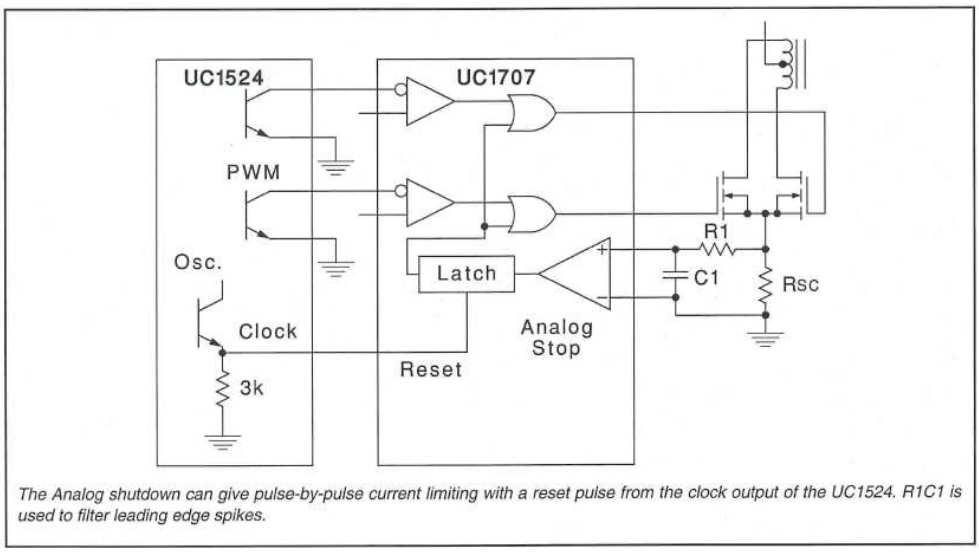
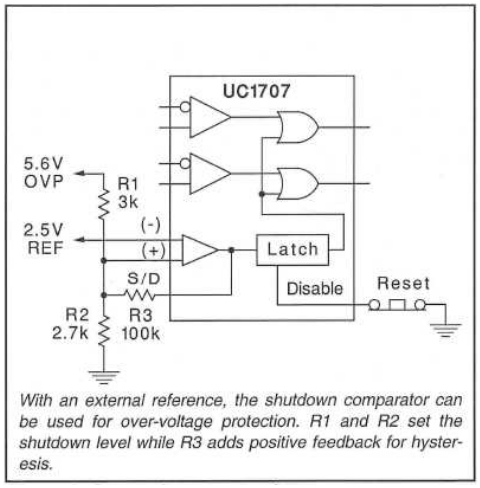
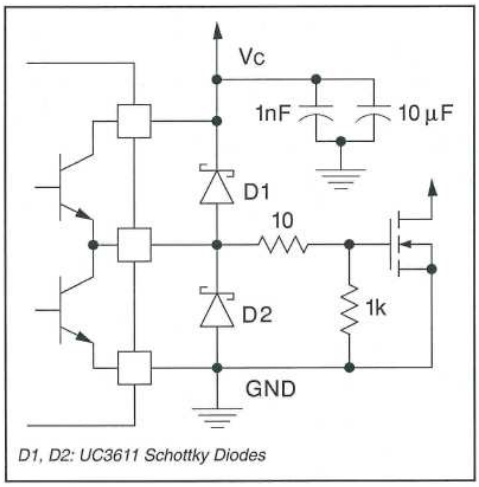



**Figure 6. Current Limiting**



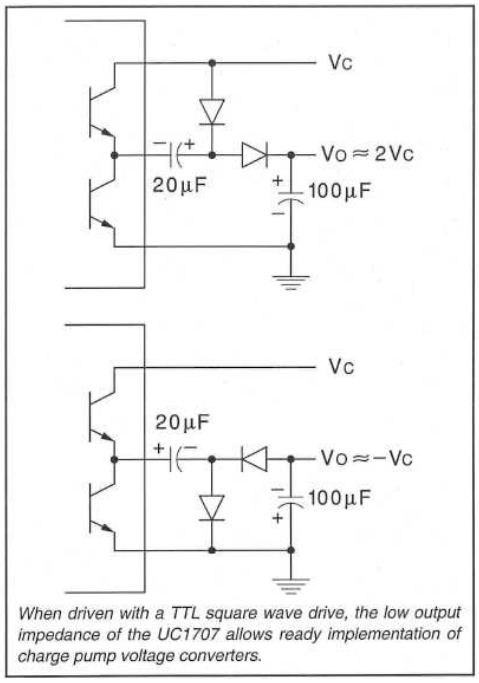

*With an external reference, the shutdown comparator can be used for over-voltage protection. R1 and R2 set the shutdown level while R3 adds positive feedback for hysteresis.*

**Figure 7. Over-Voltage Protection**




*D1, D2: UC3611 Schottky Diodes*

**Figure 8. Power MOSFET Drive Circuit**




*When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.*

**Figure 9. Charge Pump Circuits**

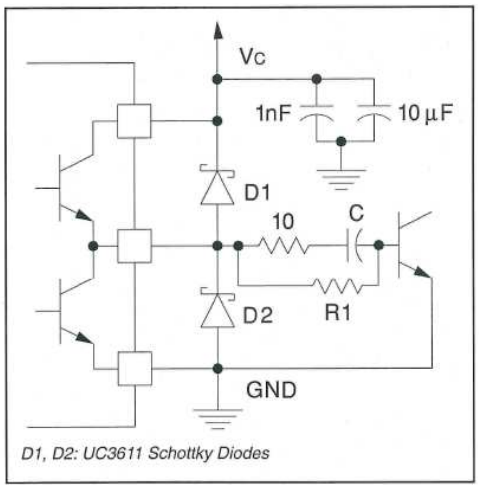



**Figure 10. Power Bipolar Drive Circuit**

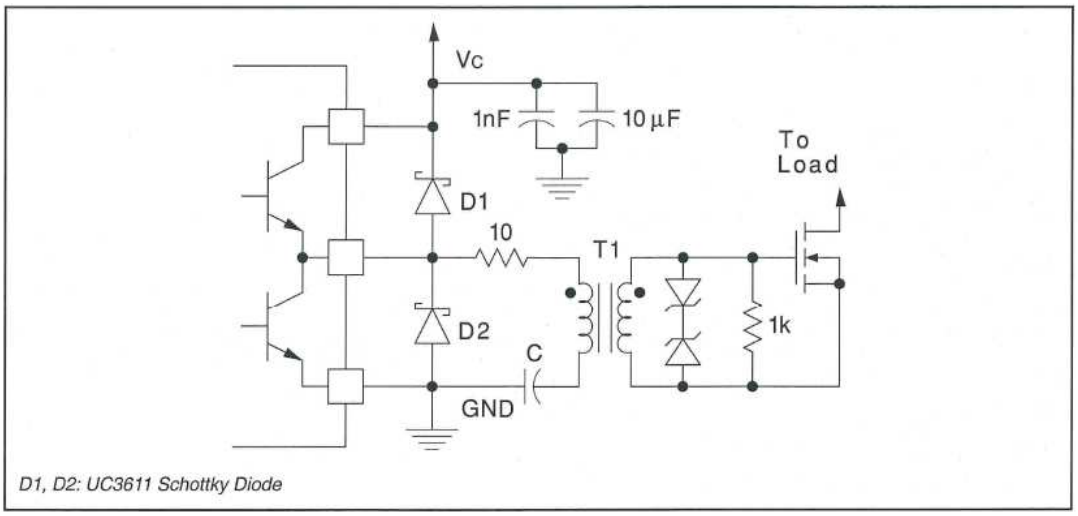



**Figure 11. Transformer Coupled MOSFET Drive Circuit**

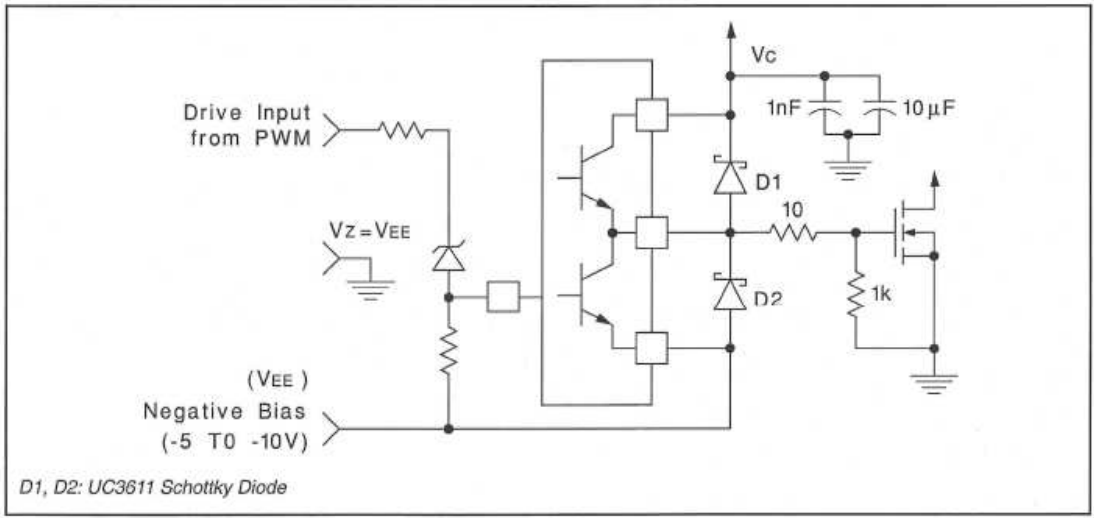



**Figure 12. Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Reference PWM**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-87619012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-87619012A UC1707L/ 81032 | Samples |
| 5962-8761901EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8761901EA UC1707J/80900 | Samples |
| 5962-8761901V2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-8761901V2A UC1707L QMLV | Samples |
| 5962-8761901VEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8761901VEA UC1707JQMLV | Samples |
| 5962-8761903VEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8761903VEA UC1707J-SP | Samples |
| 5962-8761903VFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8761903VFA UC1707W-SP | Samples |
| UC1707J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | UC1707J | Samples |
| UC1707J/80313 | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| UC1707J883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | UC1707J/883B | Samples |
| UC1707L | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | UC1707L | Samples |
| UC1707L883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | UC1707L/ 883B | Samples |
| UC2707DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2707DW | Samples |
| UC2707DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2707DW | Samples |
| UC2707DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2707DW | Samples |
| UC2707DWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2707DW | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2707N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | UC2707N | Samples |
| UC2707NG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | UC2707N | Samples |
| UC2707Q | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | UC2707Q | Samples |
| UC3707DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3707DW | Samples |
| UC3707DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3707DW | Samples |
| UC3707J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | 0 to 70 | UC3707J | Samples |
| UC3707N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3707N | Samples |
| UC3707NG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3707N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF UC1707, UC1707-SP, UC3707, UC3707M :**

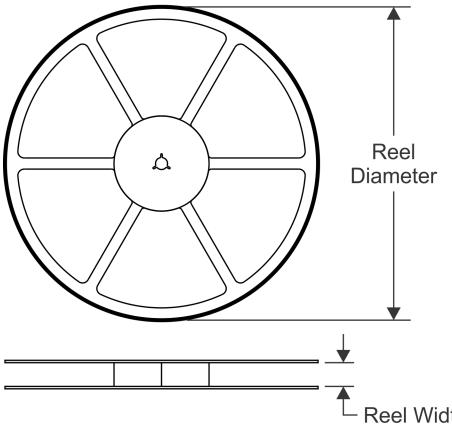
- Catalog: UC3707, UC1707, UC3707M, UC3707
- Military: UC1707
- Space: UC1707-SP

NOTE: Qualified Version Definitions:

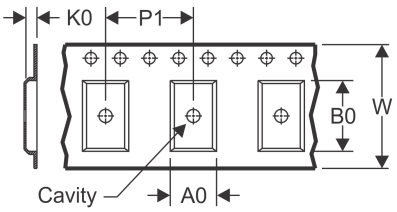
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

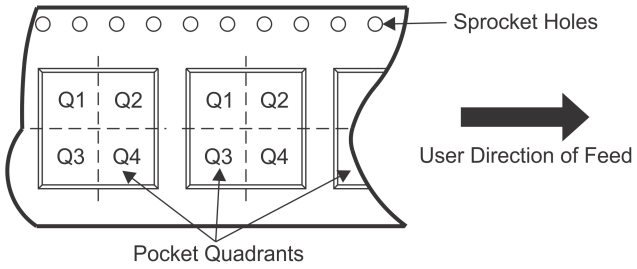



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

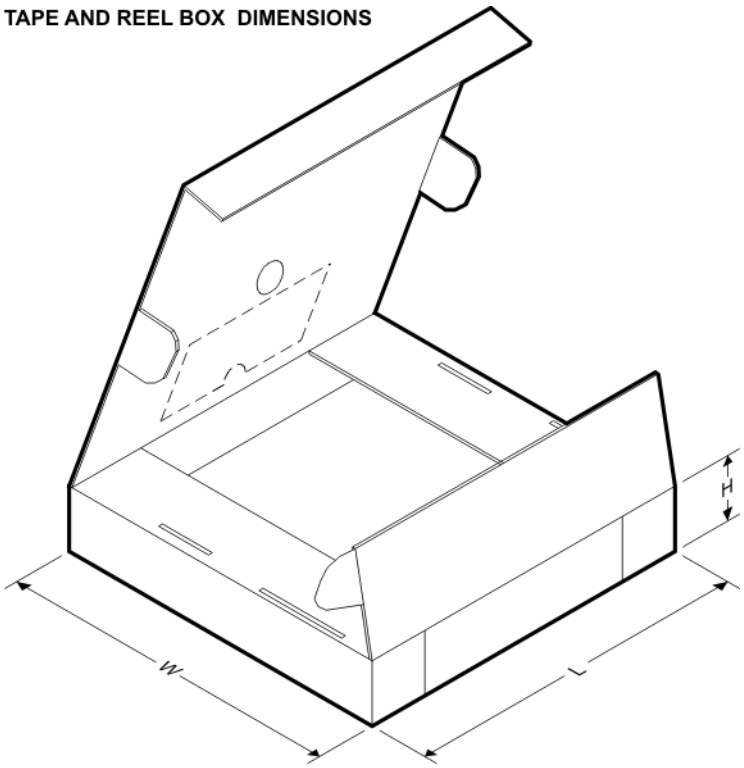
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2707DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3707DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2707DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| UC3707DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

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