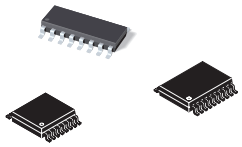


SLUS544E − SEPTEMBER 2003 − REVISED MARCH 2009

INTERLEAVED DUAL PWM CONTROLLER WITH PROGRAMMABLE MAX DUTY CYCLE

FEATURES

- **2-MHz High Frequency Oscillator with 1-MHz Operation Per Channel**
- **Matched Internal Slope Compensation Circuits**
- **Programmable Maximum Duty Cycle Clamp 60% to 90% Per Channel**
- **Peak Current Mode Control with Cycle-by-Cycle Current Limit**
- **Current Sense Discharge Transistor for Improved Noise Immunity**
- **Accurate Line Under and Over-Voltage Sense with Programmable Hysteresis**
- **Opto-Coupler Interface**
- **110-V Internal Start-Up JFET (UCC28221)**
- **Operates from 12-V Supply (UCC28220)**
- **Programmable Soft-Start**

APPLICATIONS

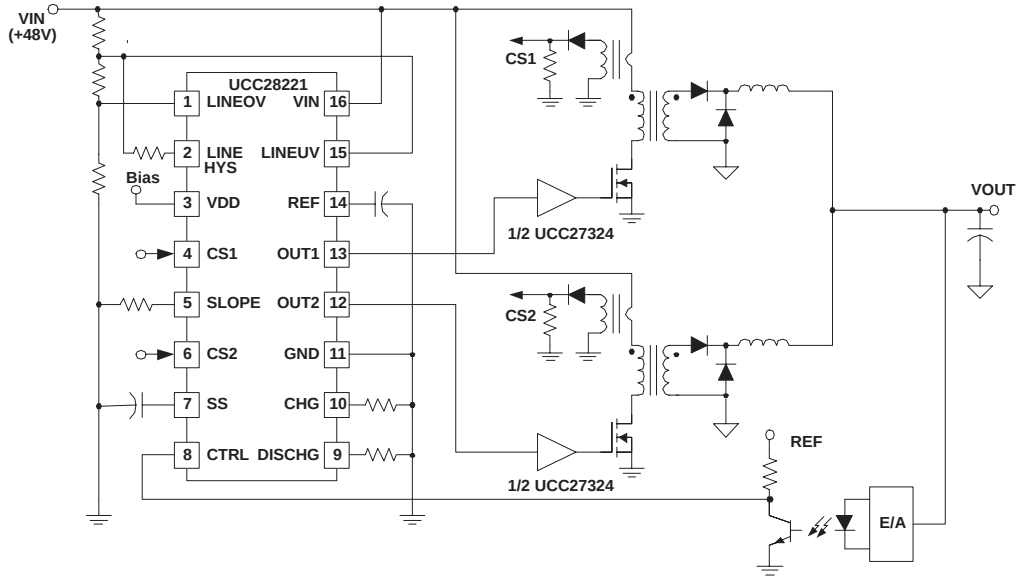
- **High Output Current (50-A to 100-A) Converters**
- **Maximum Power Density Designs**
- **High Efficiency 48-V Input with Low Output Ripple Converters**
- **High Power Offline, Telecom and Datacom Power Supplies**

DESCRIPTION

The UCC28220 and UCC28221 are a family of BiCMOS interleaved dual channel PWM controllers. Peak current mode control is used to ensure current sharing between the two channels. A precise maximum duty cycle clamp can be set to any value between 60% and 90% duty cycle per channel.

UCC28220 has an UVLO turn-on threshold of 10 V for use in 12-V supplies while UCC28221 has a turn-on threshold of 13 V for systems needing wider UVLO hysteresis. Both have 8-V turn-off thresholds.

TYPICAL APPLICATION



NOTE: Pin 16 is a no connect (N/C) on UCC28220 which does not include the JFET option.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION (CONTINUED)

Additional features include a programmable internal slope compensation with a special circuit which is used to ensure exactly the same slope is added to each channel and a high voltage 110-V internal JFET for easier startup for the wider hysteresis UCC28221 version.

The UCC28220 is available in both 16-pin SOIC and low-profile TSSOP packages. The UCC28221 also comes in 16-pin SOIC package and a slightly larger 20-pin TSSOP package to allow for high voltage pin spacing to meet UL1950 creepage clearance safety requirements.

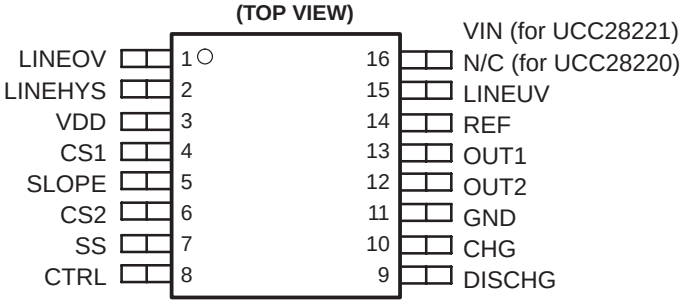
ORDERING INFORMATION

TEMPERATURE RANGE $T_A = T_J$	UVLO THRESHOLDS	110-V HV JFET STARTUP CIRCUIT	PACKAGED DEVICES		
			SOIC−16 (D)	TSSOP-16 (PW)	TSSOP-20 (PW)
−40°C to +105°C	10 V on / 8 V off	NO	UCC28220D	UCC28220PW	−
	13 V on / 8 V off	YES	UCC28221D	−	UCC28221PW

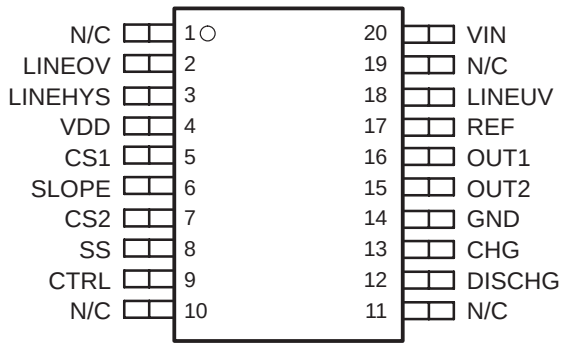
NOTE: D (SOIC) and PW (TSSOP) packages are available taped and reeled. Add R suffix to device type, e.g. UCC28220DR or UCC28221PWR. The reel quanities are 2,500 devices per reel for D package and 2,000 devices per reel for the PW package.

CONNECTION DIAGRAM

UCC28220D, UCC28220PW and UCC28221D PACKAGE (TOP VIEW)



UCC28221PW PACKAGE (TOP VIEW)



RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Condition
High voltage start-up input	V_{IN}	36 V to 76 V
Supply voltage	V_{DD}	8.4 V to 14.5 V

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)†‡

Parameter	UCC2822X	UNIT
High voltage start-up input, V_{IN}	110	V
Supply voltage, V_{DD}	15	V
Output current (OUT1, OUT2) dc , $I_{OUT(dc)}$	±10	mA
OUT1/ OUT2 capacitive load	200	pF
REF output current, I_{REF}	10	mA
Current sense inputs, CS1, CS2	−1.0 to 2.0	V
Analog inputs (CHG, DISCHG, SLOPE, REF, CNTRL)	−0.3 to 3.6	V
Analog inputs (SS, LINEOV, LINEUV, LINEHYS)	−0.3 to 7.0	V
Power dissipation at T_A = 25°C (PW package)	400	mW
Power dissipation at T_A = 25°C (D package)	650	mW
Junction operating temperature, T_J	−55 to 150	°C
Storage temperature, T_{stg}	−65 to 150	°C
Lead temperature (soldering, 10 sec.), Tsol	300	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute−maximum−rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

ELECTRICAL CHARACTERISTICS:

V_{DD} = 12 V, 0.1-µF capacitor from VDD to GND, 0.1-µF capacitor from REF to GND, F_{OSC} = 1 MHz, T_A = −40°C to 105°C, T_A = T_J, (unless otherwise noted).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Overall Section					
Operating VDD range		8.4		14.5	V
Quiescent current	SS = 0 V, no switching, Fosc = 1 MHz	1.5	3	4	mA
Operating current	Outputs switching, Fosc = 1 MHz	1.6	3.5	6	
Startup Section					
Startup current	UCC28220 VDD < (UVLO−0.8)			200	µA
UVLO start threshold	UCC28220	9.5	10	10.5	V
UVLO start threshold	UCC28221	12.3	13	13.7	
UVLO stop threshold		7.6	8	8.4	
UVLO hysteresis	UCC28220	1.8	2	2.2	V
UVLO hysteresis	UCC28221	4.8	5	5.2	V
JFET ON threshold	SS = 0, outputs not switching, VDD decreasing	9.5	10	10.5	
JFET ON threshold	SS = 2 V,Cntrl = 2 V, output switching, VDD decreasing; same threshold as UVLO stop	7.6	8	8.4	
High voltage JFET current	VIN = 36 V to 76 V, VDD = 0 V	16	48	100	mA
High voltage JFET current	VIN = 36 V to 76 V, VDD = 10 V	4	16	40	
High voltage JFET current	VIN = 36 V to 76 V, VDD < UVLO	4	12	40	
JFET leakage	VIN = 36 V to 76 V, VDD = 14 V			100	µA

ELECTRICAL CHARACTERISTICS:

V_{DD} = 12 V, 0.1-µF capacitor from VDD to GND, 0.1-µF capacitor from REF to GND, F_{OSC} = 1 MHz, T_A = −40°C to 105°C, $T_A = T_J$, (unless otherwise noted).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference					
Output voltage	8 V < VDD < 14 V, ILOAD=0 mA to −10 mA	3.15	3.3	3.45	V
Output current	Outputs not switching; CNTRL = 0 V	10			mA
Ouput short circuit current	V_{REF} = 0 V	−40	−20	−10	mA
V_{REF} UVLO		2.55	3	3.25	V
Soft-Start					
SS charge current	RCHG=10.2 kΩ, SS = 0 V	−70	−100	−130	µA
SS discharge current	RCHG=10.2 kΩ, SS = 2 V	70	100	130	
SS initial voltage	LINEOV=2 V, LINEUV = 0 V	0.5	1	1.5	V
SS voltage at 0% dc	Point at which output starts switching	0.5	1.2	1.8	
SS voltage ratio		75%	90%	100%	
SS Max voltage	LINEOV = 0 V, LINEUV = 2 V	3	3.5	4	V
Oscillator and PWM					
Output frequency	RCHG = 10.2 kΩ, RDISCHG = 10.2 kΩ	450	500	550	kHz
Oscillator frequency	RCHG = 10.2 kΩ, RDISCHG = 10.2 kΩ	900	1000	1100	
Output maximum duty cycle	RCHG = 10.2 kΩ, RDISCHG = 10.2 kΩ, measured at OUT1 and OUT2	73%	75%	77%	%
CHG voltage		2	2.5	3	V
DISCHG voltage		2	2.5	3	
Slope Compensation					
Slope	RSLOPE = 75 kΩ, RCH = 66 kΩ, RDISCHG = 44 kΩ, Csx = 0 V to 0.5 V	140	200	260	mV/us
Channel matching	RSLOPE = 75 kΩ, Csx = 0 V		0%	10%	
Current Sense					
CS1, CS2 bias current	CS1 = 0, CS2 = 0	−500	0	500	nA
Prop delay CSx to OUTx	CSx input 0 V to 1.5 V step		40	85	ns
CS1, CS2 sink current	CSx = 2 V	2.3	4.5	7	mA
CNTRL Section					
Resistor ratio(1)			0.6		
Ctrl input current	CTRL = 0 V and 3.3 V	−100	0	100	nA
Ctrl voltage at 0% dc	CSx = 0 V, Point at which output starts switching (checks resistor ratio)	0.5	1.2	1.8	V

NOTES: (1). Ensured by design. Not 100% tested in production.

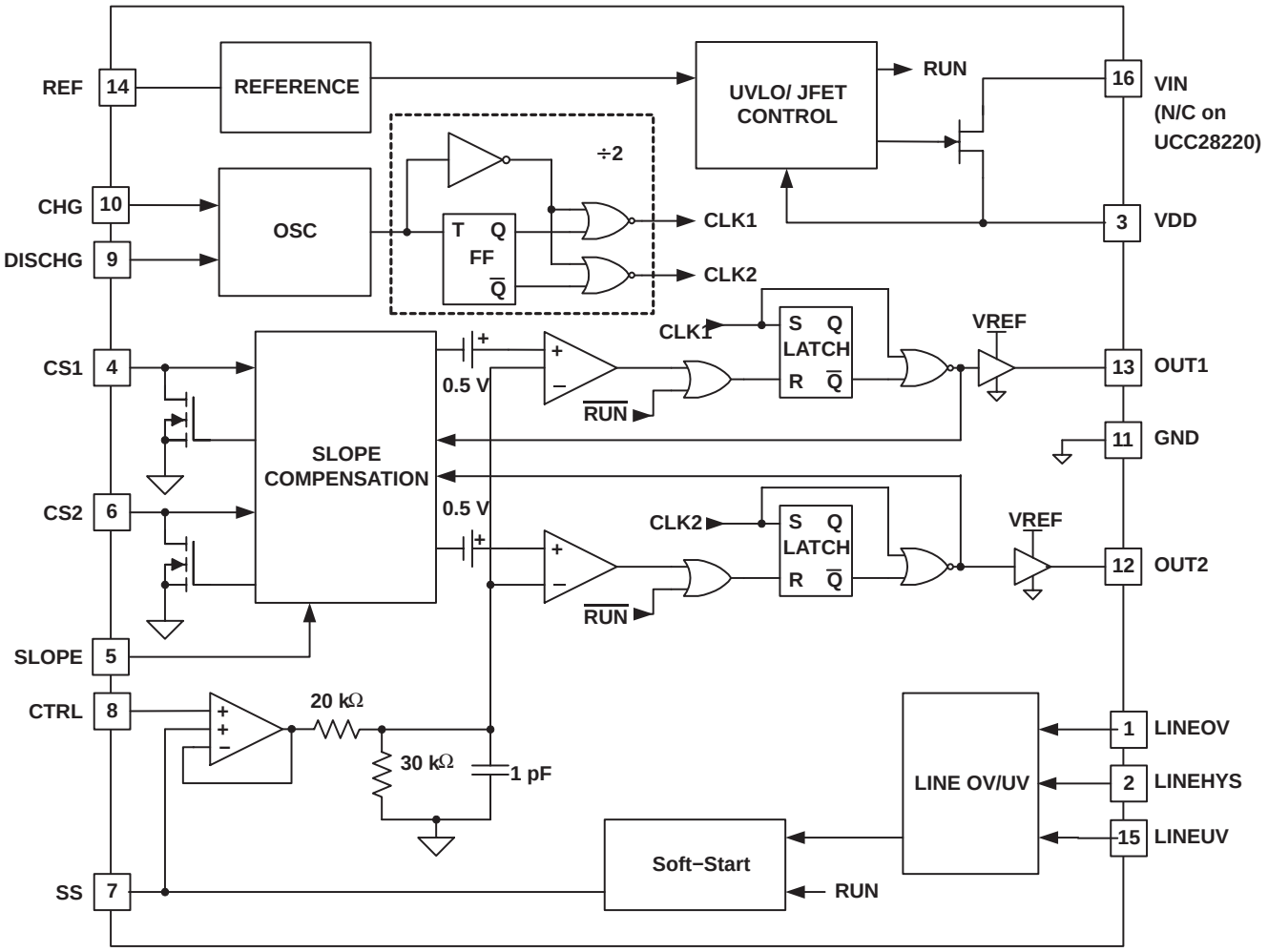
ELECTRICAL CHARACTERISTICS:

V_{DD} = 12 V, 0.1-µF capacitor from VDD to GND, 0.1-µF capacitor from REF to GND, F_{OSC} = 1 MHz, T_A = −40°C to 105°C, $T_A = T_J$, (unless otherwise noted).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Section (OUT1, OUT2)					
Low level	I_{OUT} = 10 mA		0.4	1	V
High level	I_{OUT} = −10 mA, VREF – VOUT		0.4	1	
Rise time	C_{LOAD} = 50 pF		10	20	ns
Fall time	C_{LOAD} = 50 pF		10	20	
LINE Sense section					
LINEOV threshold	T_A = 25°C	1.240	1.260	1.280	V
LINEOV threshold	T_A =−40°C to 105°C	1.235	1.260	1.285	
LINEUV threshold	T_A = 25°C	1.240	1.260	1.280	
LINEUV threshold	T_A =−40°C to 105°C	1.235	1.260	1.285	
LINEHYST pull up voltage	LINEOV = 2 V, LINEUV = 2 V	3.1	3.25	3.4	
LINEHYST off leakage	LINEOV = 0 V, LINEUV = 2 V	−500	0	500	nA
LINEHYS pull-up resistance	I = −20 µA		100	500	Ω
LINEHYS pull-down resistance	I = 20 µA		100	500	
LINEOV, LINEUV bias I	LINEOV = 1.25 V, LINEUV = 1.25 V	−500		500	nA

NOTES: (1). Ensured by design. Not 100% tested in production.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Pinout for 16 pin option shown. See the 20-pin connection to UCC28221PW in the *Terminal Functions* table on the next page.

Terminal Functions

TERMINAL			NAME	I/O	FUNCTION
PIN NUMBER					
UCC28220D UCC28220PW	UCC28221D	UCC28221PW			
1	1	2	LINEOV	I	Input for line over voltage comparator
2	2	3	LINEHYS	I	Sets line comparator hysteresis
3	3	4	VDD	I	Device supply input
4	4	5	CS1	I	Channel 1 current sense input
5	5	6	SLOPE	I	Sets slope compensation
6	6	7	CS2	I	Channel 2 current sense input
7	7	8	SS	I	Soft-start input
8	8	9	CTRL	I	Feedback control input
9	9	12	DISCHG	I	Sets oscillator discharge current
10	10	13	CHG	I	Sets oscillator charge current
11	11	14	GND	−	Device ground
12	12	15	OUT2	O	PWM output from channel 2
13	13	16	OUT1	O	PWM output from channel 1
14	14	17	REF	O	Reference voltage output
15	15	18	LINEUV	I	Input for line under voltage comparator
−	16	20	VIN	I	High voltage start-up input
16	−	1, 10, 11, 19	N/C	−	No connection

PIN DESCRIPTIONS

VDD: This is used to supply power to the device, monitoring this pin is a the UVLO circuit. This is used to insure glitch-free startup operation. Until VDD reaches its UVLO threshold, it remains in a low power mode, drawing approximately 150 μA of current and forcing pins, SS, CS1, CS2, OUT1, and OUT2 to logic 0 states. If the VDD falls below 8 V after reaching turn-on, it will go back into this low power state. In the case of the UCC28221, the UVLO threshold is 13 V. It is 10 V for the UCC28220. Both versions have a turn-off threshold of 8 V.

VIN (UCC28221 only): This pin has an internal high voltage JFET used for startup. The drain is connected to VIN, while its' source is connected to VDD. During startup, this JFET delivers 12 mA typically with a minimum of 4 mA to VDD, which in turn, charges up the VDD bypass capacitor. When VDD gets to 13 V, the JFET is turned off.

CS1 and CS2: These 2 pins are the current sense inputs to the device. The signals are internally level shifted by 0.5 V before the signal gets to the PWM comparator. Internally the slope compensation ramp is added to this signal. The linear operating range on this input is 0 to 1.5 V. Also, this pin gets pulled to ground each time its respective output goes low. (ie: OUT1 and OUT2).

SLOPE: This pin sets up a current used for the slope compensation ramp. A resistor to ground sets up a current, which is internally divided by 25 and then applied to an internal 10-pF capacitor. Under normal operation th dc voltage on this pin is 2.5 V..

SS: A capacitor to ground sets up the soft-start time for the open loop soft-start function. The source and sink current from this pin is equal to 3/7th of the oscillator charge current set by the resistor on the CHG pin. The soft start capacitor is held low during UVLO and during a Line OV or UV condition. Once an OV or UV fault occurs, the soft-start capacitor is discharged by a current equal to its charging current. The capacitor does NOT quickly discharge during faults. In this way, the controller has the ability to recover quickly from very short line transients. This pin can also be used as an Enable/Disable function.

CHG: A resistor from this pin to GND sets up the charging current of the internal C_T capacitor used in the oscillator. This resistor, in conjunction with the resistor on the DISCHG pin is used to set up the operating frequency and maximum duty cycle. Under normal operation the dc voltage on this pin is 2.5 V.

DISCHG: A resistor from this pin to GND sets up the discharge current of the internal C_T capacitor used in the oscillator. This resistor, in conjunction with the resistor on the CHG pin is used to set up the operating frequency and maximum duty cycle. Under normal operation the dc voltage on this pin is 2.5 V.

OUT1 and OUT2: These output buffers are intended to interface with high current MOSFET drivers. The output drive capability is approximately 33 mA and has an output impedance of 100 Ω. The outputs swing between GND and REF.

LINEOV: This pin is connected to a comparator and used to monitor the line voltage for an over voltage condition. The typical threshold is 1.26 V.

LINEUV: This pin is connected to a comparator and used to monitor the line voltage for an under voltage condition. The typical threshold is 1.26 V.

LINEHYST: This pin is controlled by both the LINEOV and LINEUV pins. It is used to control the hysteresis values for both the over and under voltage line detectors.

REF: REF is a 3.3-V output used primarily as a source for the output buffers and other internal circuits. It is protected from accidental shorts to ground. For improved noise immunity it is recommended that the reference pin be bypassed with a minimum of 0.1 µF of capacitance to GND.

APPLICATION INFORMATION

General

The device is comprised of several housekeeping blocks as well as two slope compensated PWM channels that are interleaved. The circuit is intended to run from an external VDD supply voltage between 8 V and 14 V, however, the UCC28221 has the addition of a high voltage startup JFET with control circuitry which can be used for system startup. Other functions contained in the device are supply UVLO, 3.3-V reference, accurate line OV and UV functions, a high speed programmable oscillator for both frequency and duty cycle, programmable slope compensation, and programmable soft start functions.

The UCC28220/1 is a primary side controller for a two channel interleaved power converter. The device is compatible with forward or flyback converters as long as a duty cycle clamp between 60 and 90 percent is required. The active clamp forward and flyback converters as well as the RCD and resonant reset forward converters are therefore compatible with this device. To ensure the two channels share the total converter output current, current mode control with internal slope compensation is used. Slope compensation is user programmable via a dedicated pin and can be set over a 50:1 range, ensuring good small-signal stability over a wide range of applications.

APPLICATION INFORMATION

LINE Over Voltage and Under Voltage

Three pins are provided to turn-off the output drivers and reset the soft-start capacitor when the converter input voltage is outside a prescribed range. The under-voltage set point and under-voltage hysteresis are accurately set via external resistors. The over-voltage set point is also accurately set via a resistor ratio, but the hysteresis is fixed by the same resistor that sets the u*nder-voltage hysteresis.

Figure 1 and 2 show detailed functional diagram and operation of the under voltage lockout (UVLO) and over-voltage lockout (OVLO) features. The equations for setting the thresholds defined in Figure 2 are:

$$V1 = 1.26 \times \frac{R1}{(R2 + R3)} + 1.26 \quad (1)$$

$$V2 = 1.26 \times \frac{(R1 + Rx)}{Rx}, \text{ where } Rx = R4 \parallel (R2 + R3) \quad (2)$$

$$V4 = 1.26 \times \frac{(R1 + R2 + R3)}{R3} \quad (3)$$

$$V3 = V4 - 1.26 \times \left(\frac{R1}{R4}\right) \quad (4)$$

The UVLO hysteresis and the OVLO hysteresis can then be calculated as V2 − V1 and V4 − V3, respectively. By examining the design equations it becomes apparent that the value of R4 sets the amount of hysteresis at both thresholds. By realizing this fact, the designer can then set the value of R4 based on the most critical hysteresis specification either at high line or at low line. In most designs the value of R4 will be determined by the desired amount of hysteresis around the UVLO threshold. As an example consider a telecom power supply with the following input UVLO and OVLO design specifications:

- V1 = 32.0 V
- V2 = 34.0 V
- V3 = 83.0 V
- V4 = 84.7 V

Then,

- R1 = 976 kΩ
- R2 = 24.9 kΩ
- R3 = 15.0 kΩ

and

- R4 = 604 kΩ

APPLICATION INFORMATION

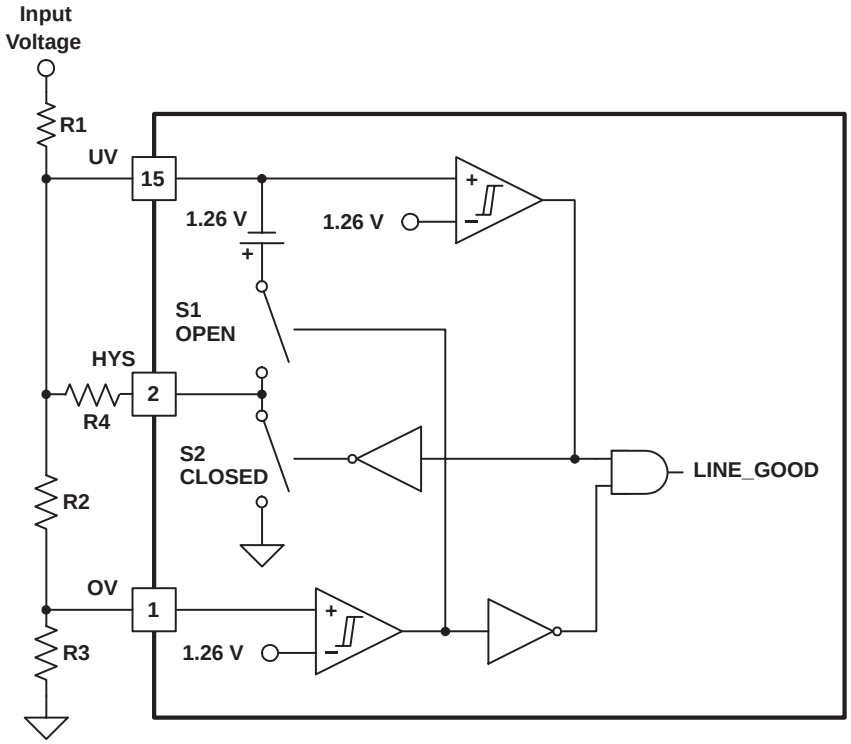


Figure 1. Line UVLO and OVLO Functional Diagram

Figure 2. Line UVLO and OVLO Operation

VDD

Because the driver output impedance is high the energy storage requirements on the VDD capacitor is low. For improved noise immunity it is recommended that the VDD pin, be bypassed with a minimum of 0.1 μF of capacitance to GND. In most typical applications the bias voltage for the MOSFET drivers will also be used as the VDD supply voltage for the chip. In the aforementioned applications it is beneficial to add a low valued resistor between the bulk storage capacitor of the driver and the VDD capacitor for the UCC28220/1. By adding a resistor in series with the bias supply any noise that is present on the bias supply will be filtered out before getting to the VDD pin of the controller.

APPLICATION INFORMATION

Reference

For improved noise immunity it is recommended that the reference pin, REF, be bypassed with a minimum of 0.1uF of capacitance to GND.

Oscillator Operation and Maximum Duty Cycle Setpoint

The oscillator uses an internal capacitor to generate the time base for both PWM channels. The oscillator is programmable over a 200 kHz to 2MHz frequency range with 20% to 80% maximum duty cycle range. Both the dead time and the frequency of the oscillator are divided by 2 to generate the PWM clock and off-time information for each of the outputs. In this way, a 20% oscillator duty cycle corresponds to a 60% maximum duty cycle at each output, where an 80% oscillator duty cycle yields a 90% duty cycle clamp at each output.

The design equations for the oscillator and maximum duty cycle set point are given by:

$$F_{OSC} = 2 \times F_{OUT} \tag{5}$$

$$D_{MAX(osc)} = 1 - 2 \times \left(1 - D_{MAX(out)}\right) \tag{6}$$

$$R_{CHG} = K_{OSC} \times \frac{D_{MAX(osc)}}{F_{OSC}} \tag{7}$$

$$R_{DISCHG} = K_{OSC} \times \frac{\left(1 - D_{MAX(osc)}\right)}{F_{OSC}} \tag{8}$$

Where:

- K_{OSC} = 2.04 x 10^{10} [Ω/s]
- F_{OUT} = Switching frequency at the outputs of the chip [Hz]
- $D_{MAX(out)}$ = Maximum duty cycle limit at the outputs of the chip
- $D_{MAX(osc)}$ = Maximum duty cycle of the Oscillator for the desired maximum duty cycle at the outputs
- F_{OSC} = Oscillator frequency for desired output frequency [Hz]
- R_{CHG} = External oscillator resistor which sets the charge current − [Ω]
- R_{DISCHG} = External oscillator resistor which sets the discharge current − [Ω]

Start-Up JFET Section

A 110-V start-up JFET is included to start the device from a wide range (36 V−75 V) telecom input source. When VDD is lower than 13 V the JFET is on, behaving as a current source charging the bias capacitors on VDD and supplying current to the device. In this way, the VDD bypass capacitors are charged to 13 V where the outputs start switching and the JFET is turned off. To enable a constant bias supply to the device during a pulse skipping condition, the JFET is turned back on whenever VDD decreases below 10 V and the outputs are not switching. Thus, the current from the JFET can overcome the internal bias currents, as long as the device is not actively switching the output drivers. See Figure 2 below for a graphical representation of the JFET/VDD operation. The UCC28220 does not contain an internal JFET and has a startup threshold of 10 V which makes it capable of directly operating off a 12 V dc bus

APPLICATION INFORMATION

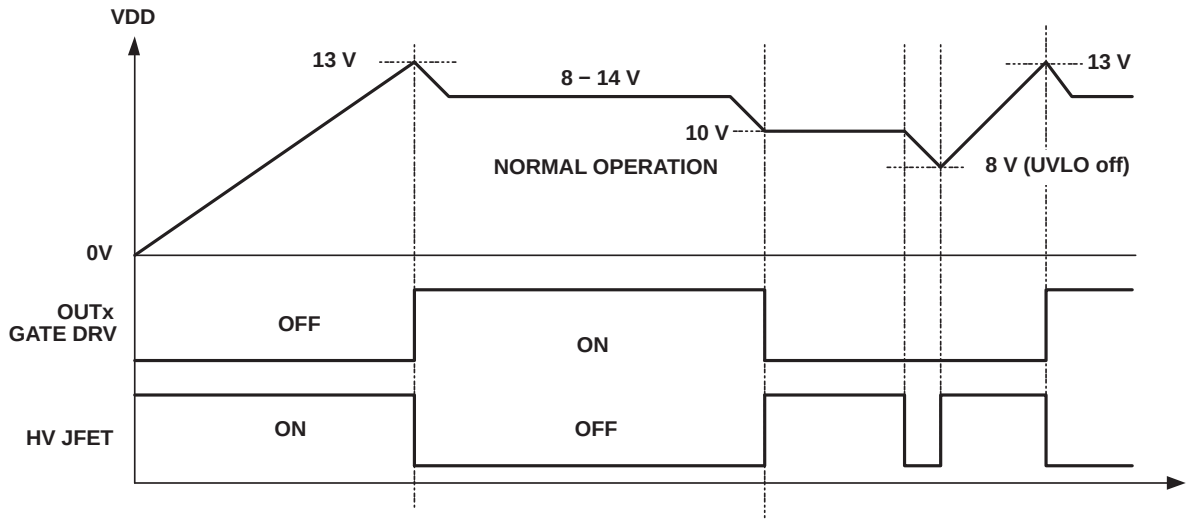


Figure 3. JFET Device Operation with VDD Voltage

Soft-Start

A current is forced out of the SS pin, equal to 3/7 of the current set by R_{CHG}, to provide a controlled ramp voltage. The current set by the R_{CHG} resistor is equal to 2.5 V divided by R_{CHG}. This ramp voltage overrides the commanded duty cycle on the CTRL pin, allowing a controlled start-up. Assuming the UCC28221 is biased on the primary side, the soft start should be quite quick to allow the secondary bias to be generated and the secondary side control can then take over. Once the soft-start time interval is complete, a closed loop soft-start on the secondary side can be executed.

$$ISS = \frac{3}{7} \times \frac{2.5}{R_{CHG}} \tag{9}$$

where,

ISS = current which is sourced out of the SS pin during the soft-start time − [Amps]

Current Sense

The current sense signals CS1 and CS2 are level shifted by 0.5 V and have the slope compensation ramps added to them before being compared to the control voltage at the input of the PMW comparators. The amplitude of the current sense signal at full load should be selected such that it is very close to the maximum control voltage in order to limit the peak output current during short circuit operation.

Output Drivers

The UCC28220/1 is intended to interface with the UCC27323/4/5 family of MOSFET drivers. As such, the output drive capability is low, effectively 100 Ω and the driver outputs swing between GND and REF.

APPLICATION INFORMATION

Slope Compensation

The slope compensation circuit in the UCC28220/1 operates on a cycle-by-cycle basis. The two channels have separate slope compensation circuits. These are fabricated in precisely the same way so as current sharing is unaffected by the slope compensation circuit. For each channel, an internal capacitor is reset whenever that channel's output is off. At the beginning of the PWM cycle, a current is mirrored off the SLOPE pin into the capacitor, developing an independent ramp. Since the two channel's ramps will start when the channel's output changes from a low to high state, the ramps are thus interleaved. These internal ramps are added to the voltages on the current sense pins, CS1 and CS2 and the result forms an input to the PWM comparators.

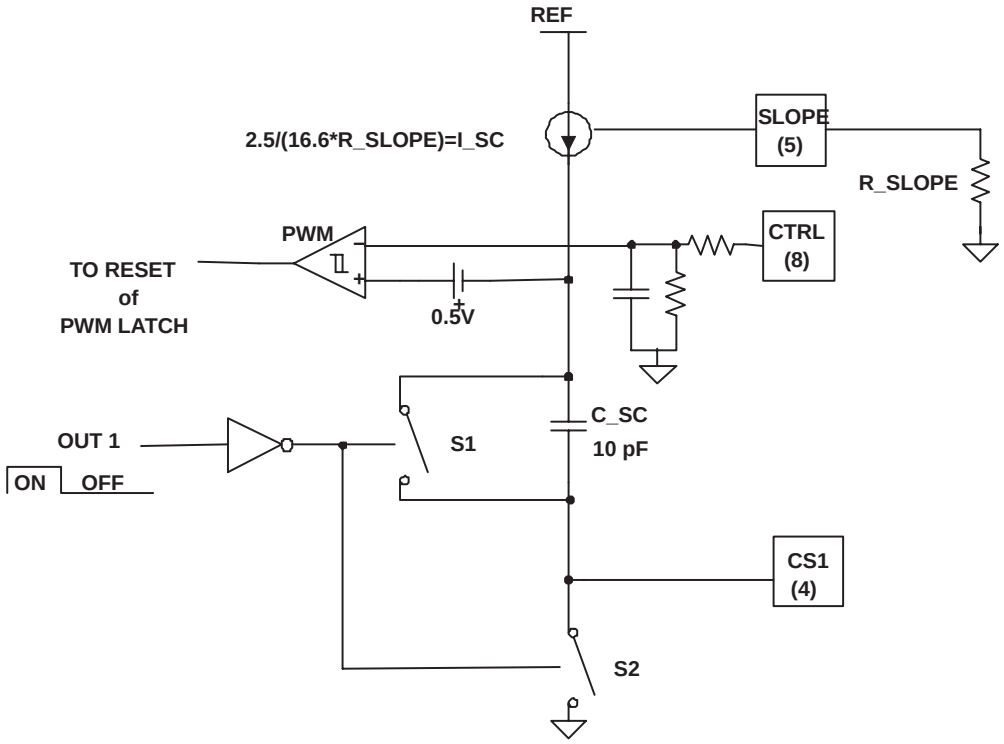


Figure 4. Slope Compensation Detail for Channel 1. Duplicate Matched Circuitry Exists for Channel 2.

To ensure stability, the slope compensation circuit must add between 1/5 and 1 times the inductor downslope to each of the current sense signals prior to being applied to the PWM comparator's input.

APPLICATION INFORMATION

Determining the value for the slope compensation resistor:

Design Example:

$N_{CT(p)} = 1$	$V_{OUT} = 12$	$Np = 7$	$R_{SENSE} = 5.23$	$F_{S(out)} = 500000$
$N_{CT(s)} = 50$	$L_{OUT} = 3.2 \times 10^{-6}$	$Ns = 5$	$V_{EA(cl)} = 1.98$	

Where,

- $N_{CT(p)}$ = Number of primary turns on the Current Transformer − [Turns]
- $N_{CT(s)}$ = Number of Secondary turns on the current transformer − [Turns]
- V_{OUT} = Nominal output voltage of the converter − [V]
- L_{OUT} = Inductance value of each output inductor − [H]
- N_P = Number of primary turns on the main transformer − [Turns]
- N_S = Number of secondary turns on the main transformer − [Turns]
- R_{SENSE} = Value of current sense resistor on secondary of current sense transformer − [Ohms]
- $V_{EA(cl)}$ = Maximum Value of the E/A output voltage − [Volts]
- $F_{S(out)}$ = Switching frequency of each output − [Hz]

Determine the correct value for the slope resistor, R_{SLOPE}, to provide the desired amount of slope compensation.

$$N_{CT} = \frac{N_{CT(p)}}{N_{CT(s)}}, \text{ Current Transformer Turns Ratio}$$

1. Transform the Secondary Inductor Downslope to the Primary

$$S_{L(prime)} = \frac{V_{OUT}}{L_{OUT}} \times \frac{N_s}{N_p}, \quad S_{L(prime)} = 2.679 \text{ A}/\mu\text{s}$$

2. Calculate the Transformed Slope Voltage at Sense Resistor:

$$VS_{L(prime)} = S_{L(prime)} \times N_{CT} \times R_{SENSE}, \quad VS_{L(prime)} = 0.2802 \text{ V}/\mu\text{s}$$

3. Calculate the R_{SLOPE} value to give a compensating ramp equal to the transformed slope voltage given above.:

$M = 1.0$

Desired ratio between the compensating ramp and the output inductor downslope ramp, transformed to the primary sense resistor

$$R_{SLOPE} = \frac{10^4}{\left(M \times VS_{L(prime)}\right)}, \quad R_{SLOPE} = 35.69 \text{ k}\Omega$$

TYPICAL APPLICATION CIRCUITS

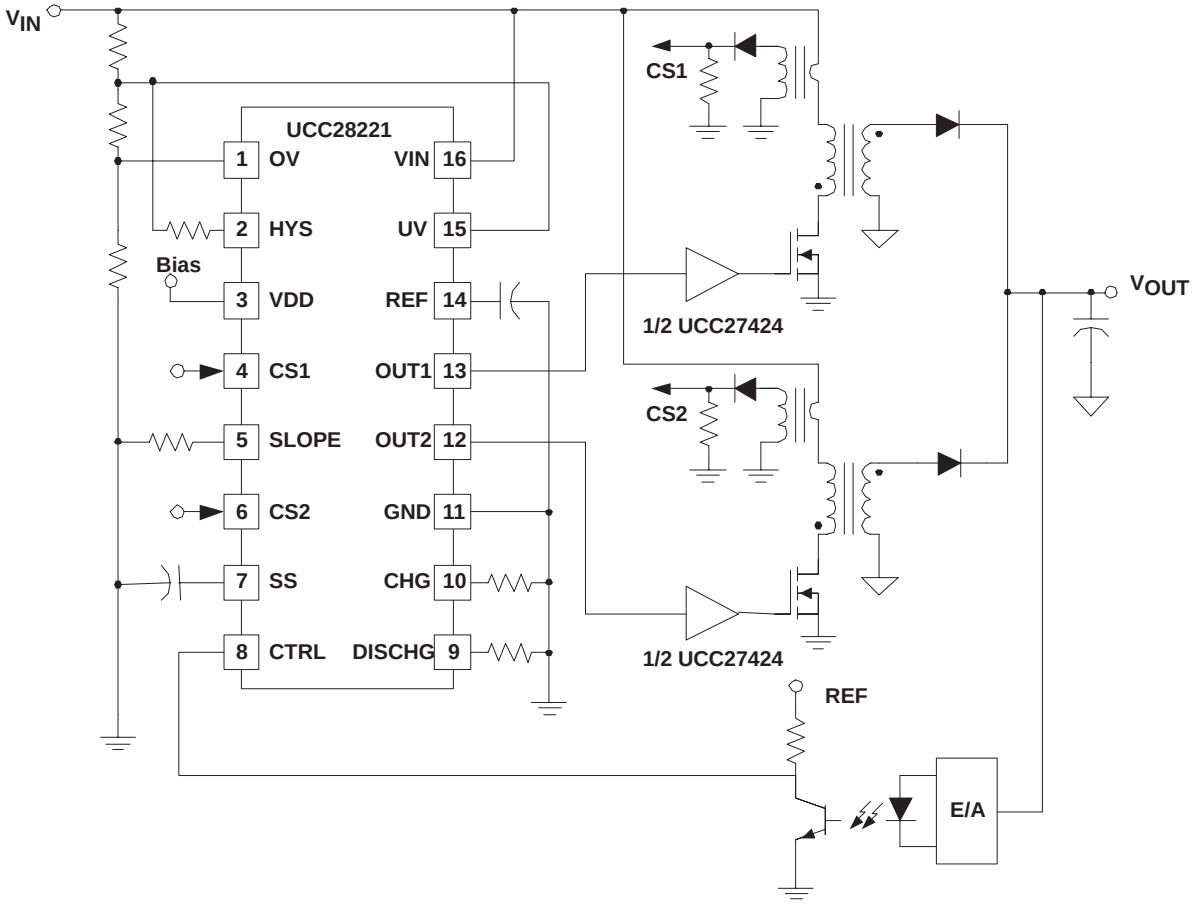


Figure 5. Interleaved Flyback Application Circuit Using the UCC28221

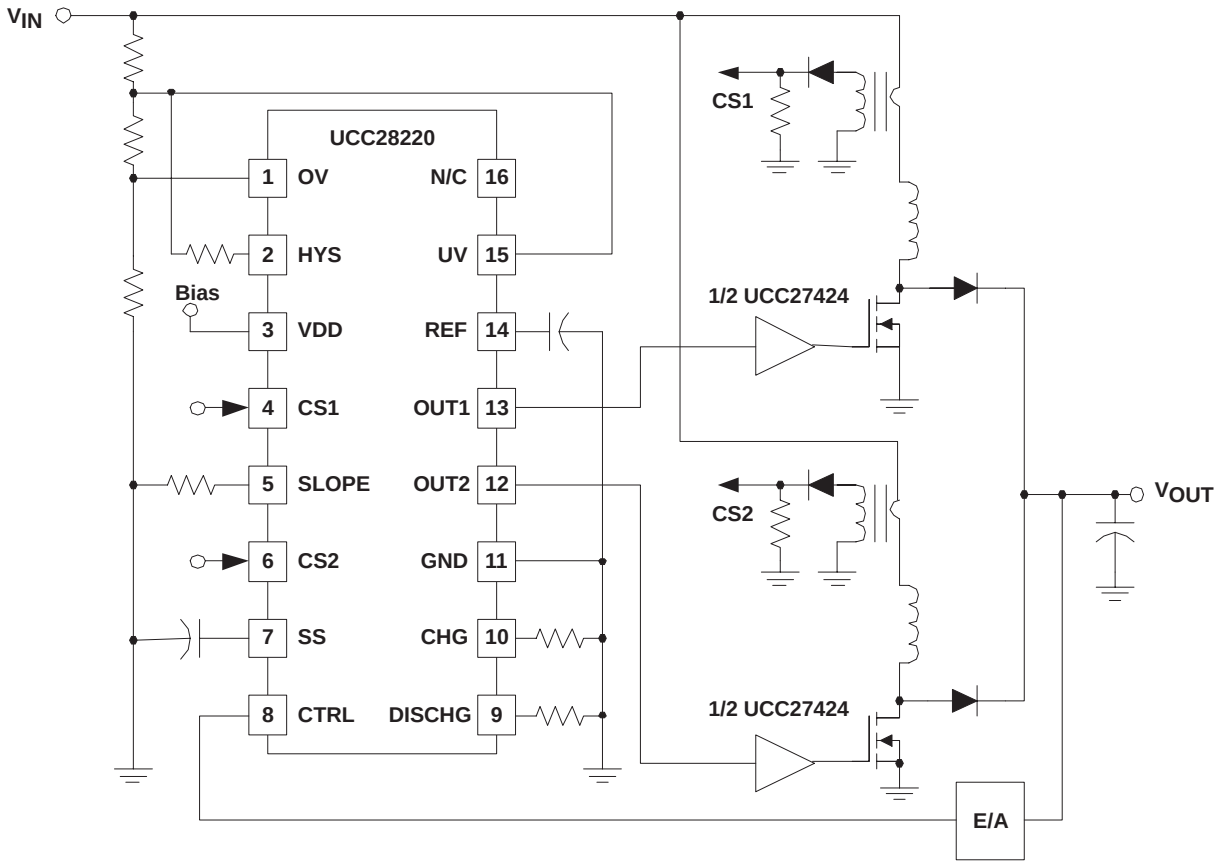


Figure 6. Interleaved Boost Application Circuit Using the UCC28220

TYPICAL CHARACTERISTICS

UVLO THRESHOLDS vs TEMPERATURE

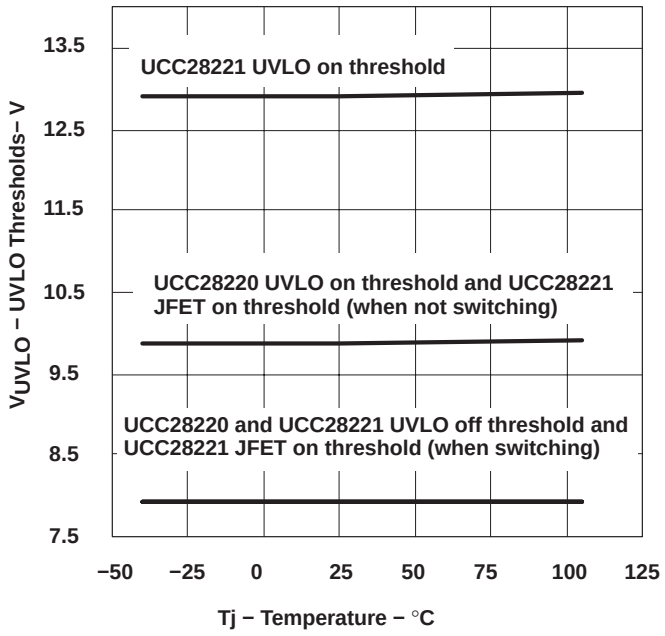


Figure 7

QUIESCENT CURRENT vs SUPPLY VOLTAGE

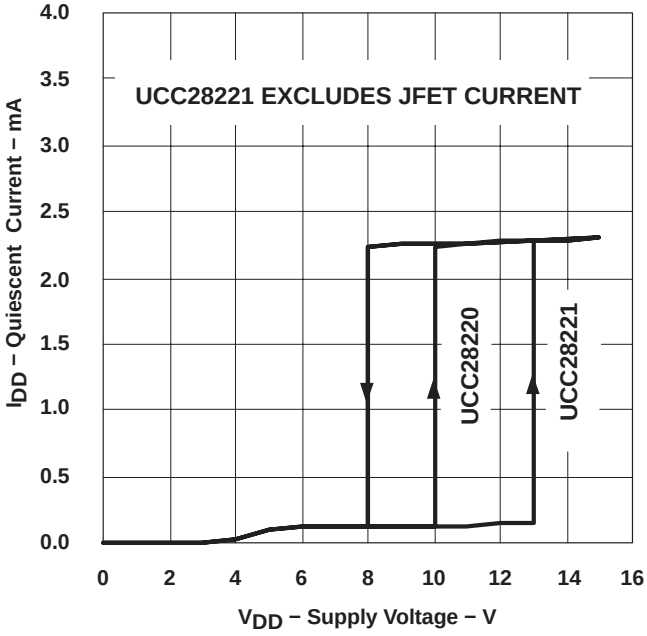


Figure 8

SUPPLY CURRENT vs SUPPLY VOLTAGE

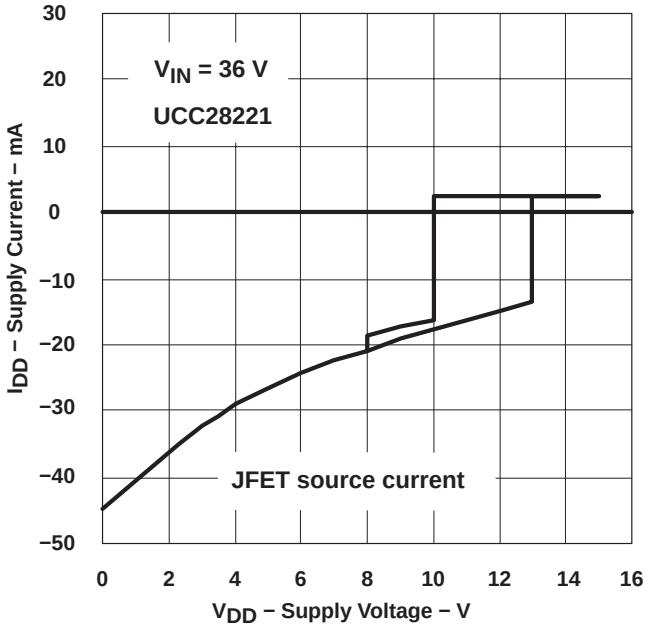


Figure 9

REFERENCE VOLTAGE vs TEMPERATURE

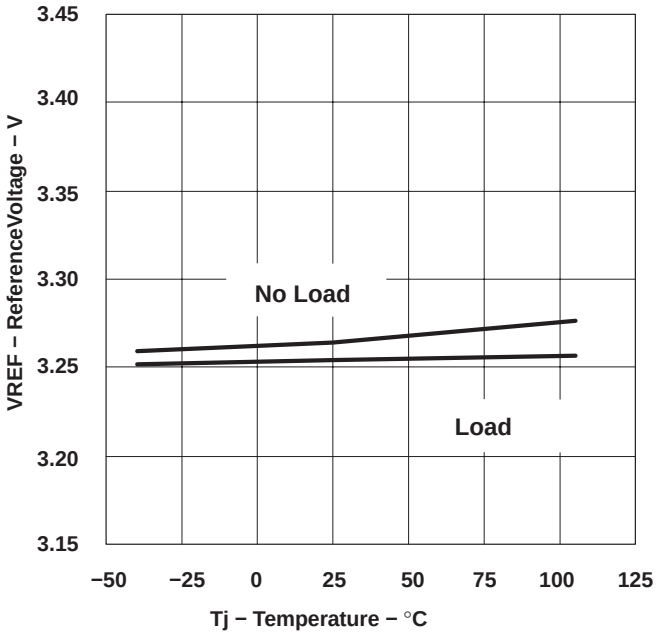


Figure 10

TYPICAL CHARACTERISTICS

LINEOV AND LINEUV THRESHOLDS vs TEMPERATURE

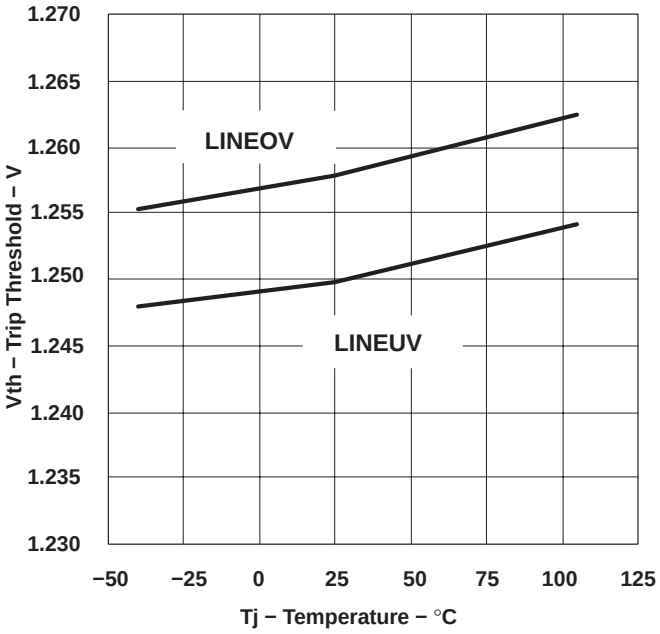


Figure 11

SLOPE COMPENSATION vs TEMPERATURE

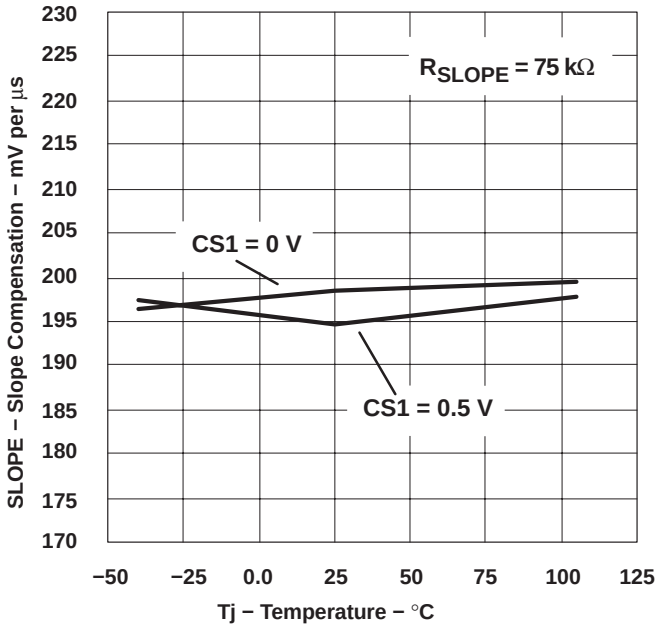


Figure 12

PROGRAMMING RESISTOR vs SLOPE COMPENSATION

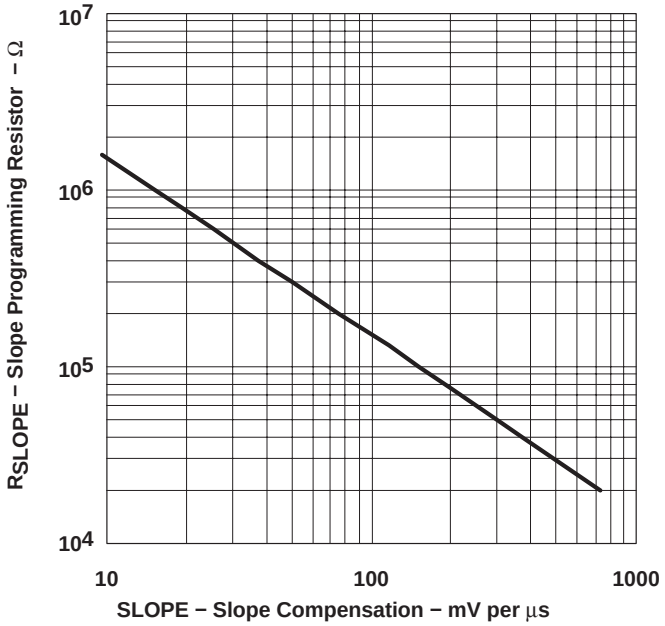


Figure 13

CHANNEL1 AND CHANNEL2 SLOPE MATCHING vs TEMPERATURE

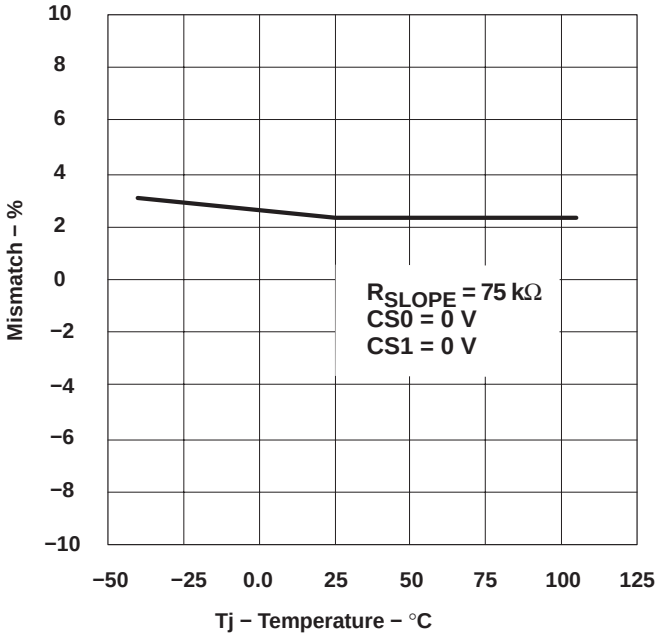


Figure 14

TYPICAL CHARACTERISTICS

RISE AND FALL TIME vs TEMPERATURE (CL = 50 pf)

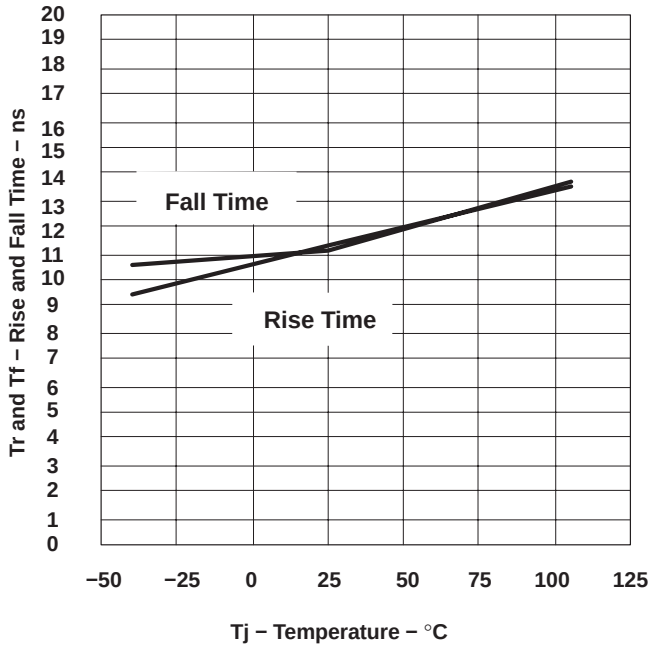


Figure 15

VOH AND VOL vs TEMPERATURE

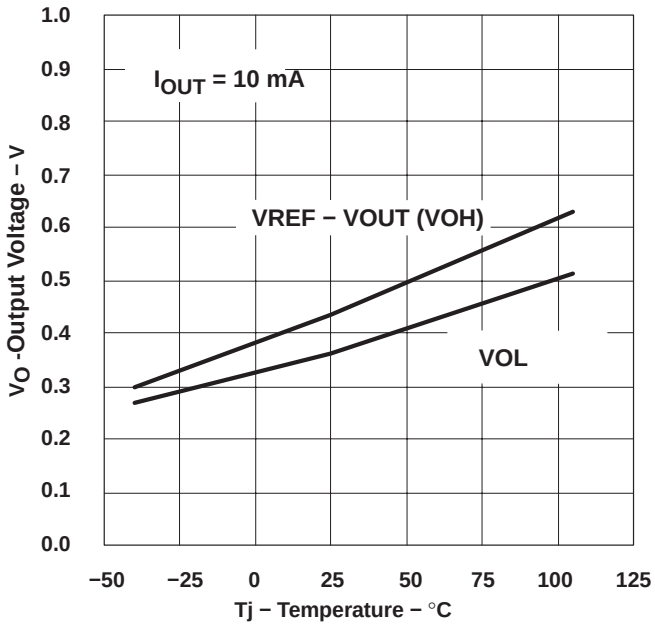


Figure 16

SOFTSTART CHARGE CURRENT vs TEMPERATURE

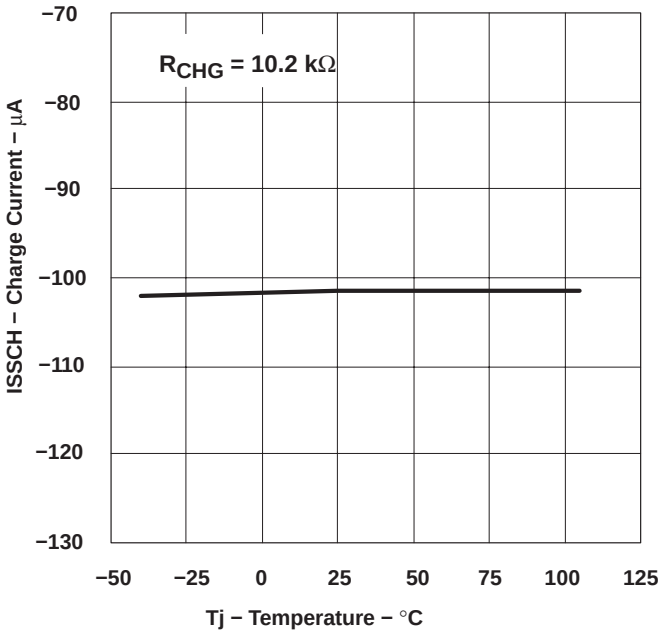


Figure 17

SOFTSTART DISCHARGE CURRENT vs TEMPERATURE

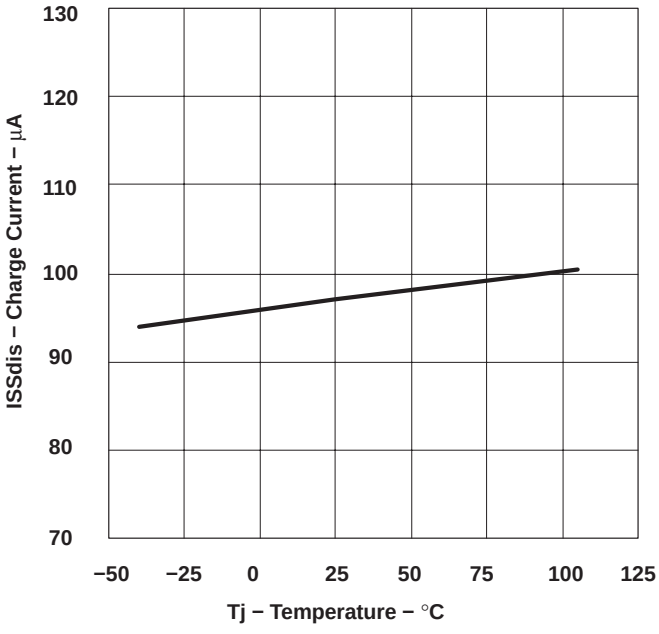


Figure 18

TYPICAL CHARACTERISTICS

PROGRAMMING RESISTORS vs SWITCHING FREQUENCY

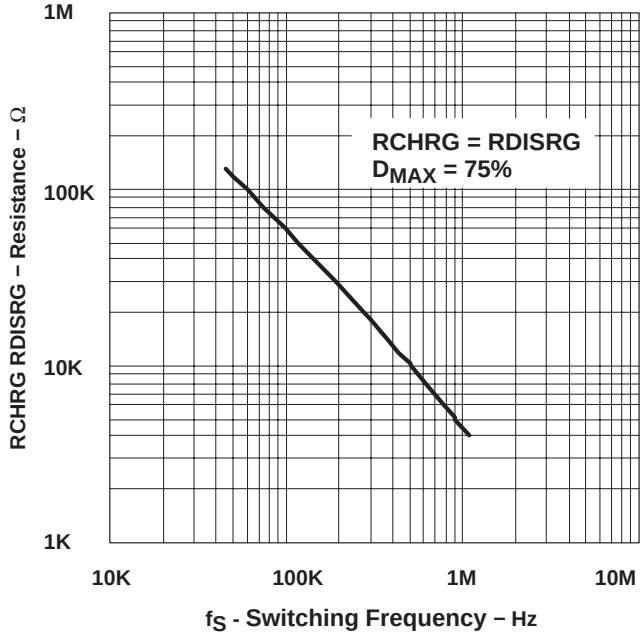


Figure 19

OSCILLATOR FREQUENCY vs TEMPERATURE

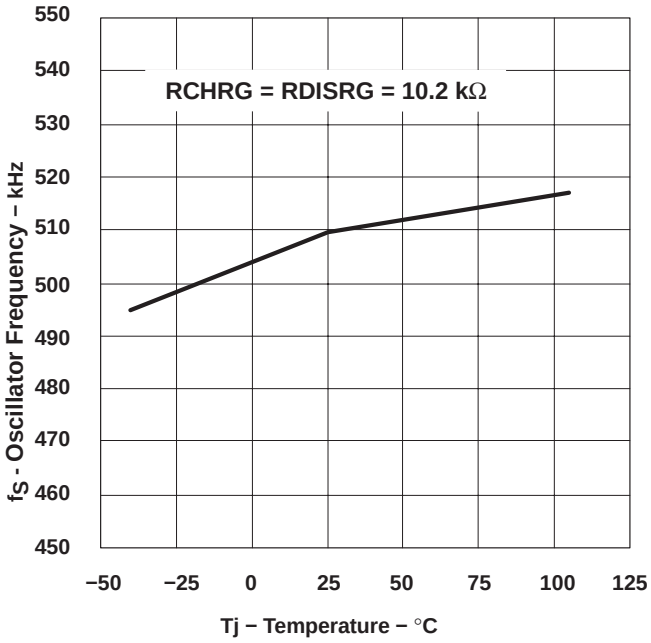


Figure 20

PROGRAMMABLE MAX DUTY CYCLE vs TEMPERATURE

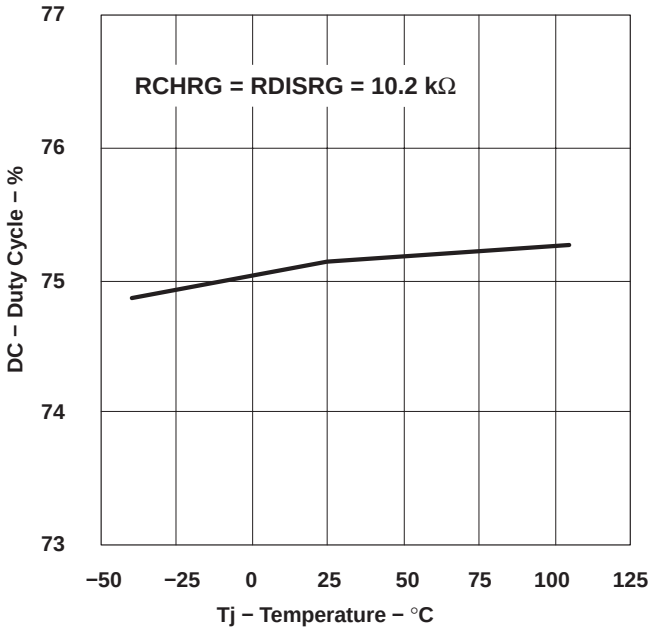


Figure 21

CSx to OUTx delay vs CSx Peak Voltage

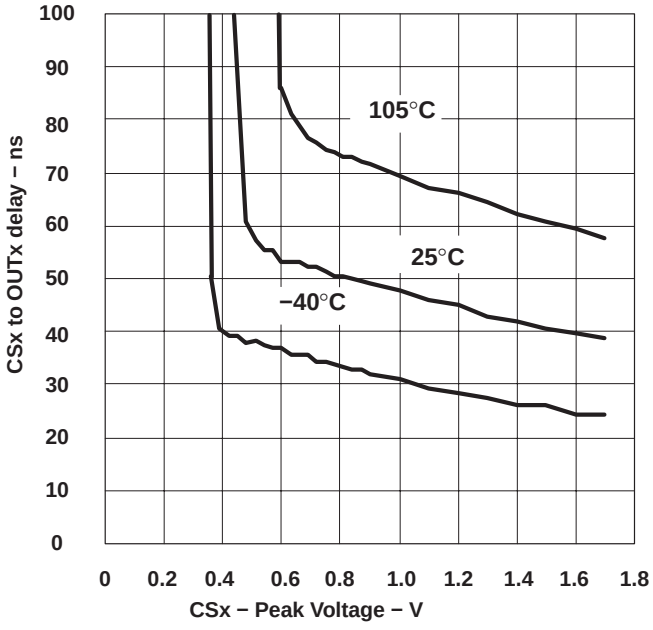


Figure 22

APPLICATION INFORMATION

Related Products

DEVICE	DESCRIPTION	PACKAGE OPTION
UCC27323/4/5	Dual 4-A High Speed Low Side MOSFET Drivers	SOIC-8, PowerPAD MSOP-8, PDIP-8
UCC27423/4/5	Dual 4-A High Speed Low Side MOSFET Drivers with Enable	SOIC-8, PowerPAD MSOP-8, PDIP-8
TPS2811/12/13	Dual 2.4-A High Speed Low Side MOSFET Drivers	SOIC-8, TSSOP-8, PDIP-8
UC3714/15	Dual 2.4-A High Speed Low Side MOSFET Drivers	SOIC-8, PowerSOIC-14, PDIP-8

References and Resources:

An evaluation module and an associated user's guide are available. The UCC28221 is used in a two-channel interleaved Forward design converting from 36-V to 76-V dc input voltage to a regulated 12-V dc output. The power module has two isolated 100 W forward power stages operating at 500 kHz, which are operating 180 degrees out of phase with each other allowing for output current ripple cancellation and smaller magnetic design. This design also takes advantage of the UCC28221's on-board 110-V internal JFET start up circuit that removes the need of an external trickle charge resistor for boot strapping. This circuit turns off after auxiliary power is supplied to the device conserving power.

- Evaluation Module, *UCC28221EVM*, 48 V_{IN}, 12 V_{OUT}, 200-W Interleaved Forward Converter
- User's Guide, *UCC28221 Evaluation Module*, Texas Instruments Literature Number SLUU173

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28220D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28221D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28221	Samples
UCC28221DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28221	Samples
UCC28221PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28221	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC28220 :

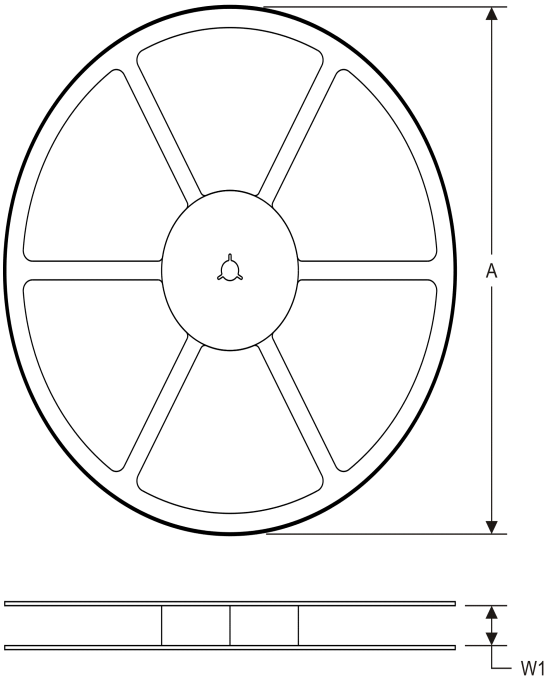
- Automotive: UCC28220-Q1

NOTE: Qualified Version Definitions:

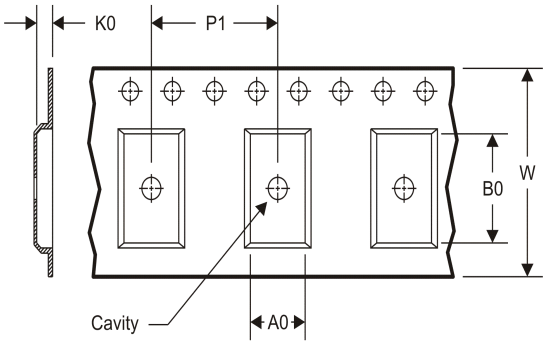
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



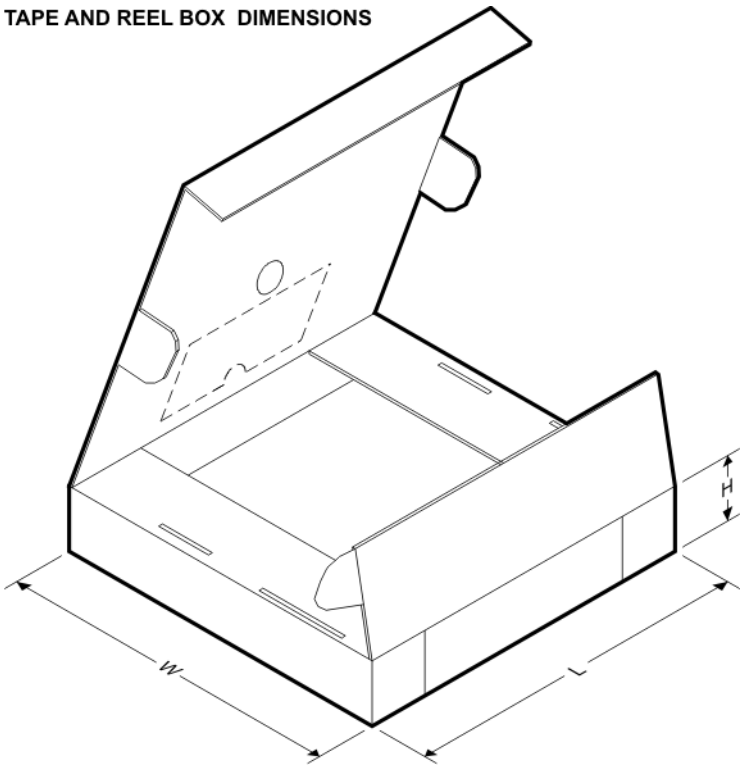
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28220DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC28220PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

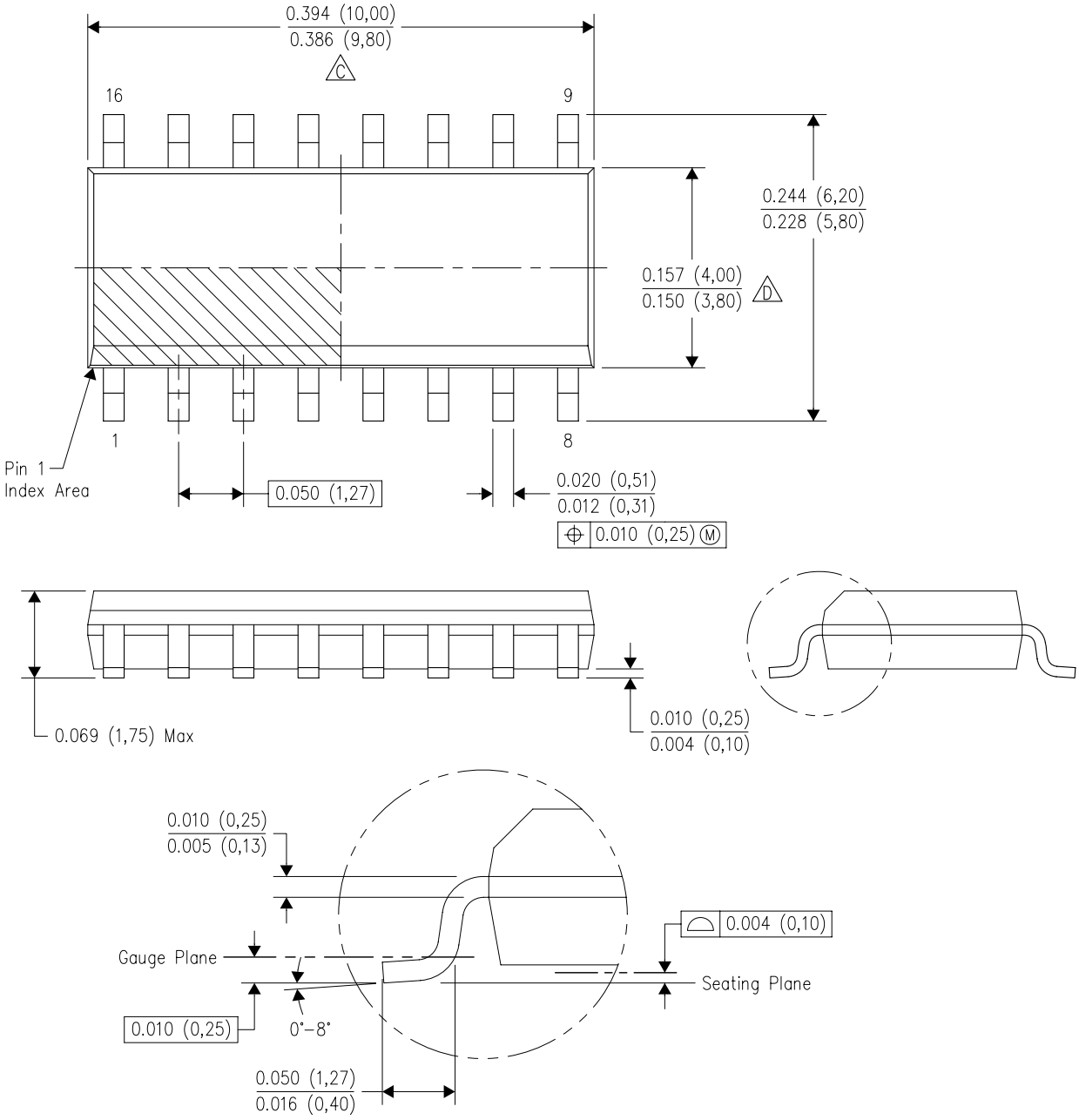
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

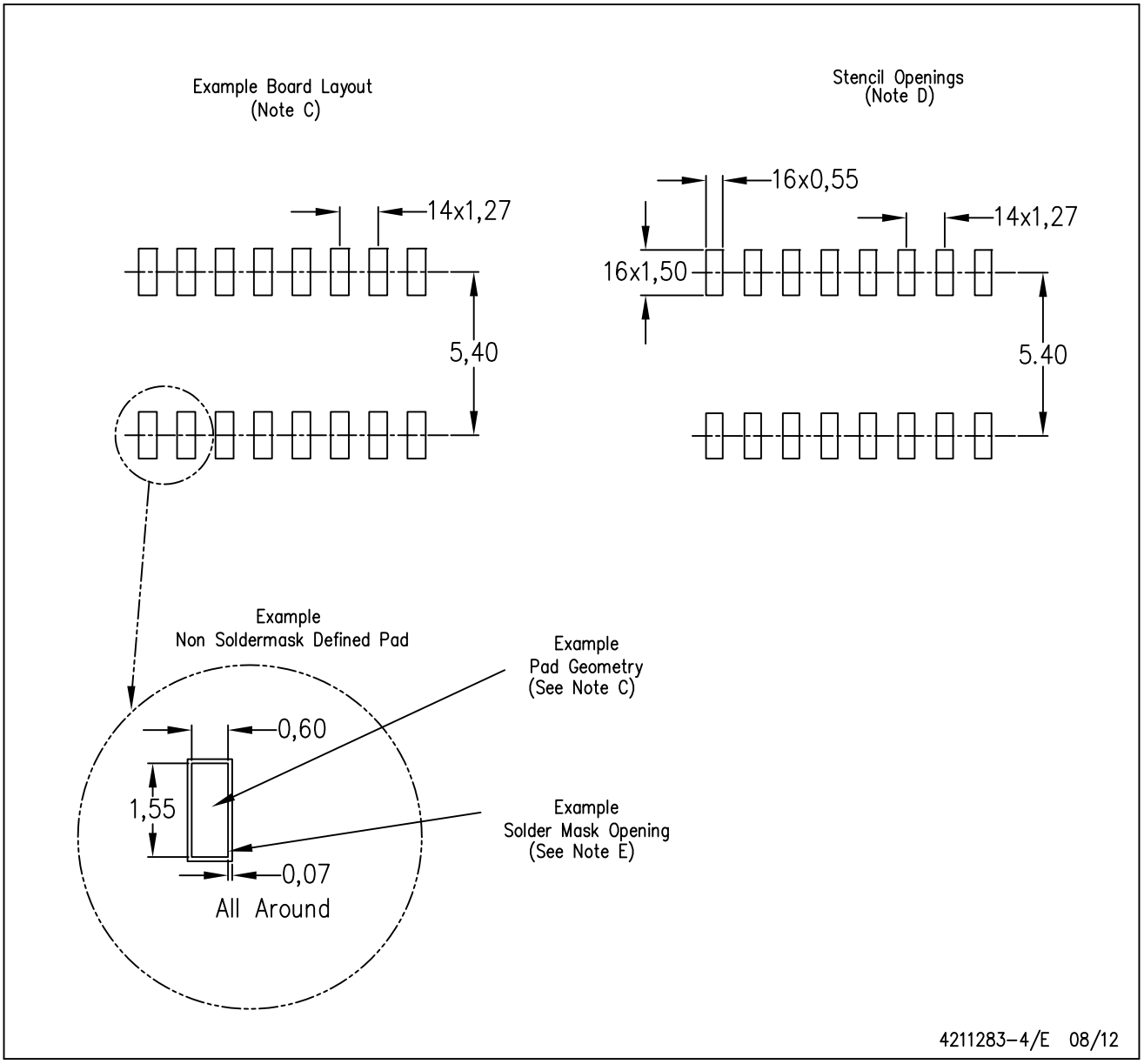
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28220DR	SOIC	D	16	2500	367.0	367.0	38.0
UCC28220PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



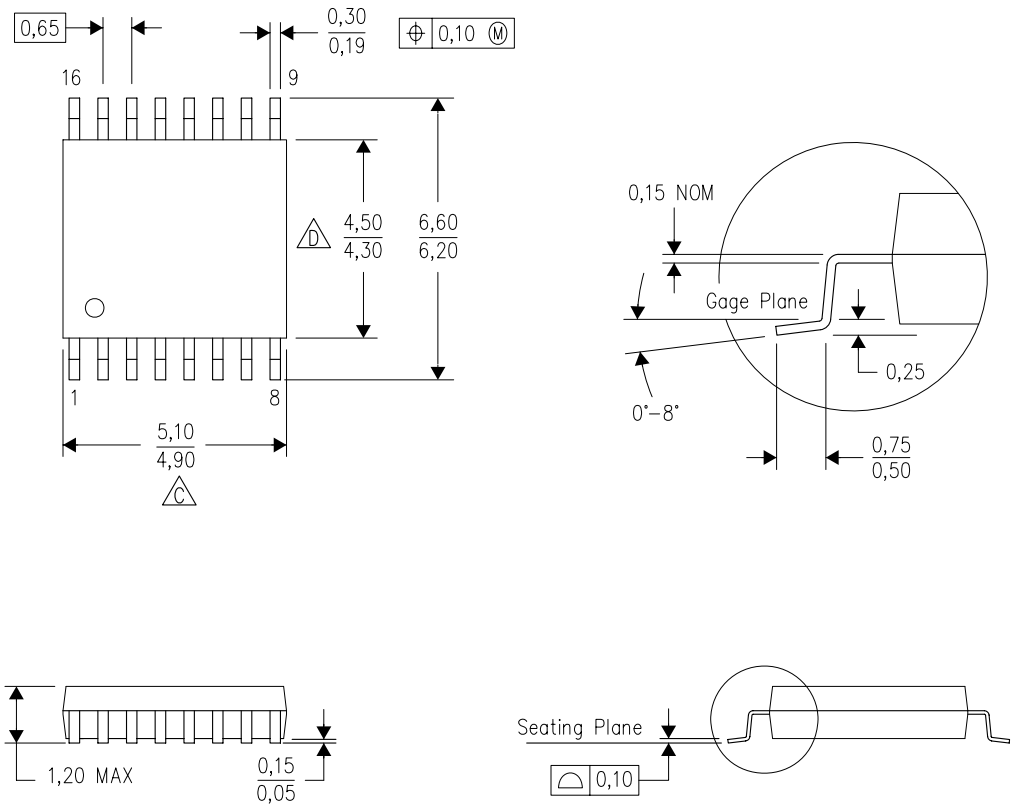
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

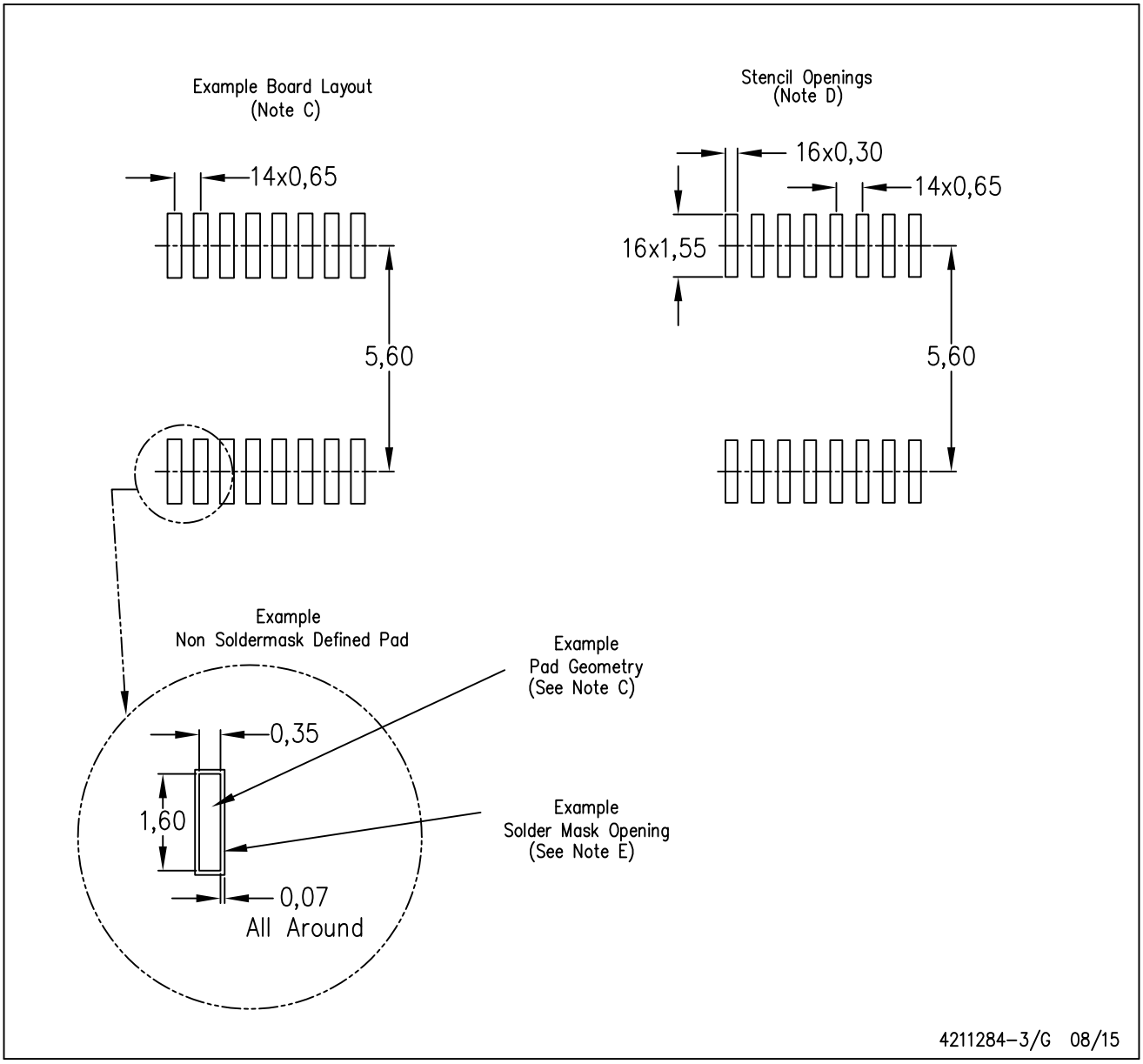
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

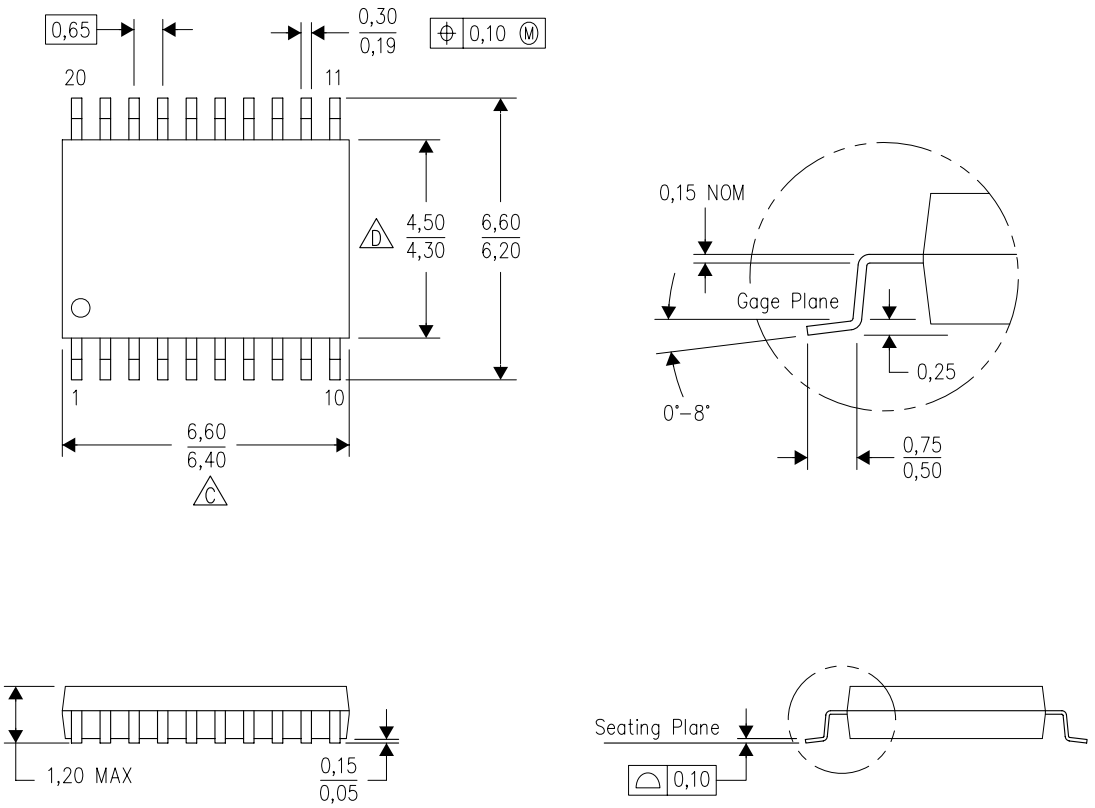
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

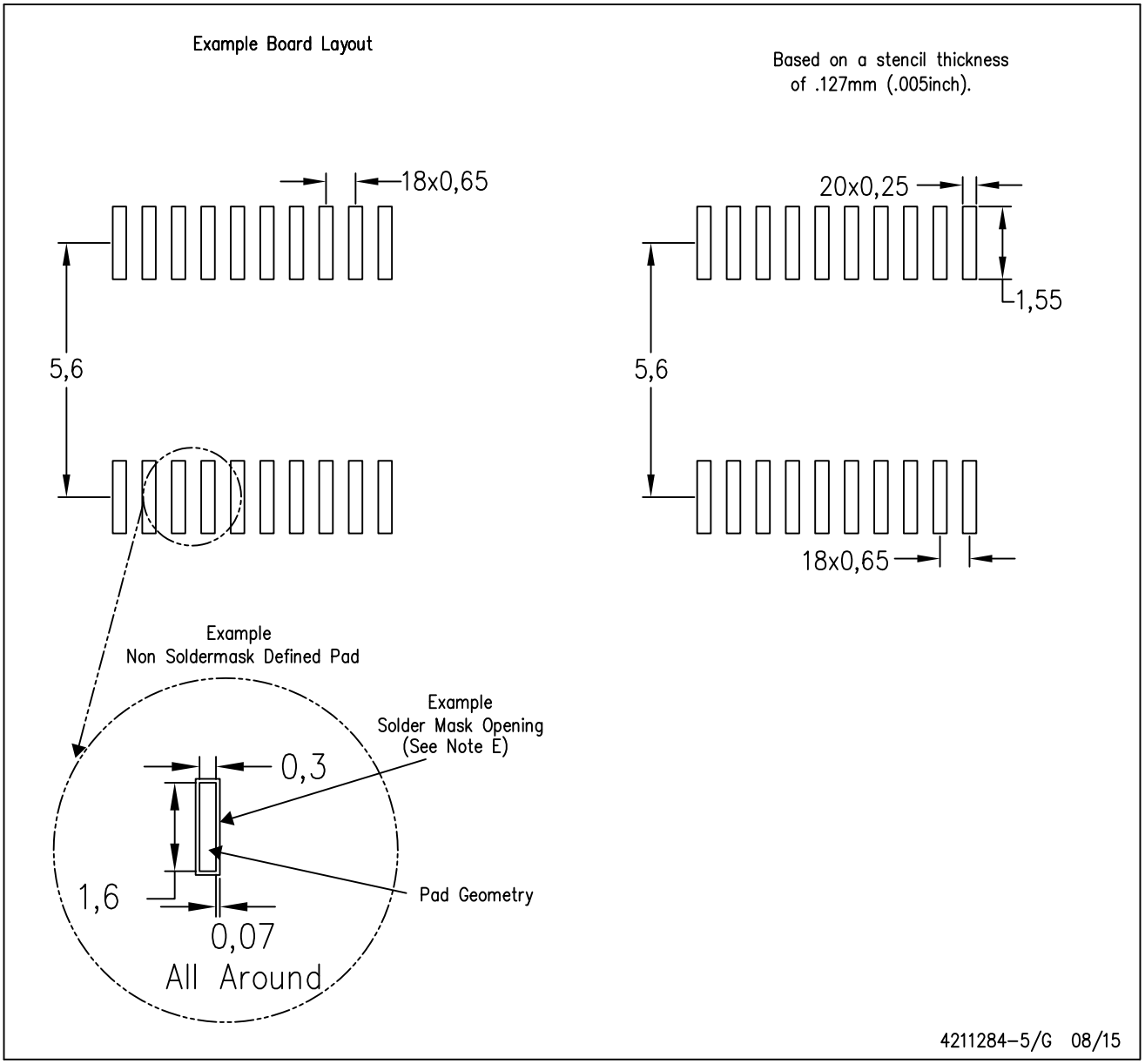
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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