Low-Power Economy BiCMOS Current-Mode PWM

Check for Samples: UCC2813-0, UCC2813-1, UCC2813-2, UCC2813-3, UCC2813-4, UCC2813-5, UCC3813-0, UCC3813-1, UCC3813-2, UCC3813-3, UCC3813-4, UCC3813-5

FEATURES

- **100-µA Typical Starting Supply Current**
- **500-µA Typical Operating Supply Current**
- **Operation to 1 MHz**
- **Internal Soft Start**
- **Internal Fault Soft Start**
- **Internal Leading-Edge Blanking of the Current-Sense Signal**
- **1-A Totem-Pole Output**
- **70-ns Typical Response from Current-Sense to Gate-Drive Output**
- **1.5% Tolerance Voltage Reference**
- **Same Pinout as UCC3802, UC3842, and UC3842A**

DESCRIPTION

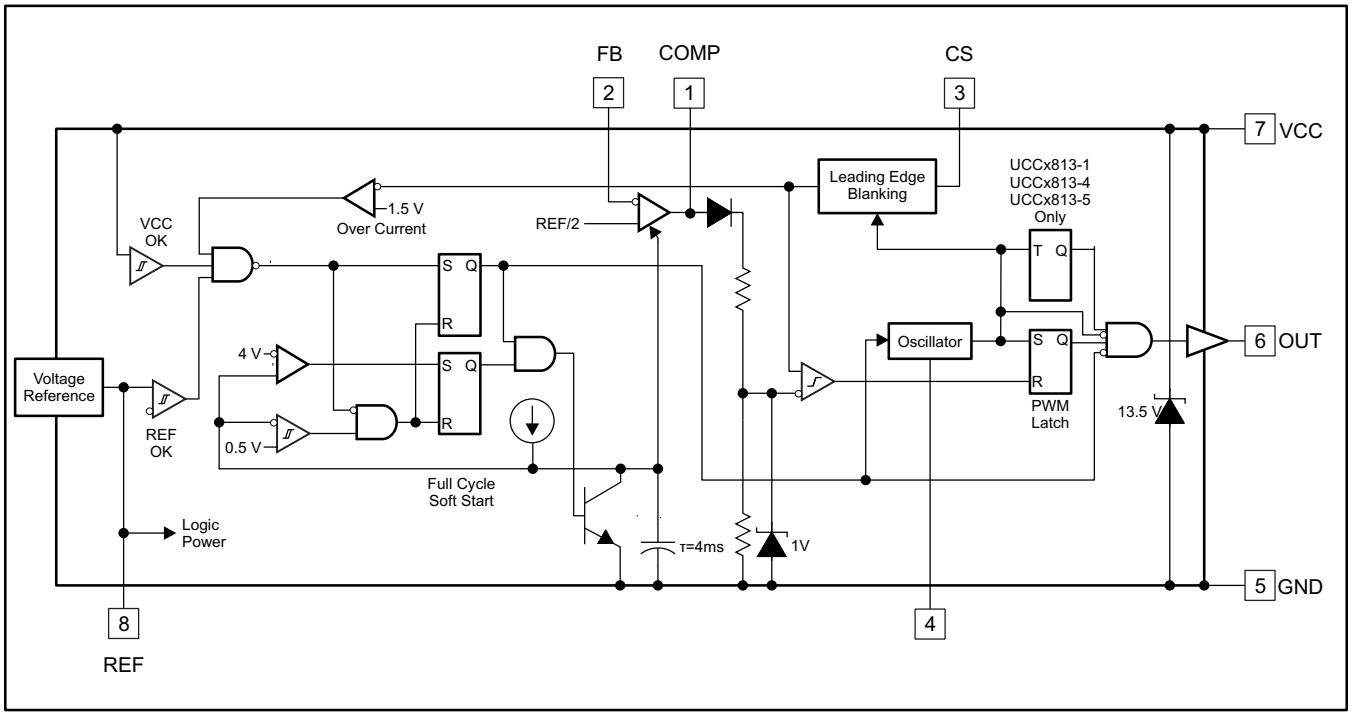
The UCC3813-x family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed-frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC384x family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC3813-x family offers a variety of package options, temperature-range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC3813-3 and UCC38135 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC3813-2 and UCC3813-4 make these ideal choices for use in off-line power supplies.

The UCC2813-x series is specified for operation from –40°C to +85°C and the UCC3813-x series is specified for operation from 0°C to 70°C.

BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Part Number(1)	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx813-0	100%	5 V	7.2 V	6.9 V
UCCx813-1	50%	5 V	9.4 V	7.4 V
UCCx813-2	100%	5 V	12.5 V	8.3 V
UCCx813-3	100%	4 V	4.1 V	3.6 V
UCCx813-4	50%	5 V	12.5 V	8.3 V
UCCx813-5	50%	4 V	4.1 V	3.6 V

(1) The *x* in the part number refers to temperature range difference between UCC2813 and UCC3813.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Analog inputs (FB, CS, RC, COMP)		–3 to the lesser of 6.3 or VCC + 0.3		V
VCC voltage(3)			12	V
OUT current			±1	A
VCC current			30	mA
OUT energy (capacitive load)			20	µJ
Power dissipation at T_A < 25°C	D package		0.65	W
	N package		1	W
Junction temperature		–55	150	°C
Storage temperature		–65	150	°C

(1) All voltages are with respect to GND. All currents are positive into the specified terminal. Consult Unitrode Integrated Circuits databook for Information regarding thermal specifications and limitations of packages.
(2) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) In normal operation VCC is powered through a current limiting resistor. Absolute maximum of 12 V applies when VCC is driven from a low impedance source such that ICC does not exceed 30 mA. The resistor must be sized so that the VCC voltage under-operating conditions is below 12 V but above the tunoff threshold.

Thermal Information

THERMAL METRIC(1)		UCCX813-X DIL (P) 8 PINS	UCCX813-X SOIC (D) 8 PINS	UCCX813-X TSSOP (PW) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	50.9	107.5	153.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	40.3	49.3	38.4	
θ_{JB}	Junction-to-board thermal resistance(4)	28.1	48.7	83.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	17.6	6.6	2.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	28.0	48.0	82.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for –40°C ≤ T_A ≤ +85°C for UCC2813-x; 0°C ≤ T_A ≤ +70°C for UCC3813-x; VCC = 10 V(1); RT = 100 k from REF to RC; CT = 330 pF from RC to GND; 0.1-µF capacitor from VCC to GND; 0.1-µF capacitor from VREF to GND. $T_A = T_J$.

PARAMETER		TEST CONDITIONS	UCC2813-x UCC3813-x			UNIT
			MIN	TYP	MAX	
Reference Section						
	Output voltage	T_J = 25°C, I = 0.2 mA, UCCx813-0 / -1 / -2 / -4	4.925	5	5.075	V
		T_J = 25°C, I = 0.2 mA, UCCx813-3 / -5	3.94	4	4.06	
	Load regulation	0.2 mA < I < 5 mA		10	30	mV
	Total variation	UCCx813-0 / -1 / -2 / -4(2)	4.84	5	5.1	V
		UCCx813-5, UCCx813-3(2)	3.84	4	4.08	
	Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C(3)		70		µV
	Long term stability	T_A = 125°C, 1000 Hours(3)		5		mV
	Output short circuit		–5		–35	mA
Oscillator Section						
	Oscillator frequency	UCCx813-0 / -1 / -2 / -4(4)	40	46	52	kHZ
		UCCx813-3 / -5(4)	26	31	36	
	Temperature stability	See (3)		2.5		%
	Amplitude peak-to-peak		2.25	2.4	2.55	V
	Oscillator peak voltage			2.45		V
Error Amplifier Section						
	Input voltage	COMP = 2.5 V; UCCx813-0 / -1 / -2 / -4	2.42	2.5	2.56	V
		COMP = 2 V; UCCx813-3 / -5	1.92	2	2.05	
	Input bias current		–2		2	µA
	Open loop voltage gain		60	80		dB
	COMP sink current	FB = 2.7 V, COMP = 1.1 V	0.4		2.5	mA
	COMP source current	FB = 1.8 V, COMP = REF – 1.2 V	–0.2	–0.5	–0.8	mA
	Gain bandwidth product	See (3)		2		MHZ
PWM Section						
	Maximum duty cycle	UCCx813-0 / -2 / -3	97	99	100	%
		UCCx813-1 / -4 / -5	48	49	50	
	Minimum duty cycle	COMP = 0 V			0	%
Current Sense Section						
	Gain	See (5)	1.1	1.65	1.8	V/V
	Maximum input signal	COMP = 5 V(6)	0.9	1	1.1	V
	Input bias current		–200		200	nA
	CS blank time		50	100	150	ns
	overcurrent threshold		1.32	1.55	1.7	V
	COMP to CS offset	CS = 0 V	0.45	0.9	1.35	V

(1) Adjust VCC above the start threshold before setting at 10 V.
(2) Total Variation includes temperature stability and load regulation.
(3) Ensured by design. Not 100% tested in production.
(4) Oscillator frequency for the UCCx813-0, UCCx813-2, and UCCx813-3 is the output frequency.
Oscillator frequency for the UCCx813-1, UCCx813-4, and UCCx813-5 is twice the output frequency.
(5) Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}} \quad 0 \le V_{CS} \le 0.8\ V$.
(6) Parameter measured at trip point of latch with Pin 2 at 0 V.

ELECTRICAL CHARACTERISTICS (continued)

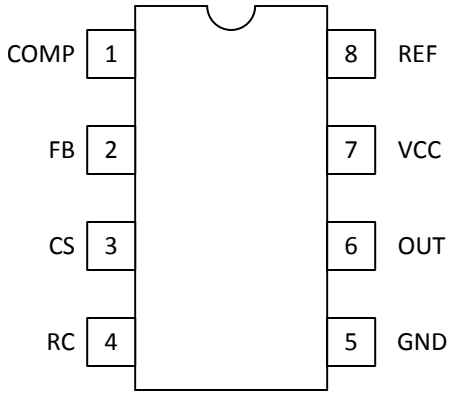
Unless otherwise stated, these specifications apply for –40°C ≤ T_A ≤ +85°C for UCC2813-x; 0°C ≤ T_A ≤ +70°C for UCC3813-x; VCC = 10 V(1); RT = 100 k from REF to RC; CT = 330 pF from RC to GND; 0.1-µF capacitor from VCC to GND; 0.1-µF capacitor from VREF to GND. $T_A = T_J$.

PARAMETER		TEST CONDITIONS	UCC2813-x UCC3813-x			UNIT
			MIN	TYP	MAX	
Output Section						
	OUT low level	I = 20 mA, all parts		0.1	0.4	V
		I = 200 mA, all parts		0.35	0.9	
		I = 50 mA, VCC = 5 V, UCCx813-3 / -5		0.15	0.4	
		I = 20 mA, VCC = 0 V, all parts		0.7	1.2	
V_{CC}-OUT	OUT high VsAT	I = –20 mA, all parts		0.15	0.4	V
		I = –20 0mA, all parts		1	1.9	
		I = –50 mA, VCC = 5 V, UCCx813-3 / -5		0.4	0.9	
	Rise time	CL= 1 nF		41	70	ns
	Fall time	CL = 1 nF		44	75	ns
Undervoltage Lockout Section						
	Start threshold (7)	UCCx813-0	6.6	7.2	7.8	V
		UCCx813-1	8.6	9.4	10.2	
		UCCx813-2 / -4	11.5	12.5	13.5	
		UCCx813-3 / -5	3.7	4.1	4.5	
	Stop threshold (7)	UCC1813-0	6.3	6.9	7.5	V
		UCC1813-1	6.8	7.4	8	
		UCCx813-2 / -4	7.6	8.3	9	
		UCCx813-3 / -5	3.2	3.6	4	
	Start to stop hysteresis	UCCx813-0	0.12	0.3	0.48	V
		UCCx813-1	1.6	2	2.4	
		UCCx813-2 / -4	3.5	4.2	5.1	
		UCCx813-3 / -5	0.2	0.5	0.8	
Soft Start Section						
	COMP rise time	FB = 1.8 V, Rise from 0.5 V to REF – 1 V		4		ms
Overall Section						
	Start-up current	VCC < Start Threshold		0.1	0.23	mA
	Operating supply current	FB = 0 V, CS = 0 V, RC = 0 V		0.5	1.2	mA
	VCC internal Zener voltage	ICC = 10 mA(7)	12	13.5	15	V
	VCC internal Zener voltage minus start-threshold voltage	UCCx813-2 / -4	0.5	1		V

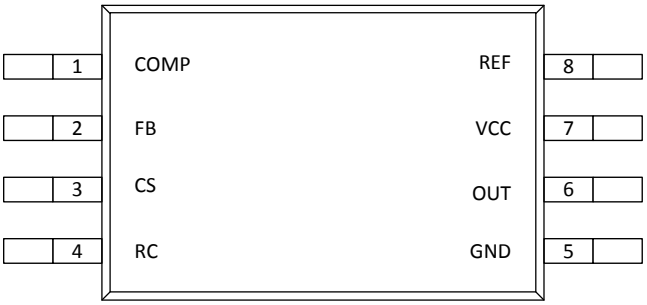
(7) Start threshold, stop threshold, and Zener-shunt thresholds track one another.

DEVICE INFORMATION

**DIL-8 (PDIP) OR SOIC-8
N (P) OR D PACKAGE
(TOP VIEW)**



**TSSOP-8
PW PACKAGE
(TOP VIEW)**



PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3813 family is a true low-output-impedance 2-MHz operational amplifier. As such, the COMP terminal both sources and sinks current. However, the error amplifier is internally current limited, so that zero duty cycle is commanded by externally forcing COMP to GND.

The UCC3813 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: CS is the input to the current-sense comparators. The UCC3813 family has two different current-sense comparators: the PWM comparator and an overcurrent comparator.

The UCC3813 family contains digital current-sense filtering, which disconnects the CS terminal from the current sense comparator during the 100-ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The overcurrent comparator is only intended for fault sensing, and exceeding the overcurrent threshold causes a soft start cycle.

FB: FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: GND is reference ground and power ground for all functions on this part.

OUT: OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±750 mA. OUT is actively held low when VCC is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to VCC. The output stage also provides a very low impedance to overshoot and undershoot which means that in many cases, external schottky clamp diodes are not required.

RC: RC is the oscillator timing pin. For fixed frequency operation, set the timing-capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation is estimated with the following equations:

$$\text{UCCx813} - 0/-1/-2/-4: \quad F = \frac{1.5}{R \times C}$$

$$\text{UCCx813} - 3, \text{UCCx813} - 5: \quad F = \frac{1}{R \times C}$$

where

- frequency is in hertz
- resistance is in ohms
- capacitance is in farads (1)

The recommended range of timing resistors is between 10 and 200 k and timing capacitor is 100 to 1000 pF. Never use a timing resistor less than 10 k.

REF: REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

When VCC is greater than 1 V and less than the UVLO threshold, REF is pulled to ground through a 5-kQ resistor which means that REF is used as a logic output indicating power-system status. For referencing stability, bypassing REF to GND with a ceramic capacitor as close to the pin as possible is important. An electrolytic capacitor is also used in addition to the ceramic capacitor. A minimum of 0.1-µF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5 mA on the reference.

To prevent noise problems with high speed switching transients, bypass REF to ground with a ceramic capacitor very close to the IC package.

VCC: VCC is the power input connection for this device. In normal operation VCC is powered through a current limiting resistor. Although quiescent VCC current is very low, total supply current will be higher, depending on OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from Equation 2.

$$I_{OUT} = Q_g \times F \quad (2)$$

To prevent noise problems, bypass VCC to GND with a 0.1-µF ceramic capacitor in parallel as close to the VCC pin as possible. An electrolytic capacitor can also be used in addition to the ceramic capacitor.

APPLICATION INFORMATION

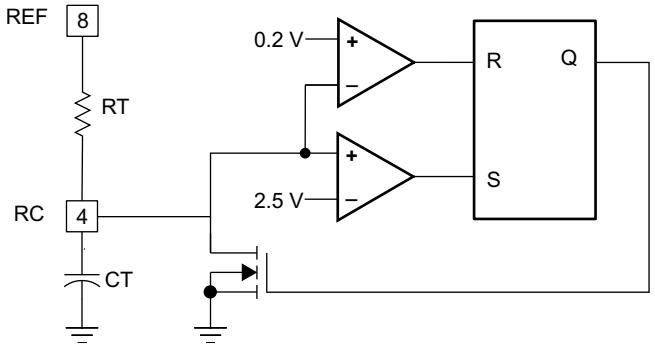


Figure 1. Oscillator

The UCC3813-0/-1/-2/-3/-4/-5 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of R_T and C_T. The fall time is set by CT and an internal transistor on-resistance of approximately 125 Ω. During the fall time, the output is off and the maximum duty cycle is reduced below 50% or 100% depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

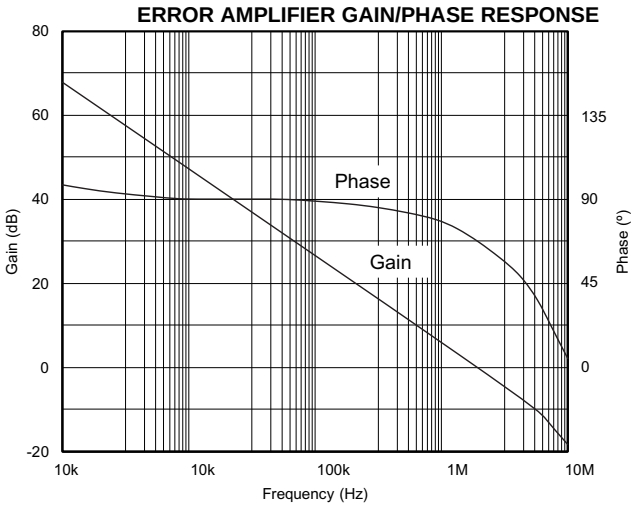


Figure 2.

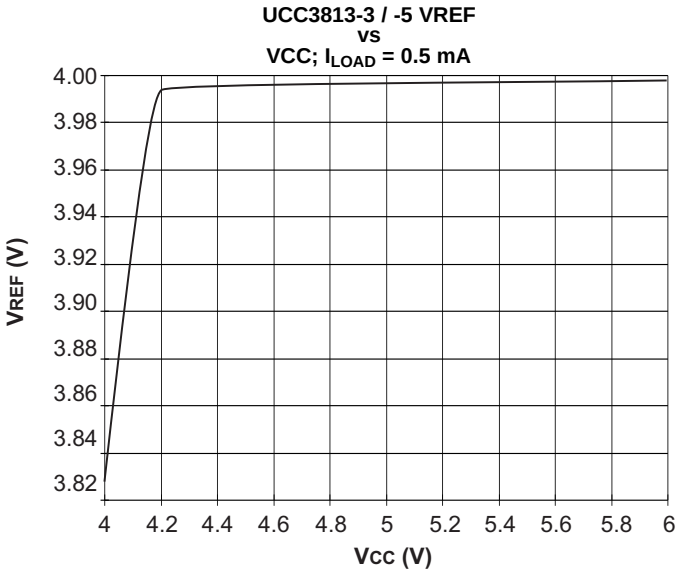


Figure 3.

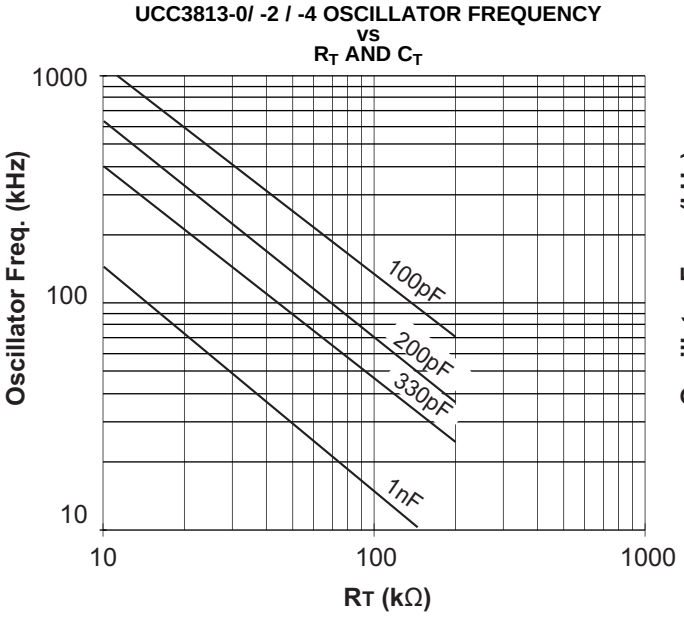


Figure 4.

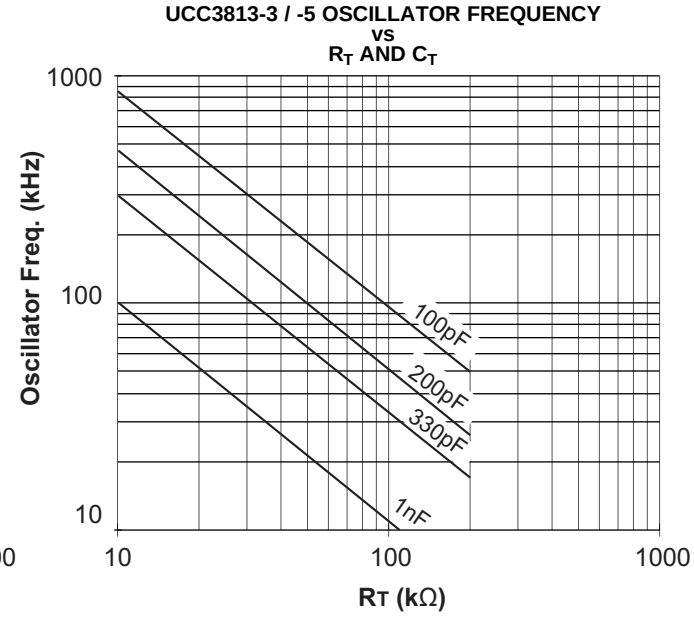


Figure 5.

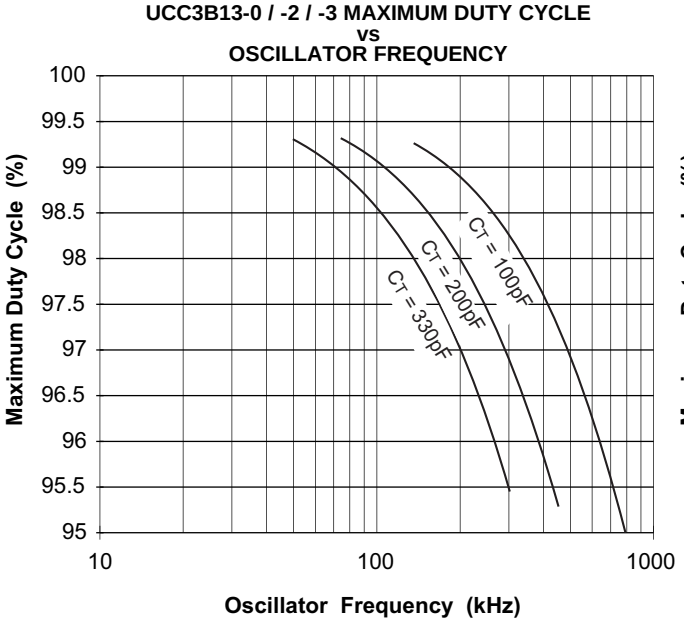


Figure 6.

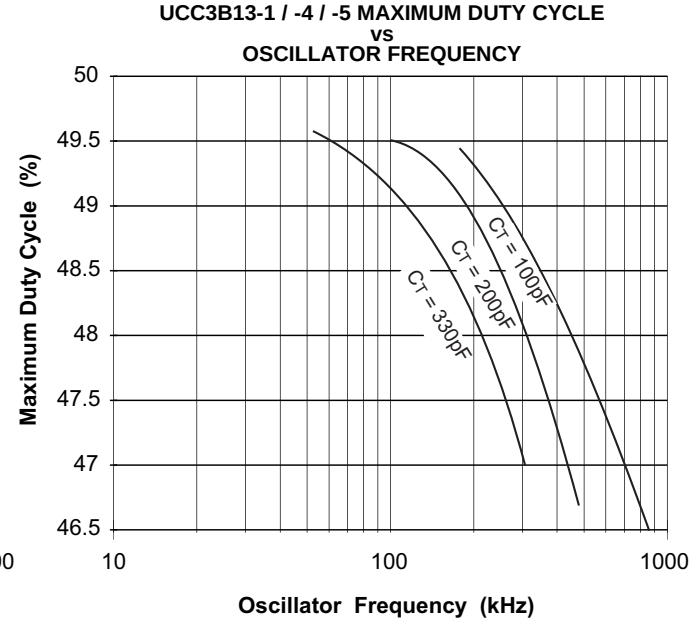


Figure 7.

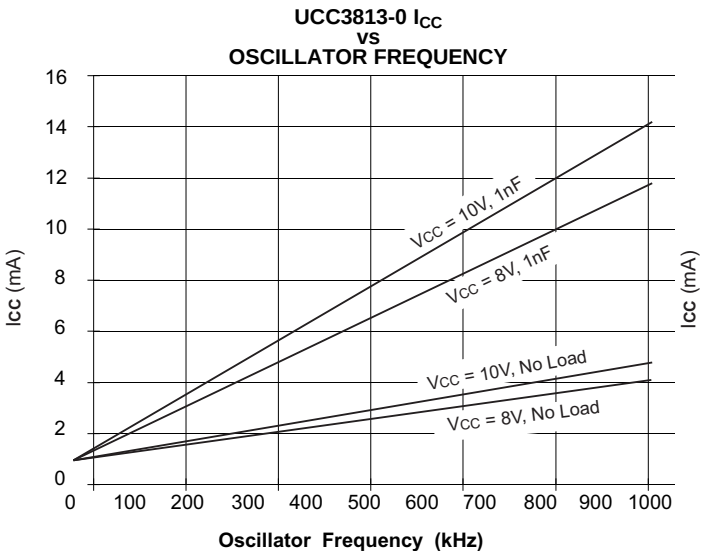


Figure 8.

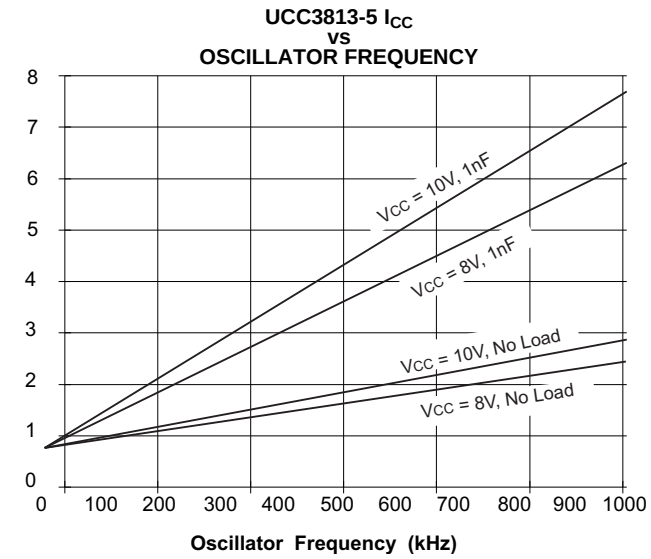


Figure 9.

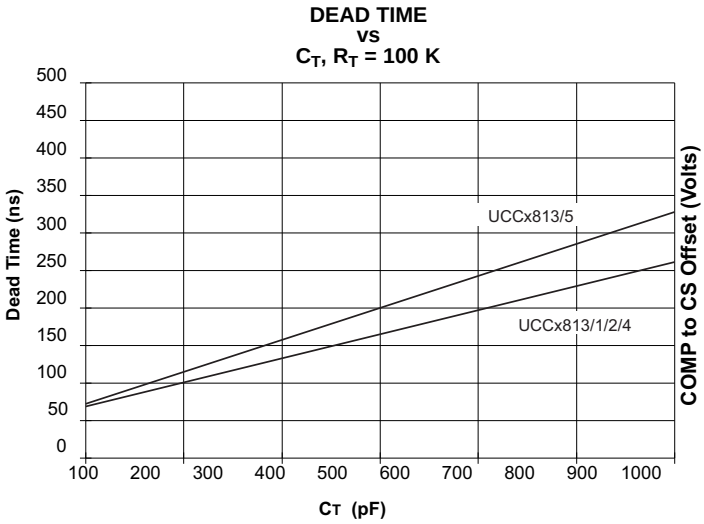


Figure 10.

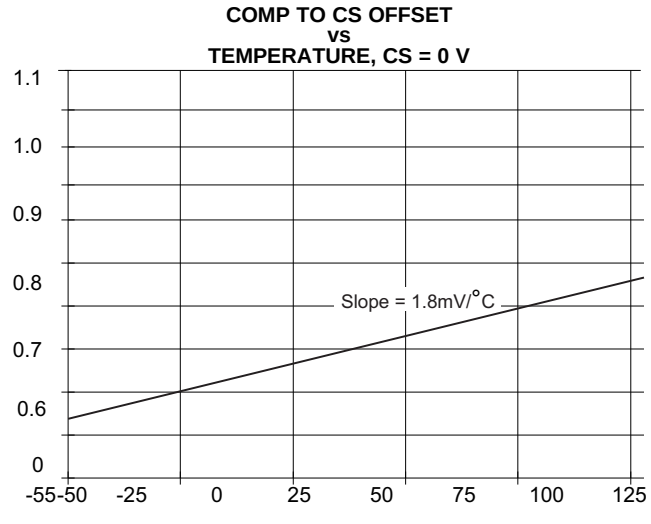


Figure 11.

REVISION HISTORY

Changes from Revision B (April 2008) to Revision C **Page**

- Added Analog inputs RC and COMP in the *ABSOLUTE MAXIMUM RATINGS* Table 2
- Added clarification to Analog Inputs min-max range in the *ABSOLUTE MAXIMUM RATINGS* table 2

Changes from Revision C (August 2010) to Revision D **Page**

- Added temperature range table note to second part of ordering information table for clarity in new datasheet format 2
- Added TI's general Absolute Maximum Ratings table note to end of *ABSOLUTE MAXIMUM RATINGS* table 2
- Added Thermal Information Table. 2
- Added UCCX813-3 to Total variation test condition line containing UCCx813-5 in *ELECTRICAL CHARACTERISTICS* table 3
- Changed part numbers in Dead Time vs C_T, R_T = 100 k graph in *APPLICATION INFORMATION* 9
- Changed layout from Unitrode Products datasheet to TI datasheet 9

PACKAGE OPTION ADDENDUM

19-Feb-2015

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2813D-0	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-0 2813D-0	Samples
UCC2813D-0G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-0 2813D-0	Samples
UCC2813D-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-1 2813D-1	Samples
UCC2813D-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-1 2813D-1	Samples
UCC2813D-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-2 2813D-2	Samples
UCC2813D-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-2 2813D-2	Samples
UCC2813D-3	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-3 2813D-3	Samples
UCC2813D-3G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-3 2813D-3	Samples
UCC2813D-4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-4 2813D-4	Samples
UCC2813D-4G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-4 2813D-4	Samples
UCC2813D-5	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-5 2813D-5	Samples
UCC2813D-5G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-5 2813D-5	Samples

19-Feb-2015

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2813DTR-0	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-0 2813D-0	Samples
UCC2813DTR-0G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-0 2813D-0	Samples
UCC2813DTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-1 2813D-1	Samples
UCC2813DTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-1 2813D-1	Samples
UCC2813DTR-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-2 2813D-2	Samples
UCC2813DTR-2G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-2 2813D-2	Samples
UCC2813DTR-3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-3 2813D-3	Samples
UCC2813DTR-3G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-3 2813D-3	Samples
UCC2813DTR-4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-4 2813D-4	Samples
UCC2813DTR-4G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-4 2813D-4	Samples
UCC2813DTR-5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-5 2813D-5	Samples
UCC2813DTR-5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2813 D-5 2813D-5	Samples
UCC2813N-0	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2813N-0	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2813N-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2813N-1	Samples
UCC2813N-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2813N-2	Samples
UCC2813N-3	ACTIVE		UTR			TBD	Call TI	Call TI			Samples
UCC2813N-4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2813N-4	Samples
UCC2813N-4G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2813N-4	Samples
UCC2813N-5	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2813N-5	Samples
UCC2813PW-0	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28130	Samples
UCC2813PW-1	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28131	Samples
UCC2813PW-1G4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28131	Samples
UCC2813PW-2	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28132	Samples
UCC2813PW-3	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28133	Samples
UCC2813PW-3G4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28133	Samples
UCC2813PW-4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28134	Samples
UCC2813PW-5	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28135	Samples
UCC2813PW-5G4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28135	Samples
UCC2813PWTR-0	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28130	Samples
UCC2813PWTR-0G4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28130	Samples
UCC2813PWTR-1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28131	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2813PWTR-3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28133	Samples
UCC2813PWTR-3G4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28133	Samples
UCC2813PWTR-4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28134	Samples
UCC2813PWTR-4G4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28134	Samples
UCC2813PWTR-5	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28135	Samples
UCC3813D-0	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-0 3813D-0	Samples
UCC3813D-0G4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70		Samples
UCC3813D-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-1 3813D-1	Samples
UCC3813D-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-1 3813D-1	Samples
UCC3813D-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-2 3813D-2	Samples
UCC3813D-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-2 3813D-2	Samples
UCC3813D-3	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-3 3813D-3	Samples
UCC3813D-3G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-3 3813D-3	Samples
UCC3813D-4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-4 3813D-4	Samples
UCC3813D-4G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-4	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										3813D-4	
UCC3813D-5	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-5 3813D-5	Samples
UCC3813D-5G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-5 3813D-5	Samples
UCC3813DTR-0	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-0 3813D-0	Samples
UCC3813DTR-0G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-0 3813D-0	Samples
UCC3813DTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-1 3813D-1	Samples
UCC3813DTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-1 3813D-1	Samples
UCC3813DTR-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-2 3813D-2	Samples
UCC3813DTR-3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-3 3813D-3	Samples
UCC3813DTR-3G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-3 3813D-3	Samples
UCC3813DTR-4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-4 3813D-4	Samples
UCC3813DTR-4G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-4 3813D-4	Samples
UCC3813DTR-5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-5 3813D-5	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3813DTR-5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3813 D-5 3813D-5	Samples
UCC3813N-0	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-0	Samples
UCC3813N-0G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-0	Samples
UCC3813N-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-1	Samples
UCC3813N-1G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-1	Samples
UCC3813N-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-2	Samples
UCC3813N-2G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-2	Samples
UCC3813N-3	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-3	Samples
UCC3813N-3G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-3	Samples
UCC3813N-4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-4	Samples
UCC3813N-4G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-4	Samples
UCC3813N-5	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3813N-5	Samples
UCC3813PW-0	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38130	Samples
UCC3813PW-1	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38131	Samples
UCC3813PW-2	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38132	Samples
UCC3813PW-3	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38133	Samples
UCC3813PW-4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38134	Samples

19-Feb-2015

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3813PW-4G4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38134	Samples
UCC3813PW-5	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38135	Samples
UCC3813PW-5G4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38135	Samples
UCC3813PWTR-0	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38130	Samples
UCC3813PWTR-0G4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38130	Samples
UCC3813PWTR-3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38133	Samples
UCC3813PWTR-3G4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38133	Samples
UCC3813PWTR-5	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	38135	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC2813-0, UCC2813-1, UCC2813-2, UCC2813-3, UCC2813-4, UCC2813-5 :

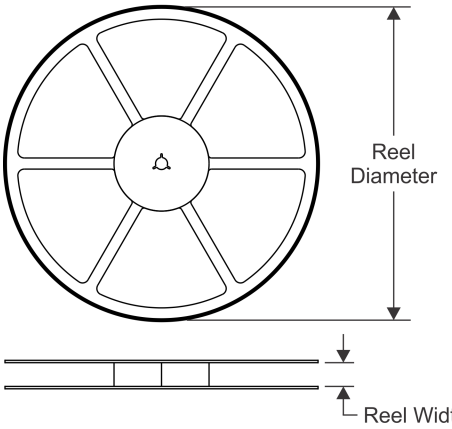
- Automotive: UCC2813-0-Q1, UCC2813-1-Q1, UCC2813-2-Q1, UCC2813-3-Q1, UCC2813-4-Q1, UCC2813-5-Q1

NOTE: Qualified Version Definitions:

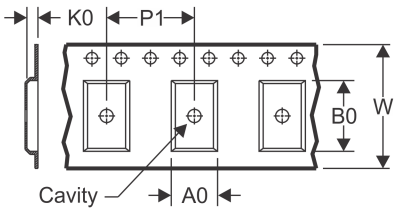
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

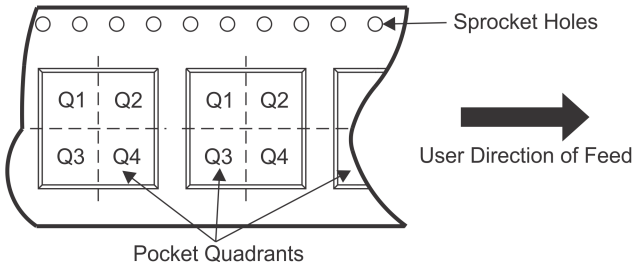


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



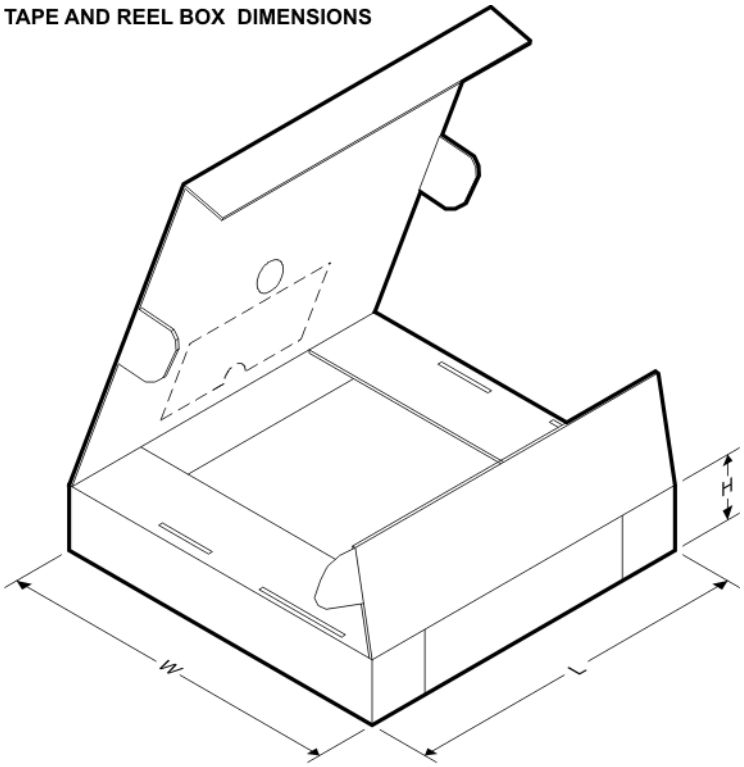
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2813DTR-0	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813DTR-3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813DTR-4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813DTR-5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2813PWTR-0	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2813PWTR-1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2813PWTR-3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2813PWTR-4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2813PWTR-5	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3813DTR-0	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3813DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3813DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3813DTR-3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3813DTR-4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3813DTR-5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

4-Mar-2015

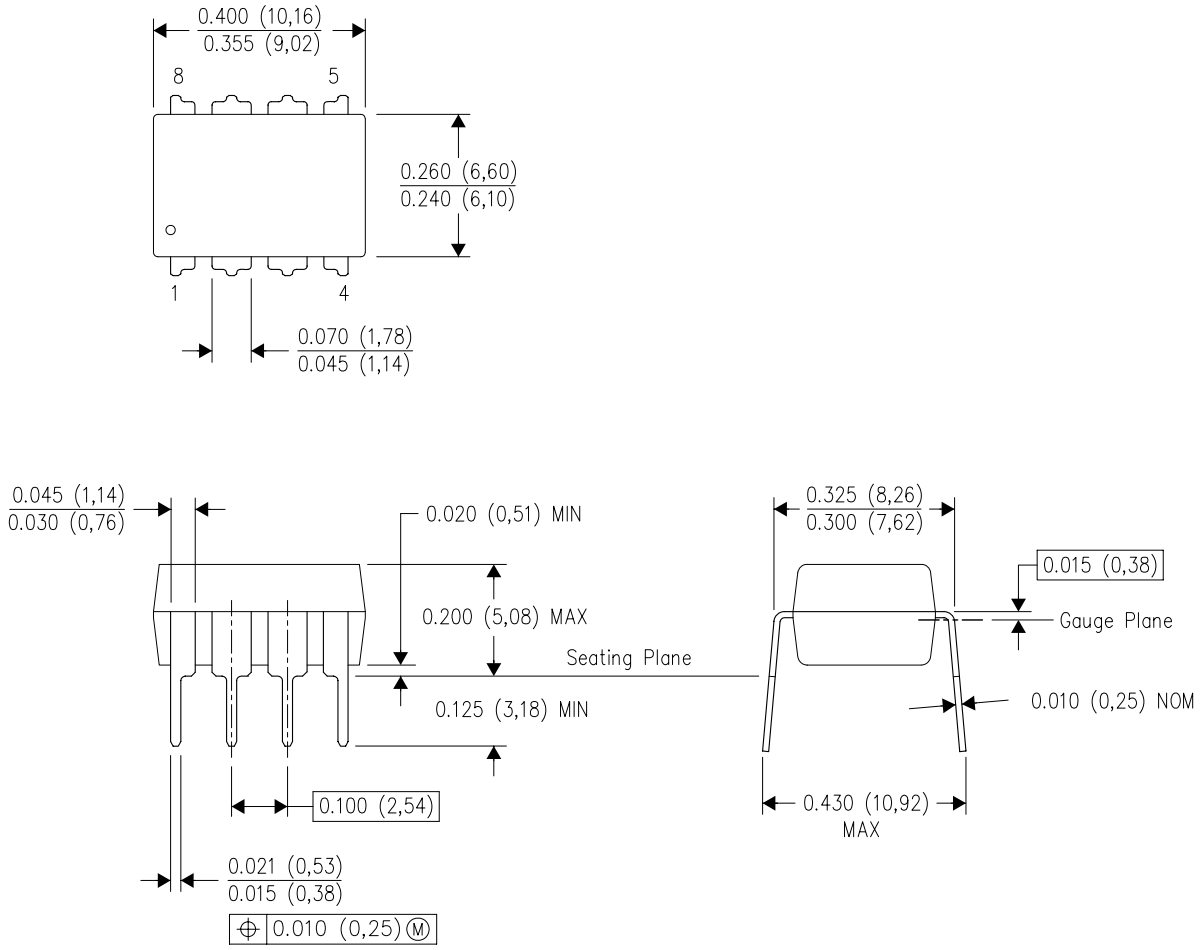
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2813DTR-0	SOIC	D	8	2500	340.5	338.1	20.6
UCC2813DTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC2813DTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC2813DTR-3	SOIC	D	8	2500	340.5	338.1	20.6
UCC2813DTR-4	SOIC	D	8	2500	340.5	338.1	20.6
UCC2813DTR-5	SOIC	D	8	2500	340.5	338.1	20.6
UCC2813PWTR-0	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC2813PWTR-1	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC2813PWTR-3	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC2813PWTR-4	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC2813PWTR-5	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3813DTR-0	SOIC	D	8	2500	340.5	338.1	20.6
UCC3813DTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC3813DTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC3813DTR-3	SOIC	D	8	2500	340.5	338.1	20.6
UCC3813DTR-4	SOIC	D	8	2500	340.5	338.1	20.6
UCC3813DTR-5	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

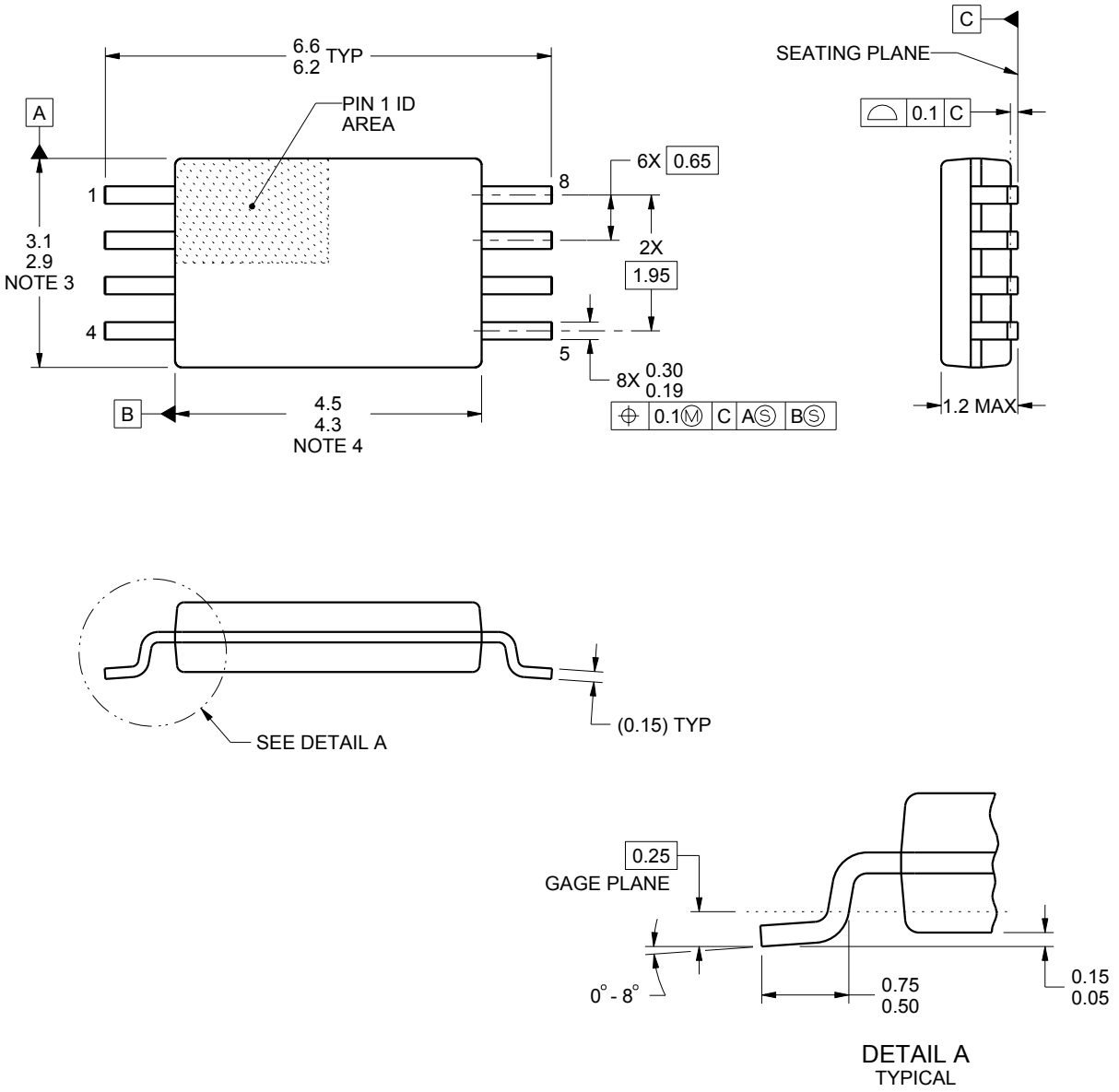
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

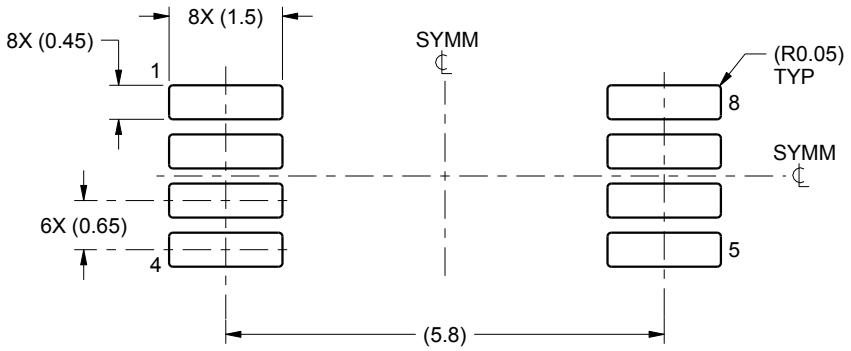
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

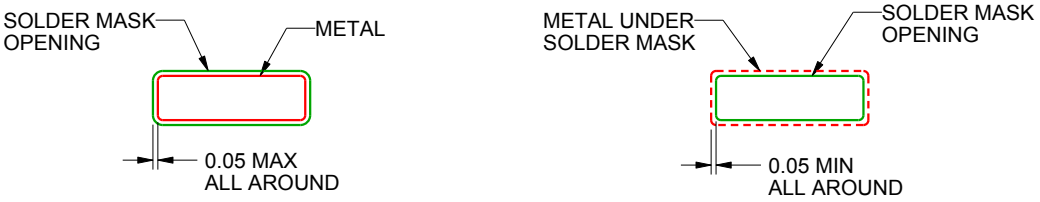


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

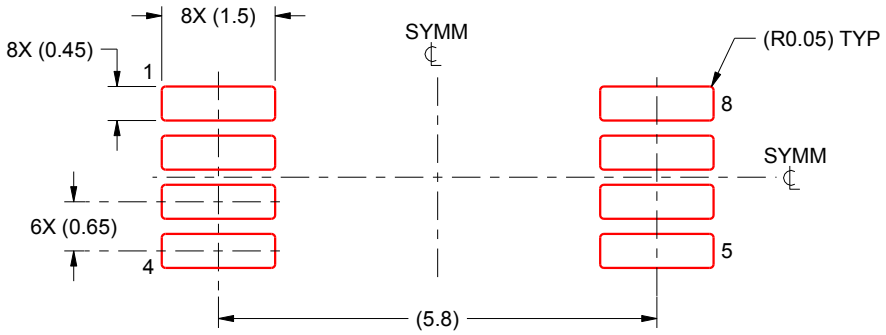
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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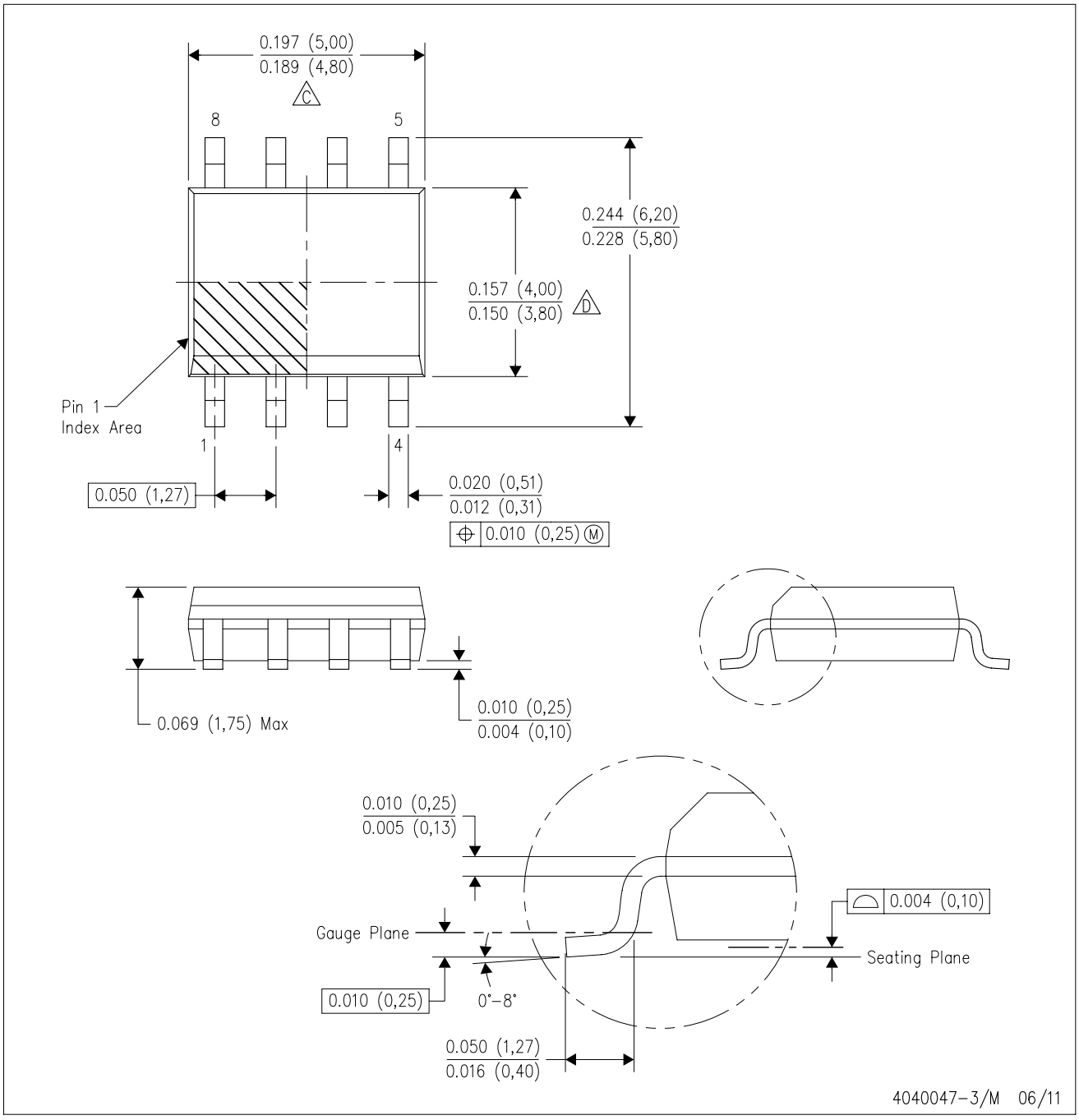
NOTES: (continued)

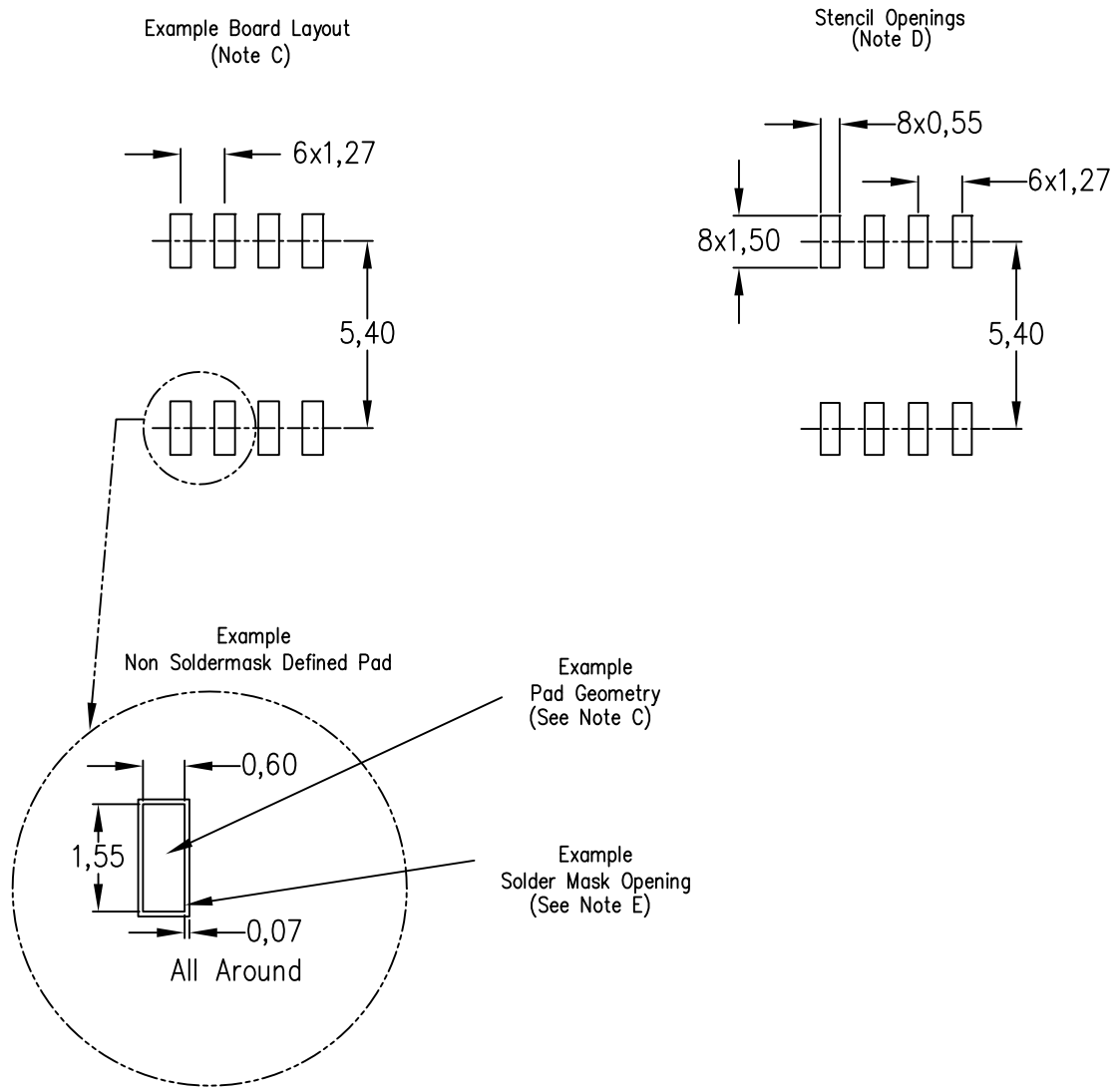
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.