



## 12-Bit, 31-MSPS, Dual-Channel CCD ANALOG FRONT-END FOR DIGITAL COPIERS

### FEATURES

- **Dual-Channel CCD Processing:**
  - Correlated Double Sampler (CDS)
  - Sample-and-Hold Mode (S/H)
  - Digital Programmable Amplifier
  - CCD Offset Correction (OB Loop)
- **High-Performance ADC:**
  - 12-Bit Resolution
  - INL:  $\pm 2$  LSB
  - DNL:  $\pm 0.5$  LSB
  - No Missing Codes Ensured
- **High-Speed Operation:**
  - Sample Rate: 31 MHz (max, Design Ensured)
  - 78-dB SNR (at 0-dB Gain)
- **Low-Power Consumption:**
  - Low Voltage: 3.0 V to 3.6 V
  - Low Power: 290 mW (typ at 3.3 V)
  - Standby Mode: 20 mW (typ)

### APPLICATIONS

- Copiers
- Scanners
- Facsimiles

### DESCRIPTION

The VSP5010 is a complete application-specific standard product (ASP) for charge-coupled device (CCD) line sensor applications such as copiers, scanners, and facsimiles. The VSP5010 provides two independent line-processing channels, and performs analog front-end (AFE) data processing and analog-to-digital conversion. Each channel features correlated double sampling (CDS) and sample-and-hold (S/H) processing stages, 14 analog-to-digital converter (ADC) blocks, a digital programmable gain amplifier (DPGA), and an optical black (OB) correction loop. Data are output in a 12-bit word; two-channel ADC data are multiplexed and then output.

The VSP5010 operates from a single 3.3-V supply. The device is available in an LQFP-64 package.

**PRODUCT PREVIEW**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP5010PM	NRND	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM	-25 to 85	VSP5010	
VSP5010PMG6	NRND	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM	-25 to 85	VSP5010	
VSP5010PMR	NRND	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM	-25 to 85	VSP5010	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

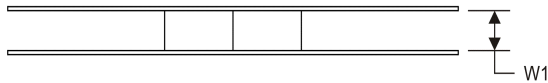
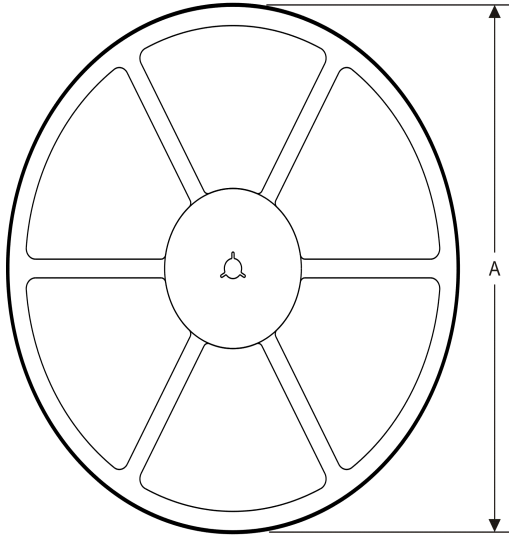
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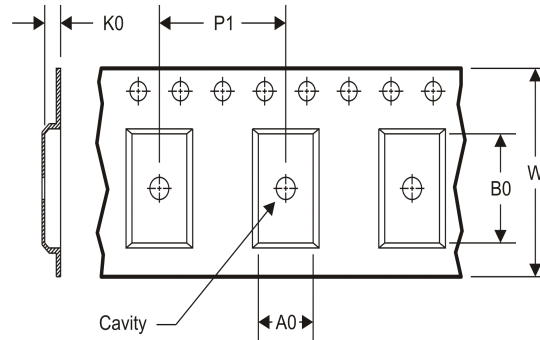
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



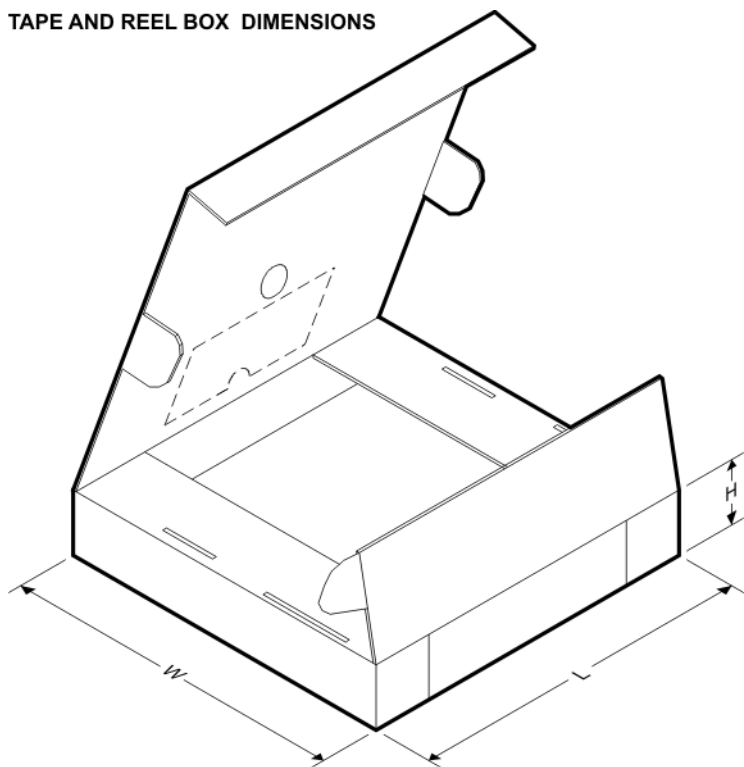
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5010PMR	LQFP	PM	64	1000	330.0	25.4	12.8	12.8	1.9	16.0	24.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

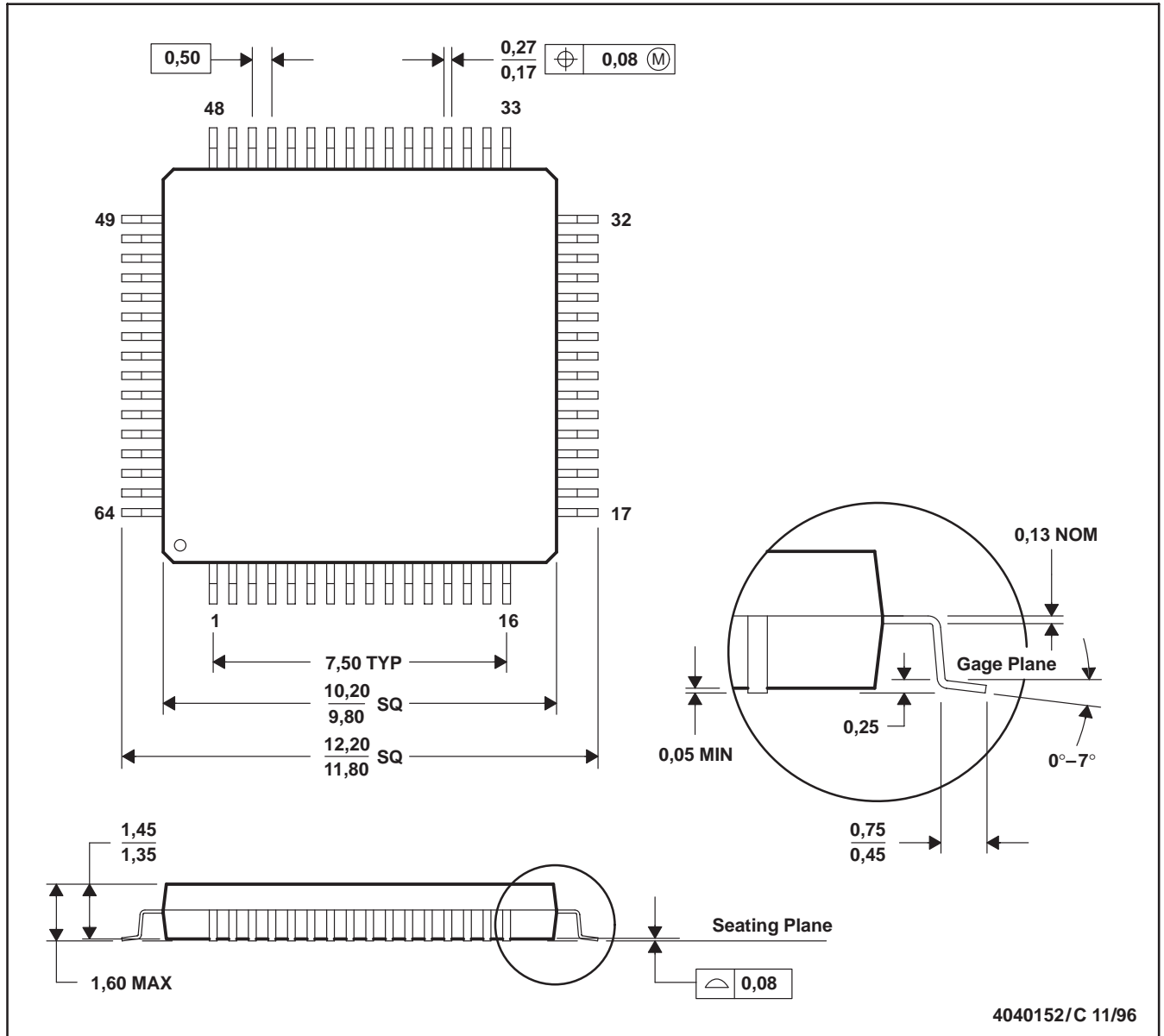


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5010PMR	LQFP	PM	64	1000	367.0	367.0	45.0

PM (S-PQFP-G64)

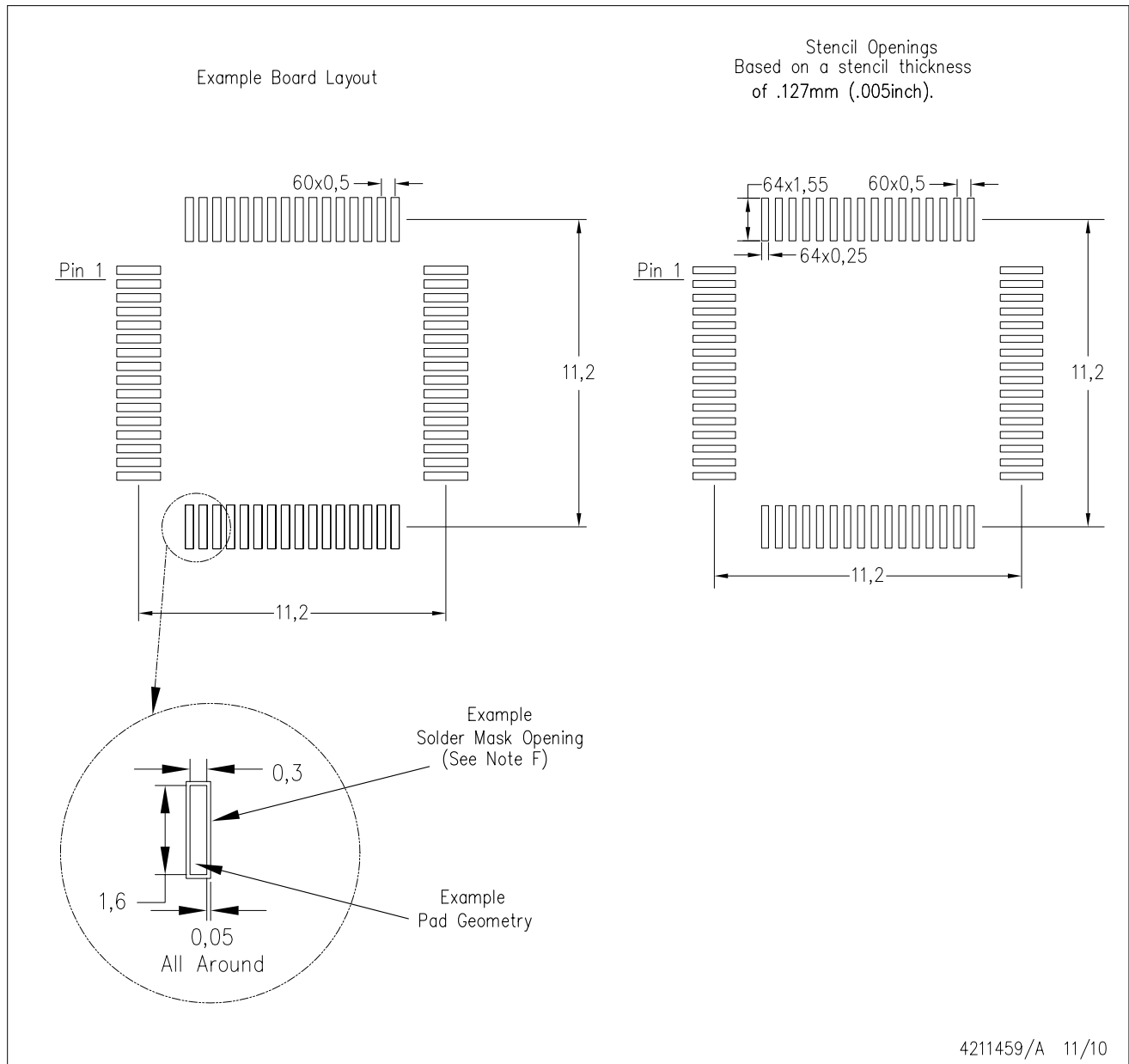
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026  
 D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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