



MLC e·MMC™ and Mobile LPDDR2 162-Ball MCP

MT29PZZZ8D5BKFTF-18 W.95L

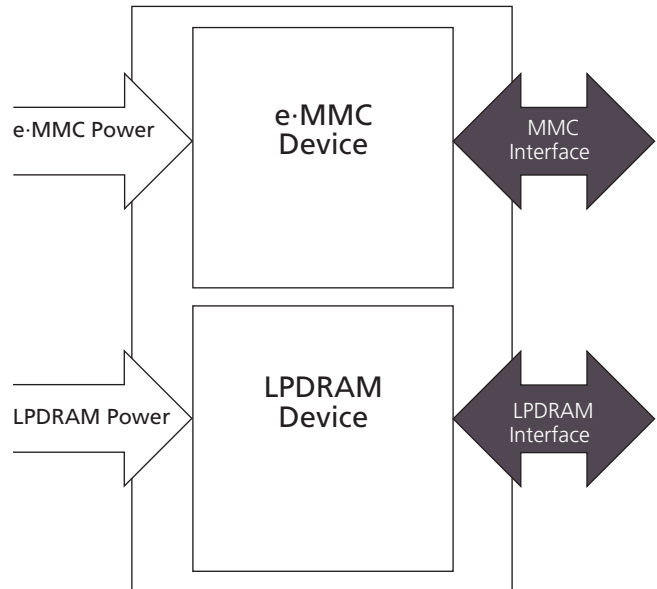
Features

- Micron® e·MMC and LPDDR2 components
- MLC NAND Flash in e·MMC
- RoHS-compliant, “green” package
- Separate e·MMC and LPDDR2 interfaces
- Space-saving multichip package
- Low-voltage operation V_{DD} (1.70–1.95V)
- Dual voltage V_{CCQM} (1.70–1.95V, 2.7–3.6V)
- Wireless temperature range: –30°C to +85°C

e·MMC-Specific Features

- JEDEC/MMC standard version 4.51-compliant SPI mode not supported¹
 - Advanced 11-signal interface
 - x1, x4, and x8 I/Os, selectable by host
 - SDR/DDR modes up to 52 MHz clock speed
 - HS200 mode
 - Real-time clock
 - Command classes: class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
 - Temporary write protection
 - Boot operation (high-speed boot)
 - Sleep mode
 - Replay-protected memory block (RPMB)
 - Secure erase and secure trim
 - Hardware reset signal
 - Multiple partitions with enhanced attribute
 - Permanent and power-on write protection
 - High-priority interrupt (HPI)
 - Background operation
 - Reliable write
 - Discard and sanitize
 - Extended partitioning
 - Context ID and data TAG
 - Packed commands
 - Thermal specification
 - Backward compatible with previous MMC
- ECC and block management implemented

Note: 1. JEDEC Standard No. 84-B451 specification is at www.jedec.org/sites/default/files/docs/JESD84-B451.pdf.

Figure 1: MCP Block Diagram


Mobile-LPDDR2-Specific Features

- Ultra-low-voltage 1.2V core power supply
- 1.2V HSUL-compatible inputs
- Programmable read and write latencies
- Programmable burst lengths: 4, 8, or 16
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- Adjustable clock frequency and clock stop capabilities

Note: 1. For physical part markings, see Part Numbering Information (page 2).

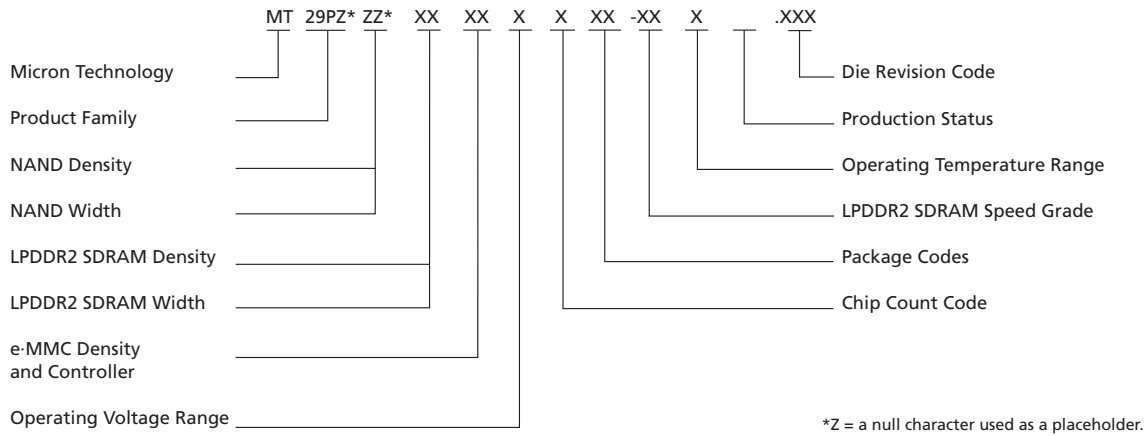


8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Features

Part Numbering Information

Micron NAND Flash and LPDRAM devices are available in different configurations and densities. The MCP/PoP part numbering guide is available at www.micron.com/numbering.

Figure 2: Part Number Chart



Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/support.



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8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP MCP General Description

MCP General Description

Micron MCP products combine *e*-MMC and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The *e*-MMC and Mobile LPDRAM devices are also members of the Micron discrete memory products portfolio.

The *e*-MMC and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate *e*-MMC and Mobile LPDRAM buses. The *e*-MMC and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, V_{SS} is tied together on the two devices).

The bus architecture of this device also supports separate *e*-MMC and Mobile LPDRAM functionality without concern for device interaction.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Ball Assignments and Descriptions

Ball Assignments and Descriptions

Figure 3: 162-Ball VFBGA (e-MMC; x32 LPDDR2) Ball Assignments

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	DAT0	DAT6	V _{DDIM}	DAT5	DAT3	V _{CCM}	DNU	DNU
B	DNU	V _{CCM}	DAT1	DAT7	CLK	DAT4	DAT2	V _{CCQM}	V _{SS}	DNU
C	RST_n	NC	V _{SSQ}	NC	CMD	NC				
D	NC	NC	NC	NC	NC	NC				
E	V _{SS}	NC	NC		V _{DD2}	V _{DD1}	DQ31	DQ29	DQ26	DNU
F	V _{DD1}	V _{SS}	NC		V _{SS}	V _{SSQ}	V _{DDQ}	DQ25	V _{SS}	V _{DDQ}
G	V _{SS}	V _{DD2}	ZQ0		V _{DDQ}	DQ30	DQ27	DQS3_t	DQS3_c	V _{SSQ}
H	V _{SS}	CA9	CA8		DQ28	DQ24	DM3	DQ15	V _{DDQ}	V _{SSQ}
J	NC	CA6	CA7		V _{SSQ}	DQ11	DQ13	DQ14	DQ12	V _{DDQ}
K	V _{DD2}	CA5	V _{REFCA}		DQS1_c	DQS1_t	DQ10	DQ9	DQ8	V _{SSQ}
L	NC	V _{SS}	CK_c		DM1	V _{DDQ}				
M	V _{SS}	NC	CK_t		V _{SSQ}	V _{DDQ}	V _{DD2}	V _{SS}	V _{REFDQ}	
N	CKE0	CKE1	NC		DM0	V _{DDQ}				
P	CS0_n	CS1_n	NC		DQS0_c	DQS0_t	DQ5	DQ6	DQ7	V _{SSQ}
R	CA4	CA3	CA2		V _{SSQ}	DQ4	DQ2	DQ1	DQ3	V _{DDQ}
T	V _{SS}	NC	CA1		DQ19	DQ23	DM2	DQ0	V _{DDQ}	V _{SSQ}
U	V _{SS}	V _{DD2}	CA0		V _{DDQ}	DQ17	DQ20	DQS2_t	DQS2_c	V _{SSQ}
V	V _{DD1}	V _{SS}	NC		V _{SS}	V _{SSQ}	V _{DDQ}	DQ22	V _{SSQ}	V _{DDQ}
W	DNU	NC	NC		V _{DD2}	V _{DD1}	DQ16	DQ18	DQ21	DNU
Y	DNU	DNU							DNU	DNU

Top View (ball down)





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Ball Assignments and Descriptions

Table 1: e-MMC Ball Descriptions

Symbol	Type	Description
CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	Input/output	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open drain for initialization. 2) Push-pull for fast command transfer.
DAT[7:0]	Input/output	Data bus: Bidirectional channel used for data transfer.
RST_n	Input	Reset
V _{CCM}	Supply	V _{CCM} : NAND I/F I/O and NAND power supply (2.70–3.6V).
V _{CCQM}	Supply	V _{CCQM} : e-MMC controller core and e-MMC I/F I/O power supply (1.70–1.95V).
V _{DDIM}	–	V _{DDIM} : The internal regulator connection to an external decoupling capacitor (see the Capacitor and Resistance Specifications table).

Table 2: x32 LPDDR2 Ball Descriptions

Symbol	Type	Description
CA[9:0]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All CA inputs are sampled on both the positive and negative edge of CK. CS and CKE inputs are sampled at the positive edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	Clock enable: For a single-die LPDDR2 MCP, only CKE0 is used. CKE1 is used in case of dual-die LPDDR2 MCP.
CS[1:0]_n	Input	Chip select: For a single-die LPDDR2 MCP, only CS0_n is used. CS1_n is used in case of dual-die LPDDR2 MCP.
DM[3:0]	Input	Data mask: DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	Input/output	Data bus: Data inputs/outputs.
DQS[3:0]_t, DQS[3:0]_c	Input/output	Data strobe: Coordinates READ/WRITE transfers of data; one DQS_t/DQS_c pair per DQ byte.
V _{DD1}	Supply	V _{DD1} : LPDDR2 power supply 1.
V _{DD2}	Supply	V _{DD2} : LPDDR2 power supply 2.
V _{DDQ}	Supply	V _{DDQ} : LPDDR2 I/O power supply.
V _{REFCA}	Supply	V _{REFCA} : LPDDR2 reference for CA pins.
V _{REFDQ}	Supply	V _{REFDQ} : LPDDR2 reference for DQ pins.
V _{SSQ}	Supply	V _{SSQ} : LPDDR2 I/O ground. It is internally connected to V _{SS} .



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Ball Assignments and Descriptions

Table 2: x32 LPDDR2 Ball Descriptions (Continued)

Symbol	Type	Description
ZQ0	Input	External reference ball for output drive calibration: Tied to an external 240Ω resistor (RZQ), which is tied to ground.

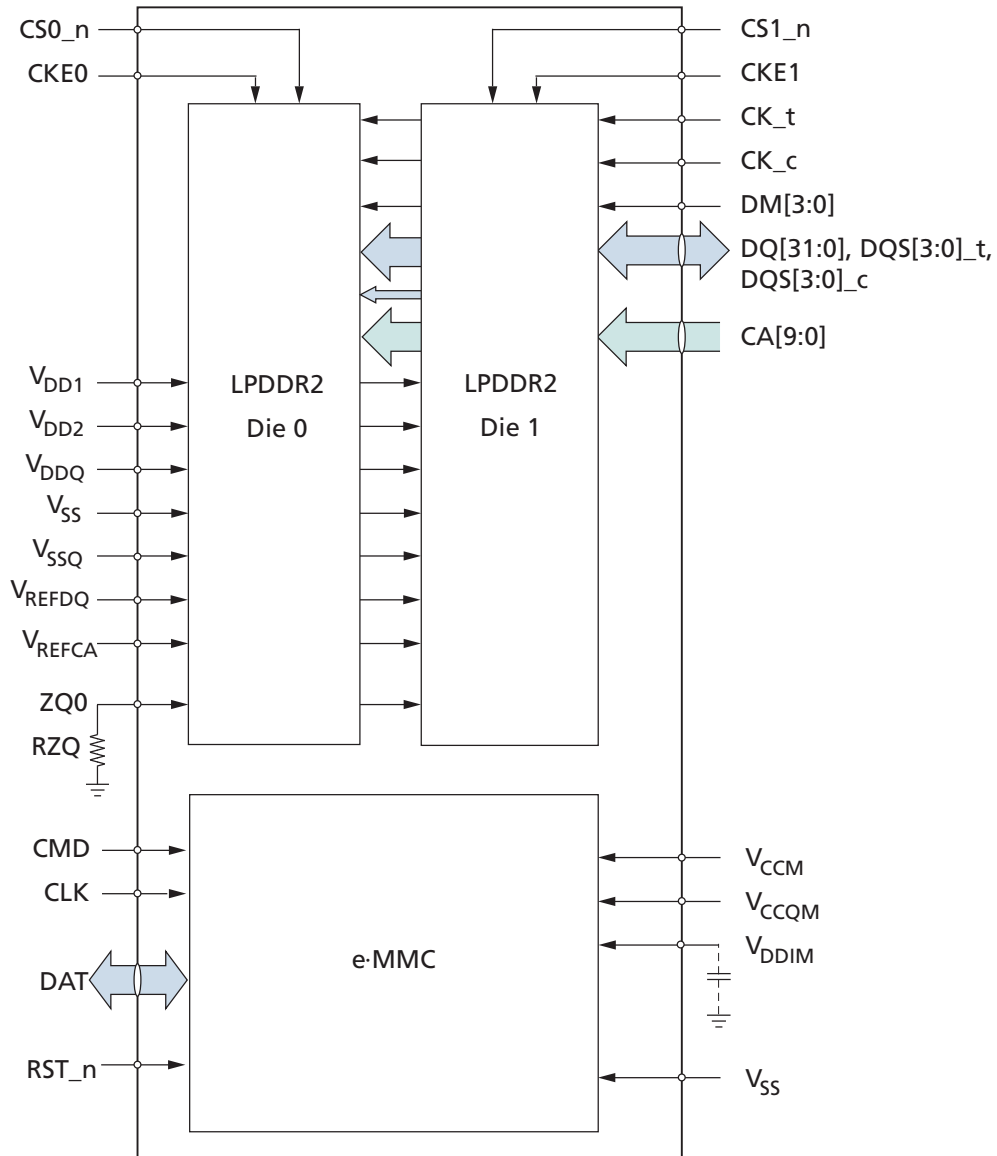
Table 3: Non-Device-Specific Descriptions

Symbol	Type	Description
V _{SS}	Supply	V _{SS} : Shared ground.
Symbol	Type	Description
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.



Device Diagrams

Figure 4: Functional Block Diagram – e-MMC and Dual-Die x32 LPDDR2



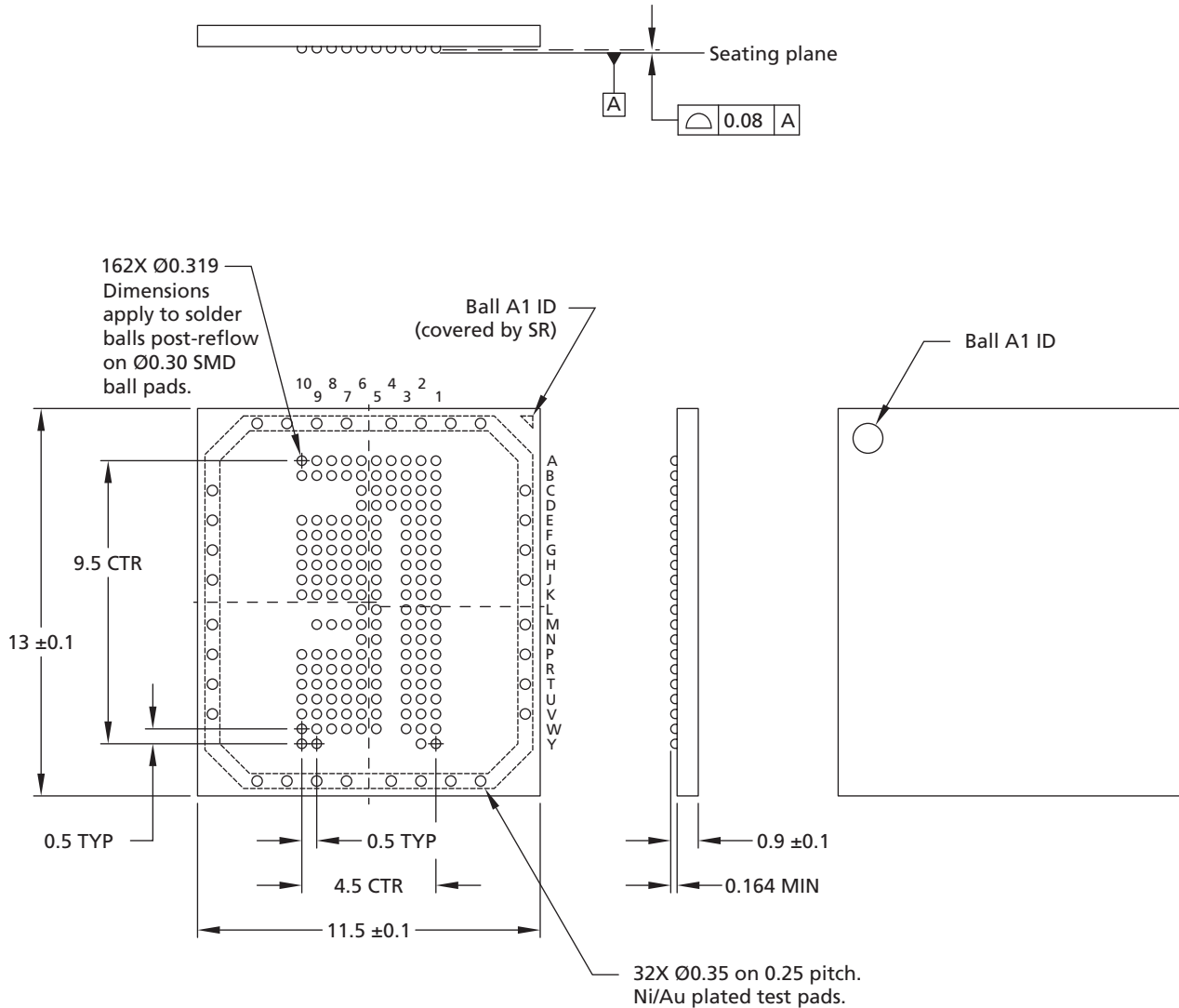
Note: 1. V_{SS} and V_{SSQ} are internally connected.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Package Dimensions

Package Dimensions

Figure 5: 162-Ball VFBGA (Package Code: TF)



- Notes:
1. All dimensions are in millimeters.
 2. Solder ball material: LF35 with Cu OSP ball pads (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).



4GB, 8GB e-MMC™ Memory

CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by *e*-MMC protocol. Each device is created with a unique identification number.

Table 4: CID Register Field Parameters

Name	Field	Width	CID Bits	CID Value
Manufacturer ID	MID	8	[127:120]	FEh
Reserved	–	6	[119:114]	–
Card/BGA	CBX	2	[113:112]	01h
OEM/application ID	OID	8	[111:104]	4Eh
Product name	PNM	48	[103:56]	50314A39354Ch
Product revision	PRV	8	[55:48]	12h
Product serial number	PSN	32	[47:16]	–
Manufacturing date	MDT	8	[15:8]	–
CRC7 checksum	CRC	7	[7:1]	–
Not used; always 1	–	1	[0]	–



OCR Register

The 32-bit operation conditions register (OCR) stores the V_{DD} voltage profile of the card and the access mode indication. In addition, this register includes a status information bit.

Table 5: OCR Parameters

OCR Bits	OCR Value	Description
[31]	1b (ready)/0b (busy) ¹	Device power-on status bit
[30:29]	10b	Sector mode
[28:24]	0 0000b	Reserved
[23:15]	1 1111 1111b	V_{DD} : 2.7–3.6V range
[14:8]	000 0000b	V_{DD} : 2.0–2.7V range
[7]	1b	V_{DD} : 1.70–1.95V range
[6:0]	000 0000b	Reserved

Note: 1. OCR = C0FF8080h after the device has completed power-up.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP CSD Register

CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DSR register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 6: CSD Register Field Parameters

Name	Field	Size (Bits)	Cell Type ¹	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	03h
System specification version	SPEC_VERS	4	R	[125:122]	04h
Reserved ²	–	2	–	[121:120]	–
Data read access time 1	TAAC	8	R	[119:112]	6Eh
Data read access time 2 in CLK cycles (NSAC × 100)	NSAC	8	R	[111:104]	01h
Maximum bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Card command classes ³	CCC	12	R	[95:84]	0F5h
Maximum read data block length	READ_BL_LEN	4	R	[83:80]	09h
Partial blocks for reads supported	READ_BL_PARTIAL	1	R	[79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77]	0h
DSR implemented ⁴	DSR_IMP	1	R	[76]	1h
Reserved	–	2	–	[75:74]	–
Device size	C_SIZE	12	R	[73:62]	FFFh
Maximum read current at V _{DD,min}	VDD_R_CURR_MIN	3	R	[61:59]	07h
Maximum read current at V _{DD,max}	VDD_R_CURR_MAX	3	R	[58:56]	07h
Maximum write current at V _{DD,min}	VDD_W_CURR_MIN	3	R	[55:53]	07h
Maximum write current at V _{DD,max}	VDD_W_CURR_MAX	3	R	[52:50]	07h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	07h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	4GB	R	[36:32]	07h
		8GB			0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	00h
Write-speed factor	R2W_FACTOR	3	R	[28:26]	04h
Maximum write data block length	WRITE_BL_LEN	4	R	[25:22]	09h
Partial blocks for writes supported	WRITE_BL_PARTIAL	1	R	[21]	0h
Reserved	–	4	–	[20:17]	–
Content protection application	CONTENT_PROT_APP	1	R	[16]	0h
File-format group	FILE_FORMAT_GRP	1	R/W	[15]	0h



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP CSD Register

Table 6: CSD Register Field Parameters (Continued)

Name	Field	Size (Bits)	Cell Type ¹	CSD Bits	CSD Value
Copy flag (OTP)	COPY	1	R/W	[14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	00h
ECC	ECC	2	R/W/E	[9:8]	00h
CRC	CRC	7	R/W/E	[7:1]	–
Reserved	–	1	–	[0]	–

- Notes:
1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable
 2. Reserved bits should be read as 0.
 3. CM0 restriction: CMD0 (SW RESET) is not supported during programming command. If SW RESET is issued during programming commands, a power cycle is required.
 4. The $I_{PEAK, max}$ driving capability can be modified according to the actual capacitive load on the e-MMC interface signals in the user application board, using CMD4. In HS200 mode, the driver strength value is set in EXT_CSD[185], using CMD6.

CMD4 Argument	Driving Capability (mA)
0x01000000	4
0x02000000	8
0x04000000	12 (default)
0x08000000	16
0x10000000	20
0x20000000	24
0x40000000	28
0x80000000	32



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP ECSD Register

ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 7: ECSD Register Field Parameters

Name	Field	Size (Bytes)	Cell Type ¹	ECSD Bytes	ECSD Value	
Properties Segment						
Reserved ²	–	7	–	[511:505]	–	
Supported command sets	S_CMD_SET	1	R	[504]	01h	
HPI features	HPI_FEATURES	1	R	[503]	03h	
Background operations support	BKOPS_SUPPORT	1	R	[502]	01h	
Max-packed read commands	MAX_PACKED_READS	1	R	[501]	3Ch	
Max-packed write commands	MAX_PACKED_WRITES	1	R	[500]	20h	
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	01h	
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	03h	
Tag resources size	TAG_RES_SIZE	1	R	[497]	00h	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	05h	
Large unit size	LARGE_UNIT_SIZE_M1	4GB	1	R	[495]	03h
		8GB			07h	
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	03h	
Reserved	–	241	–	[493:253]	–	
Cache size	CACHE_SIZE	4	R	[252:249]	00000100h	
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	64h	
Power-off notification (long) timeout	POWER_OFF_LONG_TIM	1	R	[247]	FFh	
Background operations status	BKOPS_STATUS	1	R	[246]	00h	
Number of correctly programmed sectors	CORRECTLY_PROG_SECTORS_NUM	4	R	[245:242]	00000000h	
First initialization time after partitioning (first CMD1 to device ready)	INI_TIMEOUT_AP	1	R	[241]	32h	
Reserved	–	1	–	[240]	–	
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	04h	
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	09h	
Power class for 200 MHz at 1.95V	PWR_CL_200_195	1	R	[237]	09h	
Power class for 200 MHz, at 1.3V	PWR_CL_200_130	1	R	[236]	00h	
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	00h	


**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
ECSD Register**
Table 7: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type ¹	ECSD Bytes	ECSD Value	
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	00h	
Reserved	–	1	–	[233]	–	
TRIM multiplier	TRIM_MULT	1	R	[232]	03h	
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	55h	
Secure erase multiplier	SEC_ERASE_MULT	1	R	[230]	06h	
Secure trim multiplier	SEC_TRIM_MULT	1	R	[229]	09h	
Boot information	BOOT_INFO	1	R	[228]	07h	
Reserved	–	1	–	[227]	–	
Boot partition size	BOOT_SIZE_MULT	4GB	1	R	[226]	08h
		8GB				10h
Access size	ACC_SIZE	4GB	1	R	[225]	06h
		8GB				07h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	4GB	1	R	[224]	08h
		8GB				10h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	01h	
Reliable write-sector count	REL_WR_SEC_C	1	R	[222]	01h	
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	01h	
Sleep current (V _{CC})	S_C_VCC	1	R	[220]	06h	
Sleep current (V _{CCQ})	S_C_VCCQ	1	R	[219]	0Ah	
Reserved	–	1	–	[218]	–	
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	10h	
Reserved	–	1	–	[216]	–	
Sector count	SEC_COUNT	4GB	4	R	[215:212]	0074C000h
		8GB				00E98000h
Reserved	–	1	–	[211]	–	
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	08h	
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	08h	
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	08h	
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	08h	
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	08h	
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	08h	
Reserved	–	1	–	[204]	–	



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP ECSD Register

Table 7: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type ¹	ECSD Bytes	ECSD Value
Power class for 26 MHz at 3.6V	PWR_CL_26_360	1	R	[203]	02h
Power class for 52 MHz at 3.6V	PWR_CL_52_360	1	R	[202]	02h
Power class for 26 MHz at 1.95V	PWR_CL_26_195	1	R	[201]	05h
Power class for 52 MHz at 1.95V	PWR_CL_52_195	1	R	[200]	05h
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	03h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0Ah
I/O driver strength	DRIVER_STRENGTH	1	R	[197]	0Fh
Card type	CARD_TYPE	1	R	[196]	17h
Reserved	–	1	–	[195]	–
CSD structure version	CSD_STRUCTURE	1	R	[194]	02h
Reserved	–	1	–	[193]	–
Extended CSD revision	EXT_CSD_REV	1	R	[192]	06h
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	00h
Reserved	–	1	–	[190]	–
Command set revision	CMD_SET_REV	1	R	[189]	00h
Reserved	–	1	–	[188]	–
Power class	POWER_CLASS	1	R/W/E_P	[187]	00h
Reserved	–	1	–	[186]	–
High-speed interface timing ⁴	HS_TIMING	1	R/W/E_P	[185]	00h
Reserved	–	1	–	[184]	–
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	00h
Reserved	–	1	–	[182]	–
Erased memory content	ERASED_MEM_CONT	1	R	[181]	00h
Reserved	–	1	–	[180]	–
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	00h
Boot configuration protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	00h
Boot bus width	BOOT_BUS_WIDTH	1	R/W/E	[177]	00h
Reserved	–	1	–	[176]	–
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	00h
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	00h
Boot area write protection register	BOOT_WP	1	R/W, R/W/C_P	[173]	00h
Reserved	–	1	–	[172]	–



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP ECSD Register

Table 7: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type ¹	ECSD Bytes	ECSD Value
User write protection register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	00h
Reserved	–	1	–	[170]	–
Firmware configuration	FW_CONFIG	1	R/W	[169]	00h
RPMB size	RPMB_SIZE_MULT	4GB	R	[168]	08h
		8GB			10h
Write reliability setting register ³	WR_REL_SET	1	R/W	[167]	1Fh
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	05h
SANITIZE START operation	SANITIZE_START	1	W/E_P	[165]	00h
Manually start background operations	BKOPS_START	1	W/E_P	[164]	00h
Enable background operations hand-shake	BKOPS_EN	1	R/W	[163]	00h
Hardware reset function	RST_n_FUNCTION	1	R/W	[162]	00h
HPI management	HPI_MGMT	1	R/W/E_P	[161]	00h
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	07h
Maximum enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0001D3h
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	00h
Partitioning setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	00h
General-purpose partition size	GP_SIZE_MULT_GP3	12	R/W	[154:152]	000000h
	GP_SIZE_MULT_GP2			[151:149]	000000h
	GP_SIZE_MULT_GP1			[148:146]	000000h
	GP_SIZE_MULT_GP0			[145:143]	000000h
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	000000h
Enhanced user data start address	ENH_START_ADDR	4	R/W	[139:136]	00000000h
Reserved	–	1	–	[135]	–
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	00h
Reserved	–	1	–	[133]	–
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	00h
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	00h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	01h
Reserved	–	2	TBD	[129:128]	–
Vendor specific fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	00h
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	00h
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	00h
Sector size	DATA_SECTOR_SIZE	1	R	[61]	00h


Table 7: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type ¹	ECSD Bytes	ECSD Value
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0Ah
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	00h
Number of addressed group to be re-released	DYNCAP_NEEDED	1	R	[58]	00h
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0000h
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0000h
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0000h
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	-
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	00h
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	00h
Power-off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	00h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	00h
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	00h
Reserved	-	32	TBD	[31:0]	-

- Notes:
1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable;
R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable
 2. Reserved bits should be read as 0.
 3. Micron has tested power failure under best-application knowledge conditions with positive results. Customers may request a dedicated test for their specific application condition. Micron set this register during factory test and used the one-time programming option.
 4. [†]H parameter in HS200 is 1.3ns. Refer to the JEDEC specification for the output timing diagram.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP e-MMC Performance and Current Consumption

e-MMC Performance and Current Consumption

Table 8: MLC Partition Performance

Condition ¹		Typical Values		Unit
		4GB	8GB	
Sequential Write	Cache On	12	23	MB/s
	Cache Off	10	19	MB/s
Sequential Read		75	120	MB/s
Random Write	Cache On	1510	2350	IOPS
	Cache Off	655	890	IOPS
Random Read		3290	3850	IOPS

Note: 1. Bus in x8 I/O and HS200 modes. Sequential access of 512KB chunk; random access of 4KB chunk over ~5% of the user area span (lower than 1GB). Additional performance data, such as system performance on a specific application board, will be provided in a separate document upon customer request.

Table 9: Current Consumption

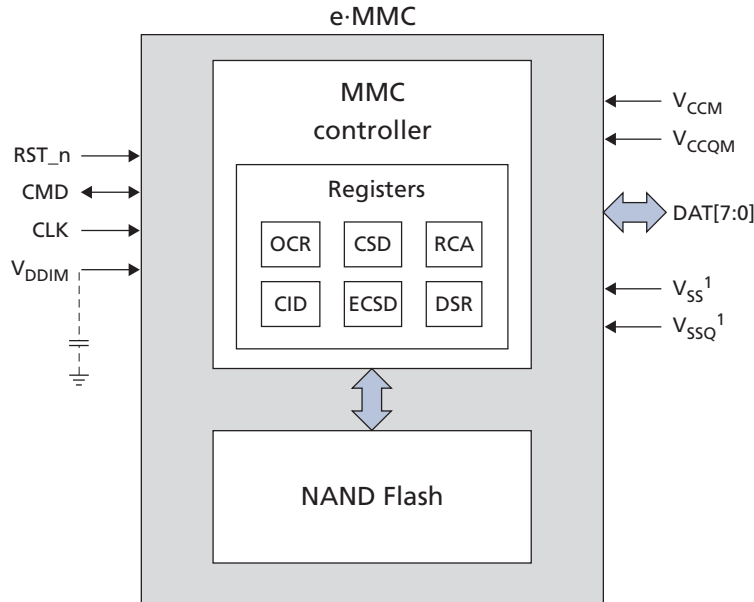
Condition ¹	Typical Values (I_{CC}/I_{CCQ})		Unit
	4GB	8GB	
Write	45/15	70/15	mA
Read	55/30	85/35	mA
Sleep	0/110	0/120	uA
Auto-Standby	30/110	45/115	uA

Note: 1. Bus in x8 I/O and HS200 modes. $V_{CC} = 3.6V$ and $V_{CCQ} = 1.95V$. 25°C. Measurements done as average RMS current consumption. I_{CCQ} in READ operation might be affected by tester load.



Architecture

Figure 6: e-MMC Functional Block Diagram



Note: 1. V_{SS} and V_{SSQ} are internally connected.

MMC Protocol Independent of NAND Flash Technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the NAND Flash features included in the device. The device has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block management functions such as logical block allocation and wear leveling. These management functions require complex algorithms and depend entirely on NAND Flash technology (generation or memory cell type).

The device handles these management functions internally, making them invisible to the host processor.

Defect and Error Management

Micron e-MMC incorporates advanced technology for defect and error management. If a defective block is identified, the device completely replaces the defective block with one of the spare blocks. This process is invisible to the host and does not affect data space allocated for the user.

The device also includes a built-in error correction code (ECC) algorithm to ensure that data integrity is maintained.

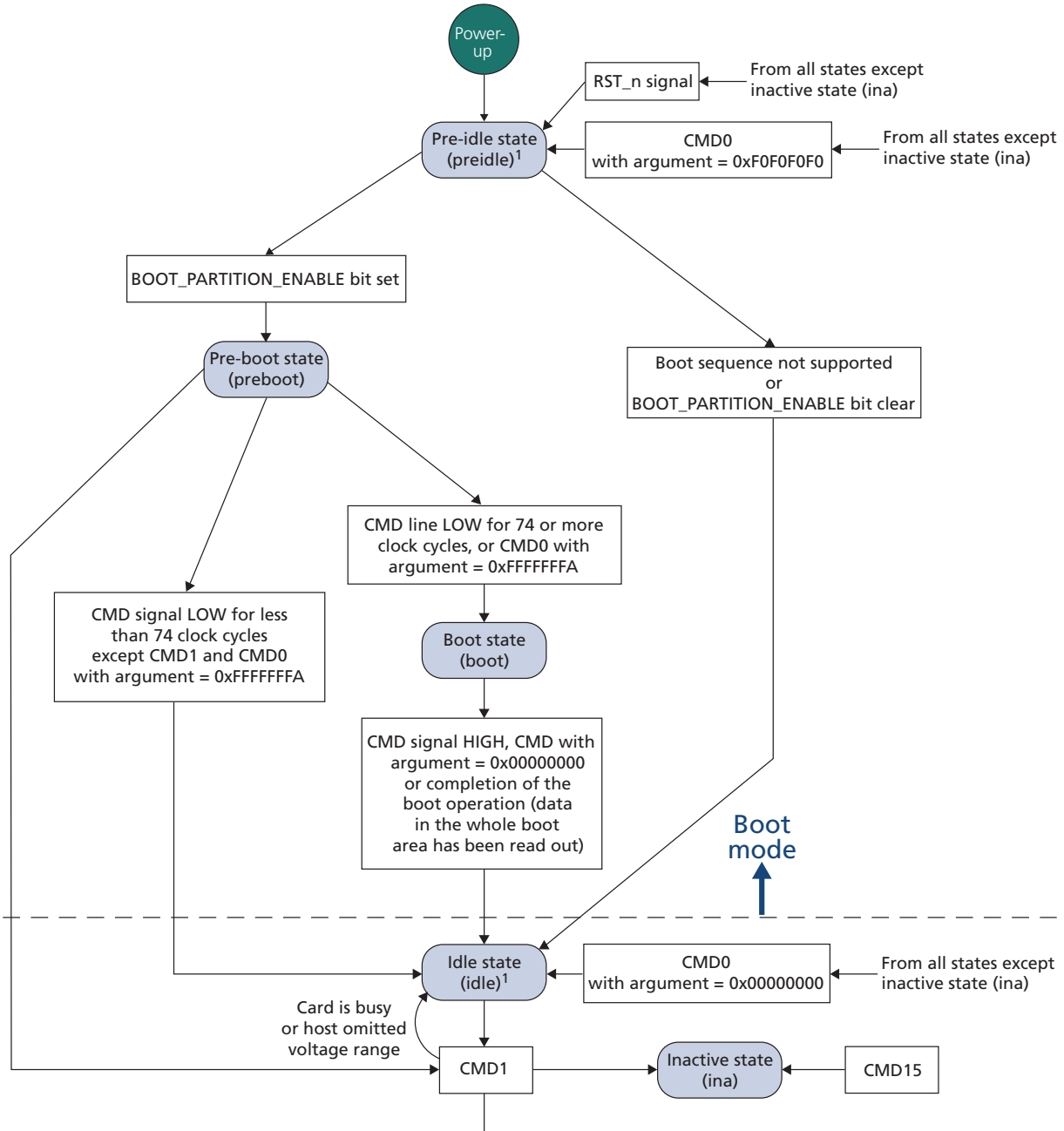
To make the best use of these advanced technologies and ensure proper data loading and storage over the life of the device, the host must exercise the following precautions:

- Check the status after WRITE, READ, and ERASE operations.
- Avoid power-down during WRITE and ERASE operations.



State Diagrams

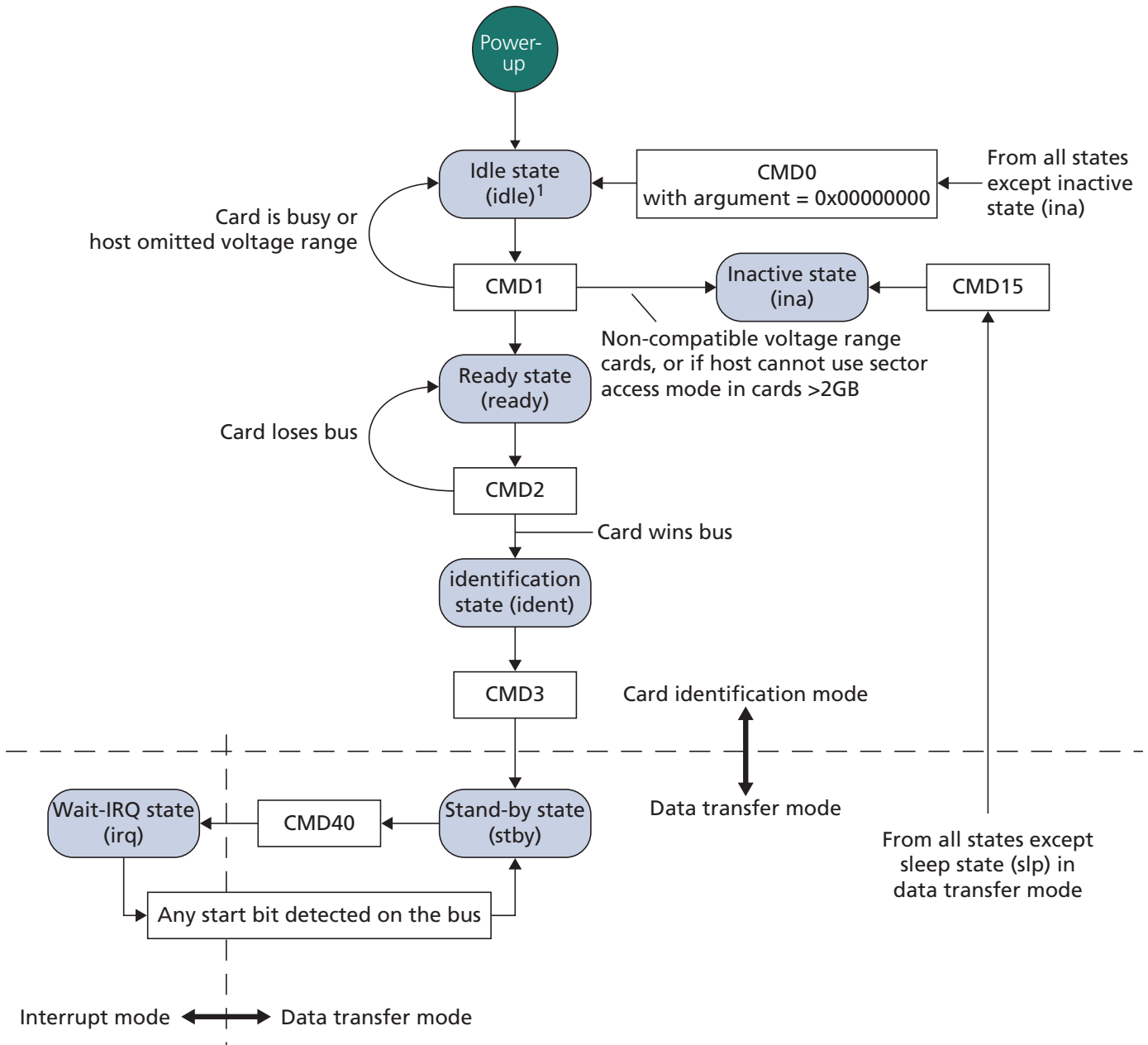
Figure 7: Boot Mode



Note: 1. When the part is in idle or pre-idle state, any invalid command may show ILLEGAL_COMMAND in the status register on the first command with R1 response. For example, CMD55 may cause a CMD3 response to show an illegal command status during the initialization sequence.



Figure 8: Card Identification Mode

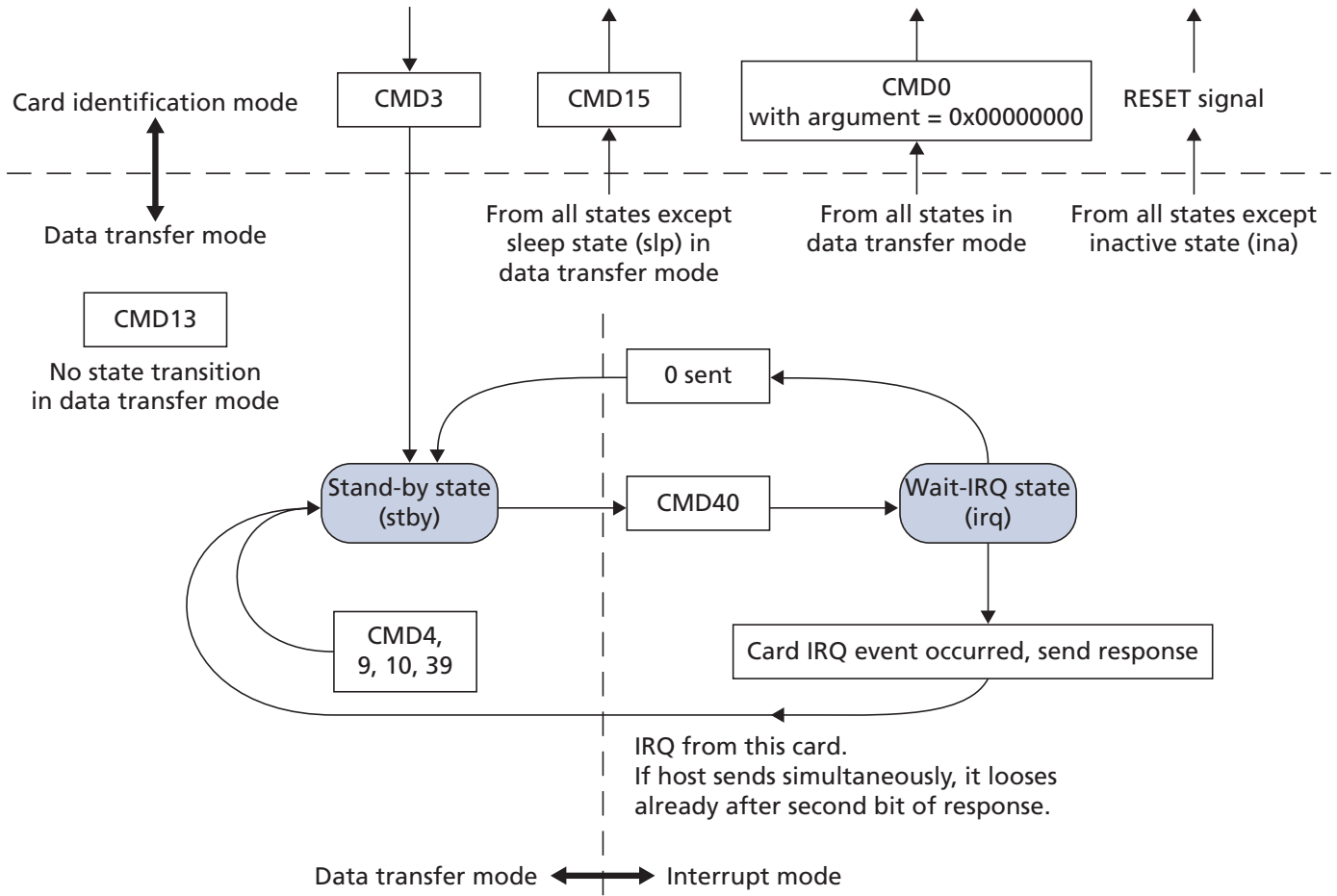


Note: 1. When the part is in idle or pre-idle state, any invalid command may show ILLEGAL_COMMAND in the status register on the first command with R1 response. For example, CMD55 may cause a CMD3 response to show an illegal command status during the initialization sequence.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP State Diagrams

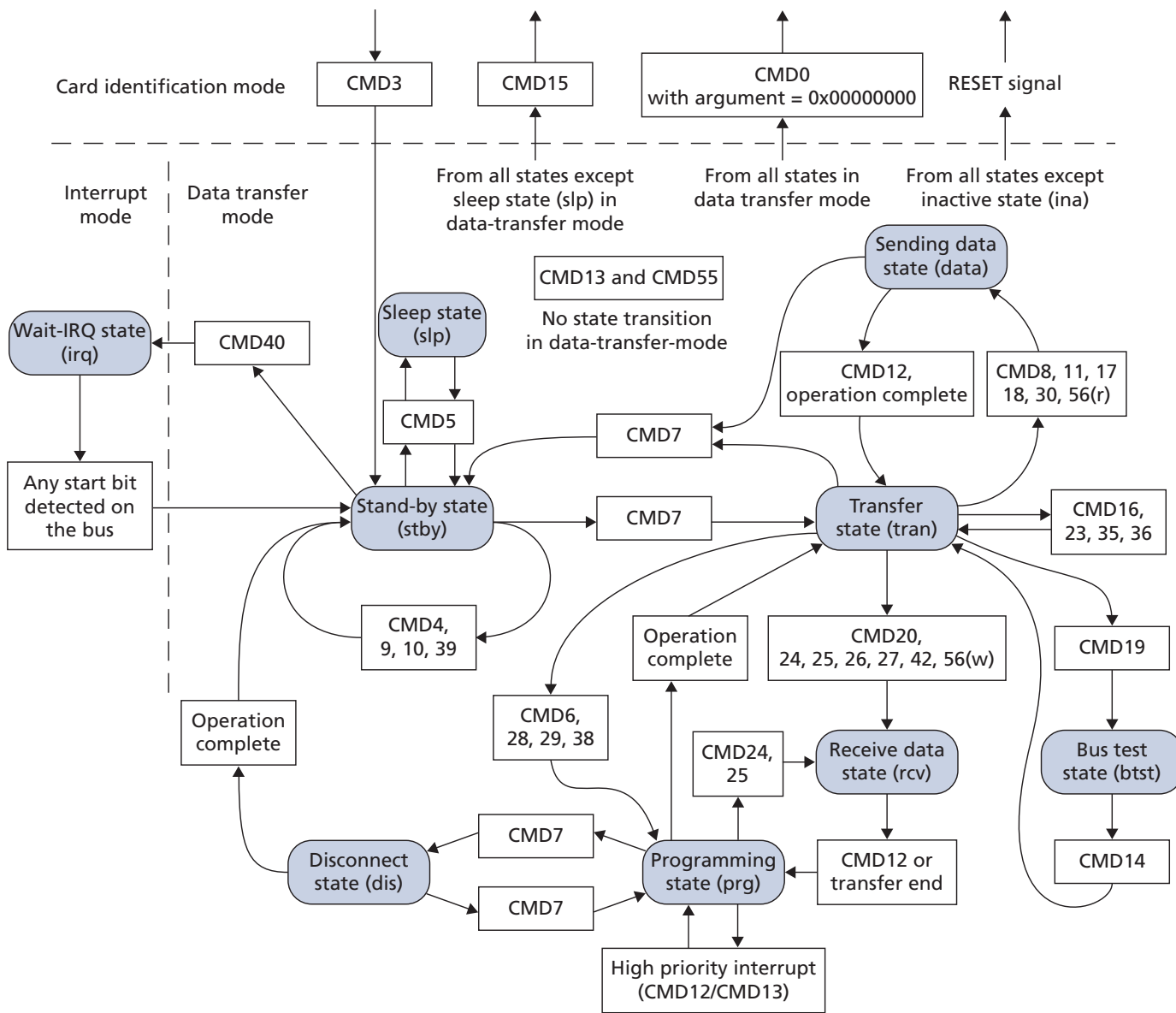
Figure 9: Interrupt Mode





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP State Diagrams

Figure 10: Data Transfer Mode





Electrical Specifications

Table 10: Absolute Maximum Ratings

Parameters/Conditions	Symbol	Min	Max	Unit
V_{CCM} and V_{CCQM} supply voltage relative to V_{SS}	V_{CCM}, V_{CCQM}	-0.5	3.6	V
Voltage on any pin relative to V_{SS}	V_{IN}	-0.5	1.6 or ($V_{DDQ} + 0.3$), whichever is less	V
Storage temperature range	-	-40	+85	°C

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11: Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CCM}	2.70	-	3.60	V
I/O supply voltage	V_{CCQM}	1.65	-	1.95	V
		2.70	-	3.60	
Operating temperature range	-	-30	-	+85	°C



**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
DC Electrical Specifications – Device Power**

DC Electrical Specifications – Device Power

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device and its interface voltage; V_{CCQ} is used for the controller and the e-MMC interface voltage.

Figure 11: Device Power Diagram

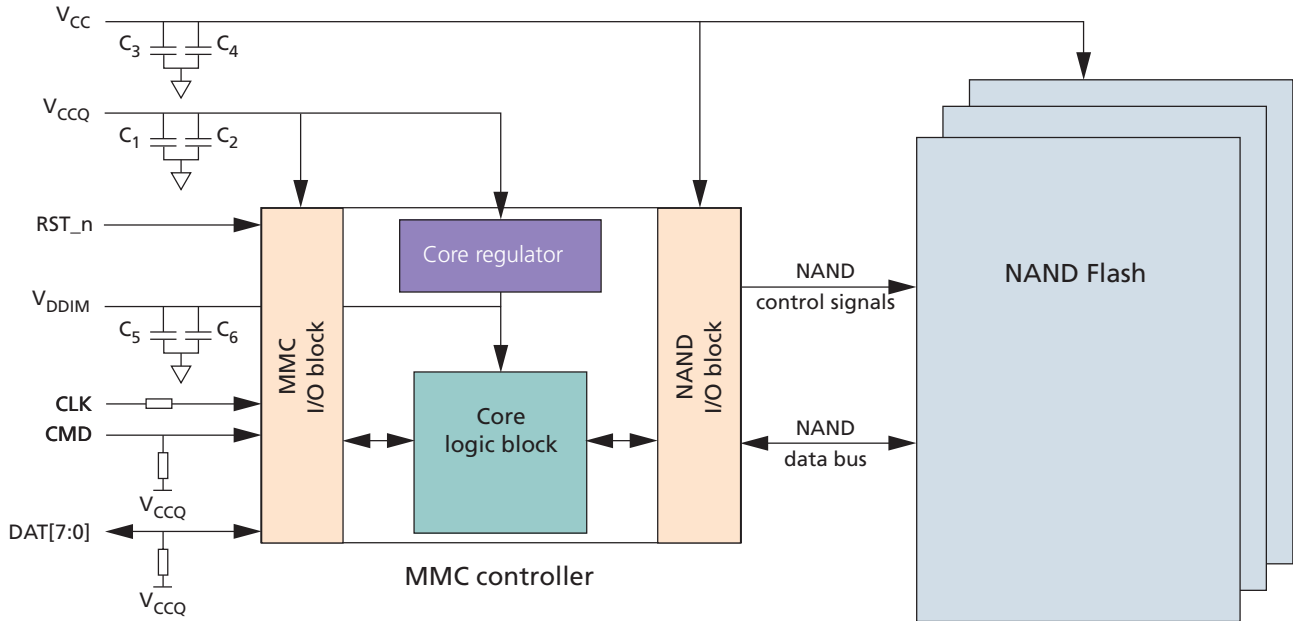


Table 12: Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Voltage input	V_{IN}	-0.6	4.6	V
V_{CC} supply	V_{CC}	-0.6	4.6	V
V_{CCQ} supply	V_{CCQ}	-0.6	4.6	V

Table 13: Power Domains

Parameter	Symbol	Comments
Host interface	V_{CCQM}	High voltage range = 3.3V (nominal) Low voltage range = 1.8V (nominal)
Memory	V_{CCM}	High voltage range = 3.3V (nominal)
Internal	V_{DDIM}	The internal regulator connection to an external decoupling capacitor



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP DC Electrical Specifications – Device Power

Table 14: Capacitor and Resistance Specifications

Parameter	Symbol	Min	Max	Typ	Units	Notes
Pull-up resistance: CMD	R_CMD	4.7	50	10	k Ω	1
Pull-up resistance: DAT[7:0]	R_DAT	10	50	50	k Ω	1
Pull-up resistance: RST_n	R_RST_n	4.7	50	50	k Ω	2
CLK/CMD/DAT[7:0] impedance		45	55	50	Ω	3
Serial resistance on CLK	SR_CLK	0	47	22	Ω	
V _{CCQ} capacitor	C1	2.2	4.7	2.2	μ F	4
	C2	0.1	0.22	0.1		
V _{CC} capacitor (\leq 8GB)	C3	2.2	4.7	2.2	μ F	5
	C4	0.1	0.22	0.1		
V _{CC} capacitor ($>$ 8GB)	C3	2.2	4.7	4.7	μ F	5
	C4	0.1	0.22	0.22		
V _{DDIM} capacitor (C _{reg})	C5	1	4.7	1	μ F	6
	C6	0.1	0.1	0.1		

- Notes:
- Used to prevent bus floating.
 - If host does not use H/W RESET (RST_n), pull-up resistance is not needed on RST_n line (Extended_CSD[162] = 00h).
 - Impedance match.
 - The coupling capacitor should be connected with V_{CCQ} and V_{SSQ} as closely as possible.
 - The coupling capacitor should be connected with V_{CC} and V_{SS} as closely as possible.
 - The coupling capacitor should be connected with V_{DDIM} and V_{SS} as closely as possible.



4Gb: x16, x32 Mobile LPDDR2 SDRAM

Hereafter, for general 4Gb Mobile LPDDR2 SDRAM, only one die specification is described. Electrical specification, including die internal organization and operating temperature range, are defined in Features in cover page. I_{DD} values can be calculated according to the die configuration in the package.

Features

- Ultra-low-voltage core and I/O power supplies
 - $V_{DD1}/V_{DD2}/V_{DDQ} = 1.8V/1.2V/1.2V$
- Organization
 - 32M words x 16 bits x 8 banks
 - 16M words x 32 bits x 8 banks
- JEDEC LPDDR2-compliant
- 4KB page size
 - Row address: R0 to R13
 - Column address: C0 to C10 (x16 bits), C0 to C9 (x32 bits)
- Data rate: 1066 Mb/s MAX (RL = 8)
- Auto precharge option for each burst access
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Double data rate, command/address inputs; commands entered on each CK edge
- Bidirectional/differential data strobe per byte of data (DQS)
- Differential clock inputs (CK_t and CK_c)
- Data mask (DM) for write data
- Command/Address (CA) training for CA input timing adjustment
- Write leveling for clock to DQ, DQS, and DM timing adjustment
- Interface: HSUL₁₂
- Read latency (RL): 3, 4, 5, 6, 7, 8
- Burst length (BL): 4, 8, 16
- Burst type (BT)
 - Sequential (4, 8, 16)
 - Interleave (4, 8)
- Per-bank refresh for concurrent operation
- Auto temperature compensated self refresh (ATCSR)
- Auto refresh and self refresh
- Refresh cycles: 8192 cycles/32ms
 - Average refresh period: 3.9 μ s
- Partial-array self refresh (PASR)
 - Bank masking
 - Segment masking
- Deep power-down (DPD)
- Programmable drive strength (DS)
- Operating temperature range
 - $T_C = -30^{\circ}C$ to $+85^{\circ}C$



LPDDR2 Array Configuration

The 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296-bits. The device is internally configured as an eight-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.



I_{DD} Specifications

Table 15: I_{DD} Specifications – Single Die (T_C = -30°C to +85°C)
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I _{DD01}	V _{DD1}	8.0	8.0	mA	Operating one bank active-precharge current t _{CK} = t _{CK} (avg) MIN; t _{RC} = t _{RC} (MIN); CKE is HIGH; CS _n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD02}	V _{DD2}	50	45		
I _{DD0,in}	V _{DDQ}	0.6	0.6		
I _{DD2P1}	V _{DD1}	0.4	0.4	mA	Idle power-down standby current t _{CK} = t _{CK} (avg) MIN; CKE is LOW; CS _n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD2P2}	V _{DD2}	0.9	0.9		
I _{DD2P,in}	V _{DDQ}	0.1	0.1		
I _{DD2PS1}	V _{DD1}	0.4	0.4	mA	Idle power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is LOW; CS _n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD2PS2}	V _{DD2}	0.9	0.9		
I _{DD2PS,in}	V _{DDQ}	0.1	0.1		
I _{DD2N1}	V _{DD1}	0.6	0.6	mA	Idle non power-down standby current t _{CK} = t _{CK} (avg) MIN; CKE is HIGH; CS _n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD2N2}	V _{DD2}	13	11		
I _{DD2N,in}	V _{DDQ}	0.6	0.6		
I _{DD2NS1}	V _{DD1}	0.6	0.6	mA	Idle non power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS _n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD2NS2}	V _{DD2}	6.0	6.0		
I _{DD2NS,in}	V _{DDQ}	0.6	0.6		
I _{DD3P1}	V _{DD1}	0.8	0.8	mA	Active power-down standby current t _{CK} = t _{CK} (avg) MIN; CKE is LOW; CS _n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD3P2}	V _{DD2}	5.0	5.0		
I _{DD3P,in}	V _{DDQ}	0.1	0.1		
I _{DD3PS1}	V _{DD1}	0.8	0.8	mA	Active power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is LOW; CS _n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD3PS2}	V _{DD2}	5.0	5.0		
I _{DD3PS,in}	V _{DDQ}	0.1	0.1		
I _{DD3N1}	V _{DD1}	1.2	1.2	mA	Active non power-down standby current t _{CK} = t _{CK} (avg) MIN; CKE is HIGH; CS _n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD3N2}	V _{DD2}	19	17		
I _{DD3N,in}	V _{DDQ}	0.6	0.6		



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP I_{DD} Specifications

Table 15: I_{DD} Specifications – Single Die (T_C = -30°C to +85°C) (Continued)
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$

Symbol	Supply	Speed		Unit	Parameter/Condition
		1066	800		
I _{DD3NS1}	V _{DD1}	1.2	1.2	mA	Active non power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS _n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD3NS2}	V _{DD2}	12	12		
I _{DD3NS,in}	V _{DDQ}	0.6	0.6		
I _{DD4R1}	V _{DD1}	2.0	2.0	mA	Operating burst read current t _{CK} = t _{CK} (avg) MIN; CS _n is HIGH between valid commands; One bank active; BL = 4; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for x16 bits
I _{DD4R2}	V _{DD2}	160 (130)	130 (105)		
I _{DD4W1}	V _{DD1}	2.0	2.0	mA	Operating burst write current t _{CK} = t _{CK} (avg) MIN; CS _n is HIGH between valid commands; One bank active; BL = 4; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for x16 bits
I _{DD4W2}	V _{DD2}	150 (110)	120 (90)		
I _{DD4W,in}	V _{DDQ}	1.0	1.0		
I _{DD51}	V _{DD1}	20	20	mA	All bank auto-refresh burst current t _{CK} = t _{CK} (avg) MIN; CKE is HIGH between valid commands; t _{RC} = t _{RFCab} (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD52}	V _{DD2}	120	120		
I _{DD5,in}	V _{DDQ}	0.6	0.6		
I _{DD5AB1}	V _{DD1}	2.0	2.0	mA	All bank auto-refresh average current t _{CK} = t _{CK} (avg) MIN; CKE is HIGH between valid commands; t _{RC} = t _{REFI} ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD5AB2}	V _{DD2}	16	15		
I _{DD5AB,in}	V _{DDQ}	0.6	0.6		
I _{DD5PB1}	V _{DD1}	2.0	2.0	mA	Per bank auto-refresh average current t _{CK} = t _{CK} (avg) MIN; CKE is HIGH between valid commands; t _{RC} = t _{REFIpb} ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD5PB2}	V _{DD2}	16	15		
I _{DD5PB,in}	V _{DDQ}	0.6	0.6		
I _{DD81}	V _{DD1}	16	16	μA	Deep power-down current CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD82}	V _{DD2}	6.0	6.0		
I _{DD8,in}	V _{DDQ}	12	12		

- Notes: 1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP I_{DD} Specifications

Table 16: I_{DD6} Partial-Array Self Refresh Current at 45°C – Single Die
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$

PASR	Supply	Value	Unit	Parameter/Conditions
Full array	V _{DD1}	200	μA	Self-refresh current CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V _{DD2}	800		
	V _{DDQ}	10		
1/2 array	V _{DD1}	160		
	V _{DD2}	500		
	V _{DDQ}	10		
1/4 array	V _{DD1}	130		
	V _{DD2}	300		
	V _{DDQ}	10		
1/8 array	V _{DD1}	120		
	V _{DD2}	200		
	V _{DDQ}	10		

Note: 1. I_{DD6} 45°C is the typical of the distribution of the arithmetic mean.

Table 17: I_{DD6} Partial-Array Self Refresh Current at 85°C – Single Die
 $V_{DD2}, V_{DDQ} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$

PASR	Supply	Value	Unit	Parameter/Conditions
Full array	V _{DD1}	900	μA	Self-refresh current CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V _{DD2}	3200		
	V _{DDQ}	12		
1/2 array	V _{DD1}	650		
	V _{DD2}	2200		
	V _{DDQ}	12		
1/4 array	V _{DD1}	550		
	V _{DD2}	1700		
	V _{DDQ}	12		
1/8 array	V _{DD1}	500		
	V _{DD2}	1400		
	V _{DDQ}	12		

Note: 1. I_{DD6} 85°C is the maximum of the distribution of the arithmetic mean.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Functional Description

Functional Description

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4- or 8-bank memory device. The device uses a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

The LPDDR2-S4 device uses a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a $4n$ prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

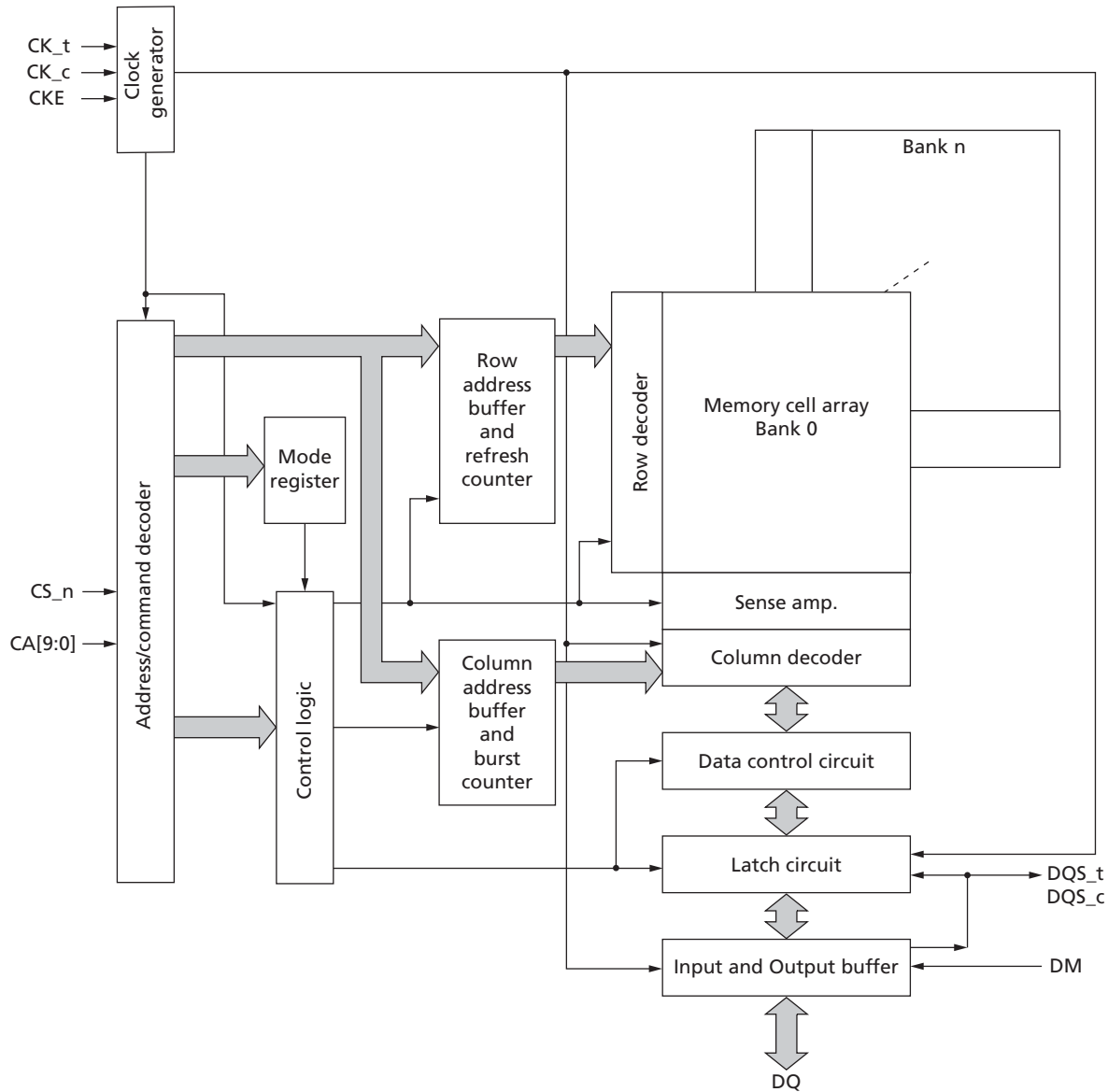
Read and write access is burst oriented; access starts at a selected location and continues for a programmed number of locations in a programmed sequence.

Access begins with the registration of an ACTIVATE command followed by a READ or WRITE command. Registered address and BA bits that coincide with the ACTIVATE command are used to select the row and bank to be accessed. Registered address bits that coincide with the READ or WRITE command are used to select the bank and the starting column location for the burst access.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Simplified State Diagram

Figure 12: Functional Block Diagram



Note: 1. 512Mb is a 4-bank only.

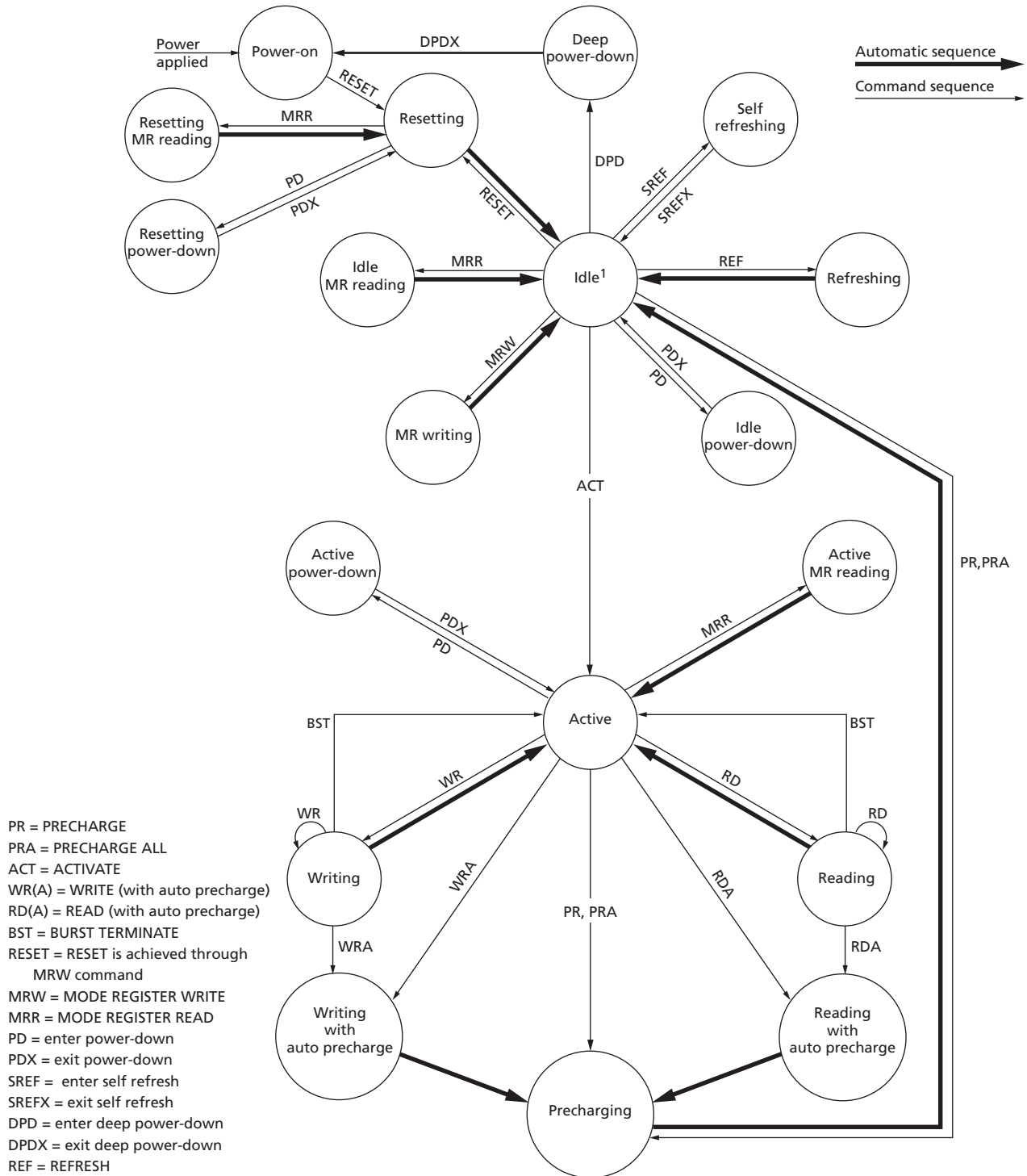
Simplified State Diagram

The state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification. The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Simplified State Diagram

Figure 13: Simplified State Diagram



Note: 1. All banks are precharged in the idle state.



Power-Up and Initialization

The device must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory (see the Voltage Ramp and Initialization Sequence figure). Power-up and initialization by means other than those specified will result in undefined operation.

1. Voltage Ramp Beginning

While applying power (after T_a), CKE must be held LOW ($\leq 0.2 \times V_{DD2}$), and all other inputs must be between V_{ILmin} and V_{IHmax} . The device outputs remain at High-Z while CKE is held LOW.

On or before the completion of the voltage ramp (T_b), CKE must be held LOW. DQ, DM, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latchup.

The following conditions apply for voltage ramp:

- T_a is the point when any power supply first reaches 300mV.
- Noted conditions apply between T_a and power-down (controlled or uncontrolled).
- T_b is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration t_{INIT0} ($T_b - T_a$) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any of V_{SS} , and V_{SSQ} pins must not exceed 100mV.

2. Voltage Ramp Completion

After T_a is reached:

- V_{DD1} must be greater than $V_{DD2} - 200mV$
- V_{DD1} and V_{DD2} must be greater than $V_{DDQ} - 200mV$
- V_{REF} must always be less than all other supply voltages

Beginning at T_b , CKE must remain LOW for at least $t_{INIT1} = 100ns$, after which CKE can be asserted HIGH. The clock must be stable at least $t_{INIT2} = 5 \times t_{CK}$ prior to the first CKE LOW-to-HIGH transition (T_c). CKE, CS_n, and CA inputs must observe setup and hold requirements (t_{IS} , t_{IH}) with respect to the first rising clock edge (and to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for t_{CKb} (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, t_{DQSCK}) could have relaxed timings (such as t_{DQSCKb}) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least $t_{INIT3} = 200\mu s$ (T_d).



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Power-Up and Initialization

3. RESET Command

After t_{INIT3} is satisfied, the MRW RESET command must be issued (T_d). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least t_{INIT4} while keeping CKE asserted and issuing NOP commands.

4. MRRs and Device Auto Initialization (DAI) Polling

After t_{INIT4} is satisfied (T_e), only MRR commands and power-down entry/exit commands are supported. After T_e , CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down).

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of t_{INIT5} or until the DAI bit is set before proceeding.

Because the memory output buffers are not properly configured by T_e , some AC parameters must use relaxed timing specifications before the system is appropriately configured.

After the memory device sets the DAI bit (MR0, DAI) to zero, indicating DAI complete, the device is in the idle state (T_f). DAI status can be determined by issuing the MRR command to MR0.

The device sets the DAI bit no later than t_{INIT5} after the RESET command. The controller must wait at least t_{INIT5} or until the DAI bit is set before proceeding.

5. ZQ Calibration

After t_{INIT5} (T_f), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10).

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands. The device is ready for normal operation after t_{ZQINIT} .

6. Normal Operation

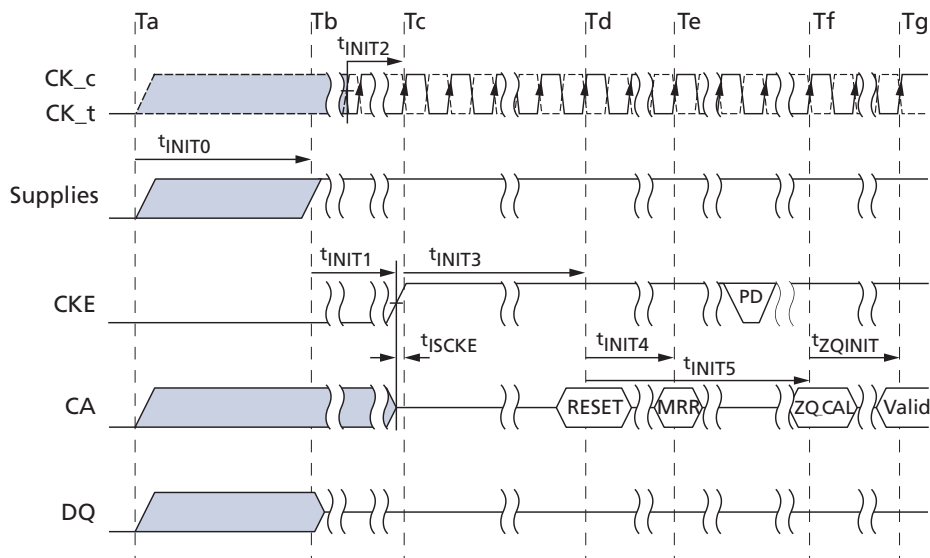
After (T_g), the MRW command must be used to properly configure the memory, including, for example, output buffer drive strength, latencies, and so on. Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After T_g , the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Stop Events.



8Gb: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Power-Off Sequence

Figure 14: Voltage Ramp and Initialization Sequence



Note: 1. High-Z on the CA bus indicates valid NOP.

Table 18: Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	–	20	ms	Maximum voltage ramp time
t_{INIT1}	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
t_{INIT2}	5	–	t_{CK}	Minimum stable clock before first CKE HIGH
t_{INIT3}	200	–	μs	Minimum idle time after first CKE assertion
t_{INIT4}	1	–	μs	Minimum idle time after RESET command
t_{INIT5}	–	10	μs	Maximum duration of device auto initialization
t_{ZQINIT}	1	–	μs	ZQ initial calibration (S4 devices only)
t_{CKb}	18	100	ns	Clock cycle time during boot

Note: 1. The t_{INIT0} maximum specification is not a tested limit and should be used as a general guideline. For voltage ramp times exceeding t_{INIT0} MAX, contact the factory.

Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Power-Off Sequence

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DD2}$); all other inputs must be between V_{ILmin} and V_{IHmax} . The device outputs remain at High-Z while CKE is held LOW.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

DQ, DM, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between V_{SS} and V_{DD2} during the power-off sequence to avoid latchup.

Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Required Power Supply Conditions Between Tx and Tz:

- V_{DD1} must be greater than $V_{DD2} - 200\text{mV}$
- V_{DD1} must be greater than $V_{DDQ} - 200\text{mV}$
- V_{REF} must always be less than all other supply voltages

The voltage difference between V_{SS} and V_{SSQ} must not exceed 100mV.

For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz, the point at which all power supplies first reach 300mV, the device must power off. The time between Tx and Tz must not exceed t_{POFF} . During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than $0.5\text{ V}/\mu\text{s}$ between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 19: Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	t_{POFF}	–	2	sec

Mode Register Definition

The LPDDR2 device contains a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignments and Definitions

The MRR command is used to read from a register. The MRW command is used to write to a register. An “R” in the access column of the mode register assignment table indicates read-only; a “W” indicates write-only; “R/W” indicates read or write capable or enabled.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 20: Mode Register Assignments

Notes 1–5 apply to all parameters and conditions

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	RFU			RZQI	RFU	DI	DAI		go to MR0
1	01h	Device feature 1	W	nWR (for AP)			WC	BT	BL			go to MR1
2	02h	Device feature 2	W	RFU			RL and WL				go to MR2	
3	03h	I/O config-1	W	RFU			DS				go to MR3	
4	04h	SDRAM refresh rate	R	TUF	RFU			Refresh rate			go to MR4	
5	05h	Basic config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06h	Basic config-2	R	Revision ID1								go to MR6
7	07h	Basic config-3	R	Revision ID2								go to MR7
8	08h	Basic config-4	R	I/O width	Density			Type			go to MR8	
9	09h	Test mode	W	Vendor-specific test mode								go to MR9
10	0Ah	I/O calibration	W	Calibration code								go to MR10
11–15	0Bh ~ 0Fh	Reserved	–	RFU								go to MR11
16	10h	PASR_Bank	W	Bank mask								go to MR16
17	11h	PASR_Seg	W	Segment mask								go to MR17
18–31	12h–1Fh	Reserved	–	RFU								go to MR18
32	20h	DQ calibration pattern A	R	See Data Calibration Pattern Description table								go to MR32
33–39	21h–27h	Do not use										go to MR33
40	28h	DQ calibration pattern B	R	See Data Calibration Pattern Description table								go to MR40
41–47	29h–2Fh	Do not use										go to MR41
48–62	30h–3Eh	Reserved	–	RFU								go to MR48
63	3Fh	RESET	W	X								go to MR63
64–126	40h–7Eh	Reserved	–	RFU								go to MR64
127	7Fh	Do not use										go to MR127
128–190	80h–BEh	Reserved for vendor use		RVU								go to MR128
191	BFh	Do not use										go to MR191
192–254	C0h–FEh	Reserved for vendor use		RVU								go to MR192
255	FFh	Do not use										go to MR255

- Notes:
1. RFU bits must be set to 0 during MRW.
 2. RFU bits must be read as 0 during MRR.
 3. For READs to a write-only or RFU register, DQS will be toggled and undefined data is returned.
 4. RFU mode registers must not be written.
 5. WRITEs to read-only registers must have no impact on the functionality of the device.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 21: MR0 Device Information (MA[7:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	RFU		RZQI		RFU	DI	DAI

Table 22: MR0 Op-Code Bit Definitions

Notes 1–4 apply to all parameters and conditions

Register Information	Tag	Type	OP	Definition
Device auto initialization status	DAI	Read-only	OP0	0b: DAI complete
				1b: DAI in progress
Device information	DI	Read-only	OP1	0b:DDR2 Mobile RAM (S4 SDRAM)
Built-in self test for RZQ information	RZQI	Read-only	OP[4:3]	01b: ZQ pin might be connected to V _{DD2} or left floating
				10b: ZQ pin might be shorted to ground
				11b: ZQ pin self test complete; no error condition detected(ZQ-pin may not connect to VDD or float nor short to GND)

- Notes:
1. If RZQI is supported, it will be set upon completion of the MRW ZQ initialization calibration.
 2. If ZQ is connected to V_{DD2} to set default calibration, OP[4:3] must be set to 01. If ZQ is not connected to V_{DD2}, either OP[4:3] = 01 or OP[4:3] = 10 could indicate a ZQ-pin assembly error. It is recommended that the assembly error be corrected.
 3. In the case of a possible assembly error (either OP[4:3] = 01 or OP[4:3] = 10, as defined above), the device will default to factory trim settings for R_{ON}(output impedance) and will ignore ZQ calibration commands. In either case, the system might not function as intended.
 4. If a ZQ self test returns a value of 11b, this indicates that the device has detected a resistor connection to the ZQ pin. Note that this result cannot be used to validate the ZQ resistor value, nor does it indicate that the ZQ resistor tolerance meets the specified limits (240 ohms ±1%).

Table 23: MR1 Device Feature 1 (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	nWR (for AP)		WC	BT		BL	

Table 24: MR1 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
BL = burst length	Write-only	OP[2:0]	010b: BL4 (default)	1
			011b: BL8	
			100b: BL16	
			All others: Reserved	



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 24: MR1 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition	Notes
BT = burst type	Write-only	OP3	0b: Sequential (default)	
			1b: Interleaved	
WC = wrap control	Write-only	OP4	0b: Wrap (default)	
			1b: No wrap (allowed for BL4 only)	
nWR = number of ^t WR clock cycles	Write-only	OP[7:5]	001b: nWR = 3 (default)	2
			010b: nWR = 4	
			011b: nWR = 5	
			100b: nWR = 6	
			101b: nWR = 7	
			110b: nWR = 8	
			All others: Reserved	

- Notes:
1. BL16, interleaved is not an official combination to be supported.
 2. The programmed value in nWR register is the number of clock cycles that determines when to start internal precharge operation for a WRITE burst with AP enabled. It is determined by RU (^tWR/^tCK).

Table 25: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC)

Notes 1–5 apply to all parameters and conditions

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence																
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
4	Any	X	X	0b	0b	Wrap	0	1	2	3													
		X	X	1b	0b		2	3	0	1													
	Any	X	X	X	0b	No wrap	y	y+1	y+2	y+3													
8	Seq	X	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7									
		X	0b	1b	0b		2	3	4	5	6	7	0	1									
		X	1b	0b	0b		4	5	6	7	0	1	2	3									
		X	1b	1b	0b		6	7	0	1	2	3	4	5									
	Int	X	0b	0b	0b		0	1	2	3	4	5	6	7									
		X	0b	1b	0b		2	3	0	1	6	7	4	5									
		X	1b	0b	0b		4	5	6	7	0	1	2	3									
		X	1b	1b	0b		6	7	4	5	2	3	0	1									
	Any	X	X	X	0b		No wrap	Illegal (not supported)															



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 25: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC) (Continued)

Notes 1–5 apply to all parameters and conditions

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
16	Seq	0b	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	Int	X	X	X	0b	Illegal (not supported)																
Any	X	X	X	0b	Illegal (not supported)																	
					No wrap																	

- Notes:
1. C0 input is not present on CA bus. It is implied zero.
 2. For BL = 4, the burst address represents C[1:0].
 3. For BL = 8, the burst address represents C[2:0].
 4. For BL = 16, the burst address represents C[3:0].
 5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable y can start at any address with C0 equal to 0, but must not start at any address shown in the following table.

Table 26: No-Wrap Restrictions

Width	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
Cannot cross full-page boundary				
x16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
x32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Cannot cross sub-page boundary				
x16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
x32	None	None	None	None

Note: 1. No-wrap BL = 4 data orders shown are prohibited.

Table 27: MR2 Device Feature 2 (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				RL and WL			



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 28: MR2 Op-Code Bit Definitions

Feature	Type	OP	Definition
RL and WL	Write-only	OP[3:0]	0001b: RL3/WL1 (default)
			0010b: RL4/WL2
			0011b: RL5/WL2
			0100b: RL6/WL3
			0101b: RL7/WL4
			0110b: RL8/WL4
			All others: Reserved

Table 29: MR3 I/O Configuration 1 (MA[7:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

Table 30: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition
DS	Write-only	OP[3:0]	0000b: Reserved
			0001b: 34.3 ohm typical
			0010b: 40 ohm typical (default)
			0011b: 48 ohm typical
			0100b: 60 ohm typical
			0101b: Reserved
			0110b: 80 ohm typical
			0111b: 120 ohm typical
			All others: Reserved

Table 31: MR4 Device Temperature (MA[7:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF							
	RFU			SDRAM refresh rate			



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 32: MR4 Op-Code Bit Definitions

Notes 1–8 apply to all parameters and conditions

Feature	Type	OP	Definition
SDRAM refresh rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded
			001b: $4 \times t_{REFI}$, $4 \times t_{REFIpb}$, $4 \times t_{REFW}$
			010b: $2 \times t_{REFI}$, $2 \times t_{REFIpb}$, $2 \times t_{REFW}$
			011b: $1 \times t_{REFI}$, $1 \times t_{REFIpb}$, $1 \times t_{REFW}$ ($\leq 85^{\circ}\text{C}$)
			100b: Reserved
			101b: $0.25 \times t_{REFI}$, $0.25 \times t_{REFIpb}$, $0.25 \times t_{REFW}$, do not derate SDRAM AC timing
			110b: $0.25 \times t_{REFI}$, $0.25 \times t_{REFIpb}$, $0.25 \times t_{REFW}$, derate SDRAM AC timing
			111b: SDRAM high temperature operating limit exceeded
Temperature update flag (TUF)	Read-only	OP7	0b: OP[2:0] value has not changed since last read of MR4
			1b: OP[2:0] value has changed since last read of MR4

- Notes:
1. A MODE REGISTER READ from MR4 will reset OP7 to 0.
 2. OP7 is reset to 0 at power-up.
 3. If OP2 = 1, the device temperature is greater than 85°C.
 4. OP7 is set to 1 if OP[2:0] has changed at any time since the last MR4 read.
 5. The device might not operate properly when OP[2:0] = 000b or 111b.
 6. For specified operating temperature range and maximum operating temperature, refer to the Operating Temperature Range table.
 7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: t_{RCD} , t_{RC} , t_{RAS} , t_{RP} , and t_{RRD} . The t_{DQSCK} parameter must be derated as specified in AC Timing. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
 8. The recommended frequency for reading MR4 is provided in Temperature Sensor.

Table 33: MR5 Basic Configuration 1 (MA[7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

Table 34: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	00000011b
			All others: Reserved



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 35: MR6 Basic Configuration 2 (MA[7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1 (Die Revision)							

Note: 1. MR6 is vendor-specific.

Table 36: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1 (Die Revision)	Read-only	OP[7:0]	0000 0000b: Version A 0000 0001b: Version B 0000 0010b: Version C 0000 0010b: Version D(512Mb only) 0000 0011b: Version D

Table 37: MR7 Basic Configuration 3 (MA[7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2 (RFU)							

Table 38: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2 (RFU)	Read-only	OP[7:0]	0000 0000b: Default Value

Note: 1. MR7 is vendor-specific.

Table 39: MR8 Basic Configuration 4 (MA[7:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 40: MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S4 SDRAM
			01b: S2 SDRAM
			10b: Reserved
			11b: Reserved



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 40: MR8 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition
Density	Read-only	OP[5:2]	0000b: 64Mb
			0001b: 128Mb
			0010b: 256Mb
			0011b: 512Mb
			0100b: 1Gb
			0101b: 2Gb
			0110b: 4Gb
			0111b: 8Gb
			1000b: 16Gb
			1001b: 32Gb
			All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x32
			01b: x16
			10b: x8
			11b: not used

Table 41: MR9 Test Mode (MA[7:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 42: MR10 Calibration (MA[7:0] = 0Ah)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4	Calibration code							

Table 43: MR10 Op-Code Bit Definitions

Notes 1–6 apply to all parameters and conditions

Feature	Type	OP	Definition
Calibration code	Write-only	OP[7:0]	0xFF: Calibration command after initialization
			0xAB: Long calibration
			0x56: Short calibration
			0xC3: ZQRESET
			All others: Reserved

- Notes:
1. Host processor must not write MR10 with reserved values.
 2. The device ignores calibration commands when a reserved value is written into MR10.
 3. See AC timing table for the calibration latency.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

4. If ZQ is connected to V_{SS} through R_{ZQ} , either the ZQ calibration function (see MODE REGISTER WRITE command) or default calibration (through the ZQRESET command) is supported. If ZQ is connected to V_{DD2} , the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
5. LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
6. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

Table 44: MR[11:15] Reserved (MA[7:0] = 0Bh-0Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

Table 45: MR16 PASR Bank Mask (MA[7:0] = 010h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank mask (4-bank or 8-bank)							

Table 46: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: refresh enable to the bank = unmasked (default)
			1b: refresh blocked = masked

Note: 1. For 4-bank devices, only OP[3:0] are used.

Table 47: MR16 Bank and OP corresponding table

Feature	Type	OP	4-Bank Mask		8-Bank Mask	
			Bank #	Bank Address	Bank #	Bank Address
Bank[7:0] mask	Write-only	0	Bank 0	000b	Bank 0	000b
		1	Bank 1	001b	Bank 1	001b
		2	Bank 2	010b	Bank 2	010b
		3	Bank 3	011b	Bank 3	011b
		4	-	-	Bank 4	100b
		5	-	-	Bank 5	101b
		6	-	-	Bank 6	110b
		7	-	-	Bank 7	111b

Note: 1. Each bank can be masked independently by setting each OP value.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Mode Register Definition

Table 48: MR17 PASR Segment Mask (MA[7:0] = 011h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment mask							

Note: 1. This table applies for 1Gb to 8Gb devices only.

Table 49: MR17 PASR Segment Mask Definitions (1Gb - 8Gb only)

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: refresh enable to the segment: = unmasked (default)
			1b: refresh blocked: = masked

Table 50: MR17 PASR Row Address Ranges in Masked Segments

Segment	OP	Segment Mask	1Gb	2Gb, 4Gb	8Gb
			R[12:10]	R[13:11]	R[14:12]
0	0	XXXXXXX1		000b	
1	1	XXXXXX1X		001b	
2	2	XXXXX1XX		010b	
3	3	XXXX1XXX		011b	
4	4	XXX1XXXX		100b	
5	5	XX1XXXXX		101b	
6	6	X1XXXXXX		110b	
7	7	1XXXXXXX		111b	

Note: 1. X is "Don't Care" for the designated segment.


Table 51: Reserved Mode Registers

Mode Register	MA	Address	Restriction	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR[18:19]	MA[7:0]	12h–13h	RFU	Reserved							
MR[20:31]		14h–1Fh	NVM ¹								
MR[33:39]		21h–27h	DNU ¹								
MR[41:47]		29h–2Fh									
MR[48:62]		30h–3Eh	RFU								
MR[64:126]		40h–7Eh	RFU								
MR127		7Fh	DNU								
MR[128:190]		80h–BEh	RVU ¹								
MR191		BFh	DNU								
MR[192:254]		C0h–FEh	RVU								
MR255		FFh	DNU								

Note: 1. NVM = nonvolatile memory use only; DNU = Do not use; RVU = Reserved for vendor use.

Table 52: MR32 DQ Calibration Pattern A (MA[7:0] = 20H)

MR32 Reads
Reads to MR32 return DQ Calibration Pattern A

Table 53: MR40 DQ Calibration Pattern B (MA[7:0] = 28H)

MR40 Reads
Reads to MR40 return DQ Calibration Pattern B

Table 54: MR63 RESET (MA[7:0] = 3Fh) – MRW Only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note: 1. For additional information on MRW RESET see MODE REGISTER WRITE Command.

ACTIVATE Command

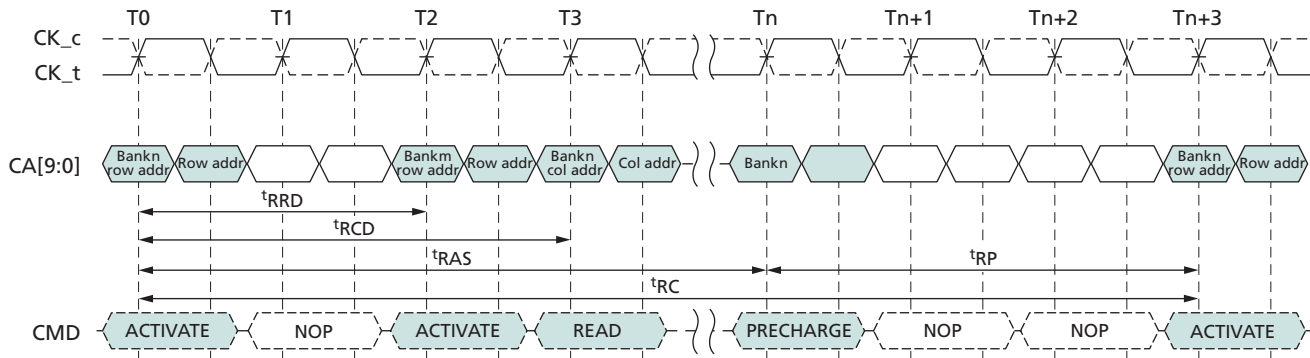
The ACTIVATE command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA[2:0] are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at ^tRCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP ACTIVATE Command

precharge times are defined as t_{RAS} and t_{RP} , respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between ACTIVATE commands to different banks is t_{RRD} .

Figure 15: ACTIVATE Command



- Notes:
1. $t_{RCD} = 3$, $t_{RP} = 3$, $t_{RRD} = 2$.
 2. A PRECHARGE ALL command uses t_{RPab} timing, and a single-bank PRECHARGE command uses t_{RPpb} timing. In this figure, t_{RP} is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

8-Bank Device Operation

Two rules regarding 8-bank device operation must be observed: One rule restricts the number of sequential ACTIVATE commands that can be issued; the second rule provides additional RAS precharge time for a PRECHARGE ALL command.

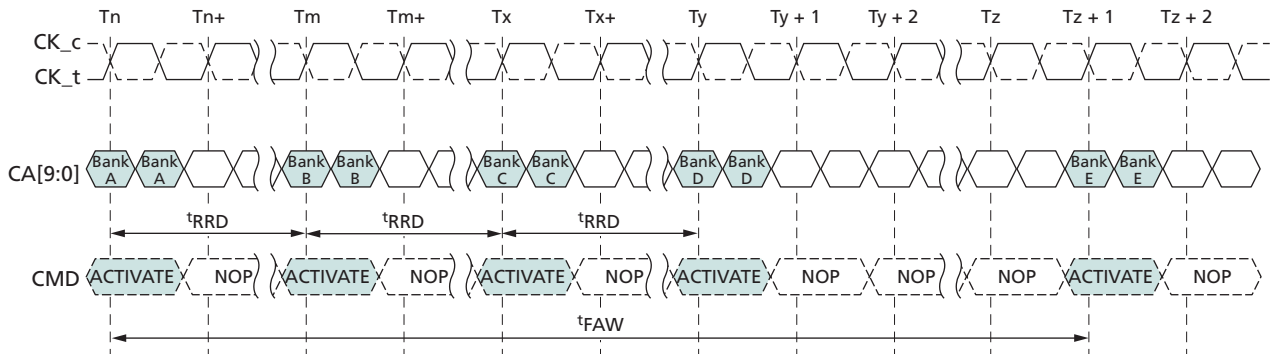
The 8-Bank Device Sequential Bank Activation Restriction: No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling t_{FAW} window. To convert to clocks, divide $t_{FAW}[ns]$ by $t_{CK}[ns]$, and round up to the next integer value. For example, if $RU(t_{FAW}/t_{CK})$ is 10 clocks, and an ACTIVATE command is issued in clock n , no more than three further ACTIVATE commands can be issued at or between clock $n + 1$ and $n + 9$. REFpb also counts as bank activation for purposes of t_{FAW} .

The 8-Bank Device PRECHARGE ALL Provision: t_{RP} for a PRECHARGE ALL command must equal t_{RPab} , which is greater than t_{RPpb} .



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Commands and Timing

Figure 16: t_{FAW} Timing (8-Bank Devices)

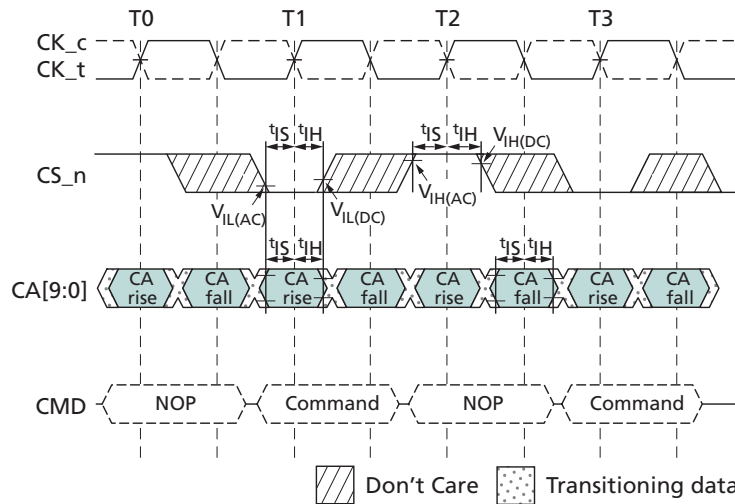


Note: 1. Exclusively for 8-bank devices.

Commands and Timing

The setup and hold timings shown in the figures below apply for all commands.

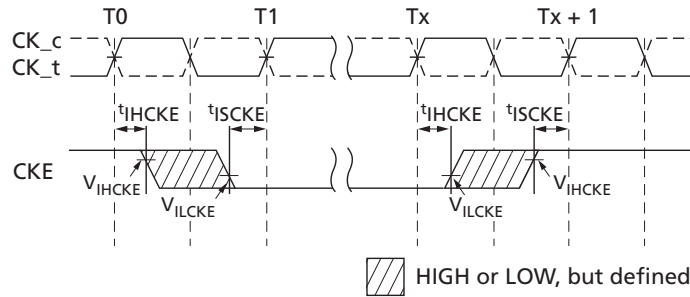
Figure 17: Command and Input Setup and Hold



Note: 1. Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see the Power-Down section.



Figure 18: CKE Input Setup and Hold



- Notes:
1. After CKE is registered LOW, the CKE signal level is maintained below V_{ILCKE} for t_{CKE} specification (LOW pulse width).
 2. After CKE is registered HIGH, the CKE signal level is maintained below V_{IHCKE} for t_{CKE} specification (HIGH pulse width).

Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles.

A new burst access must not interrupt the previous 4-bit burst operation when BL = 4. When BL = 8 or BL = 16, a READ can be interrupted by a READ and a WRITE can be interrupted by a WRITE, provided that the interrupt occurs on a 4-bit boundary and that t_{CCD} is met.

Burst READ Command

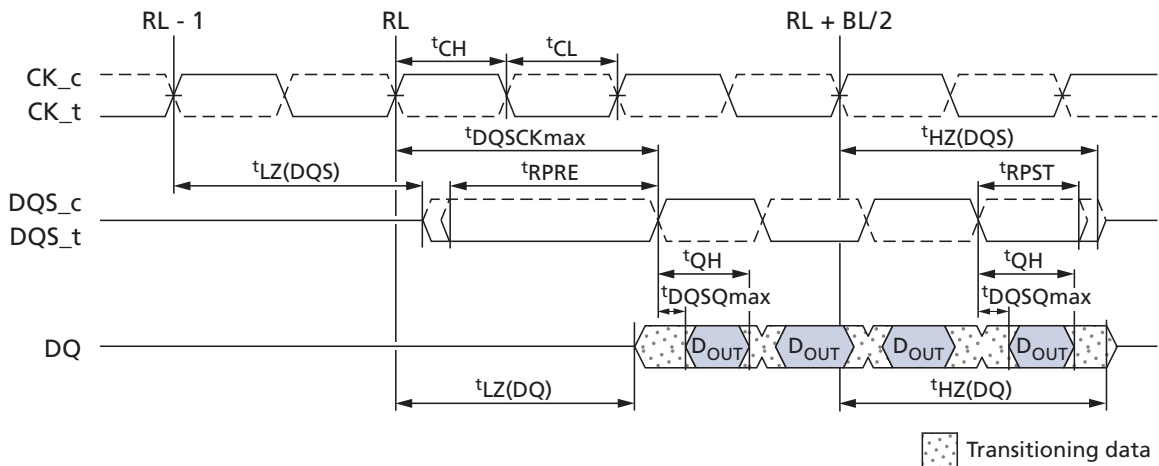
The burst READ command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid data is available $RL \times t_{CK} + t_{DQSCK} + t_{DQSQ}$ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW t_{RPRE} before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers.

Pin input timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.



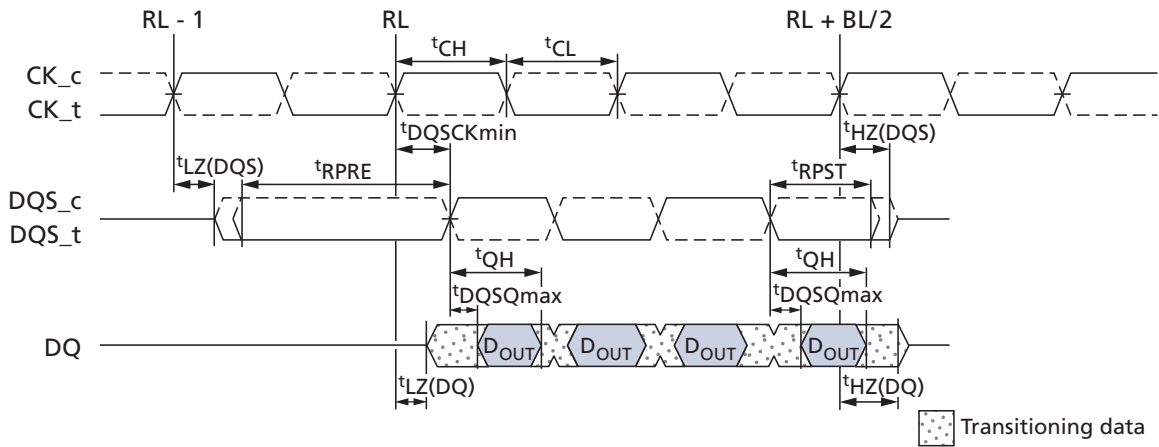
8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
Burst READ Command

Figure 19: READ Output Timing – $t_{DQSCK} (MAX)$



- Notes: 1. t_{DQSCK} can span multiple clock periods.
2. An effective burst length of 4 is shown.

Figure 20: READ Output Timing – $t_{DQSCK} (MIN)$



- Note: 1. An effective burst length of 4 is shown.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
Burst READ Command

Figure 21: Burst READ – RL = 5, BL = 4, $t_{DQSCK} > t_{CK}$

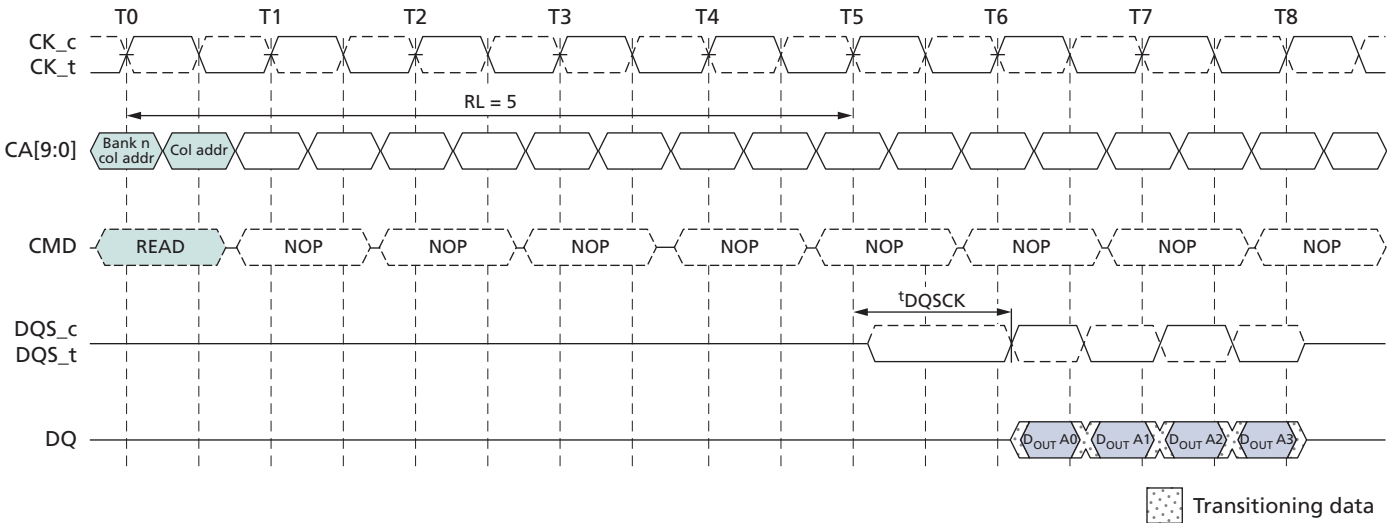
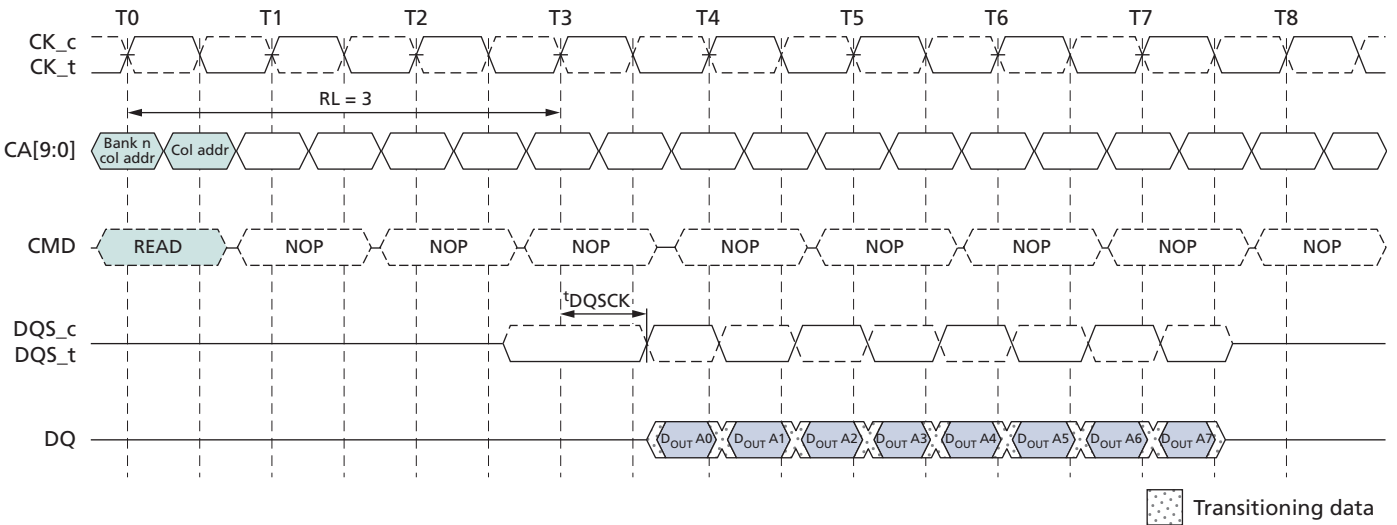


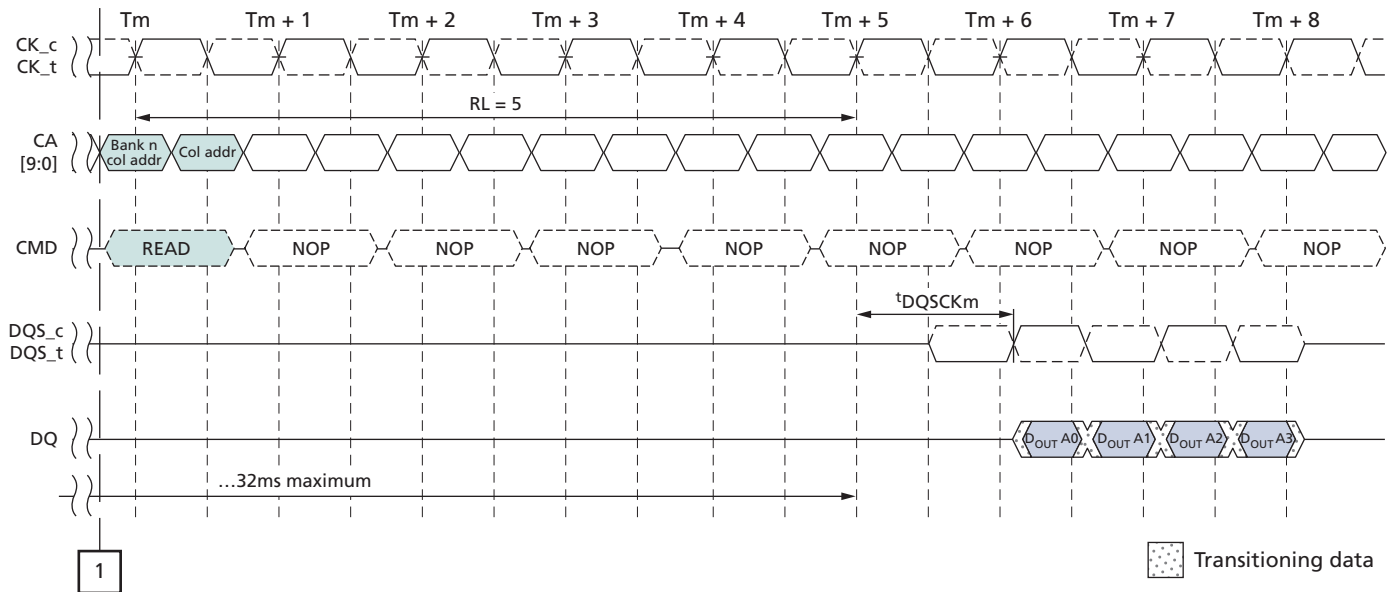
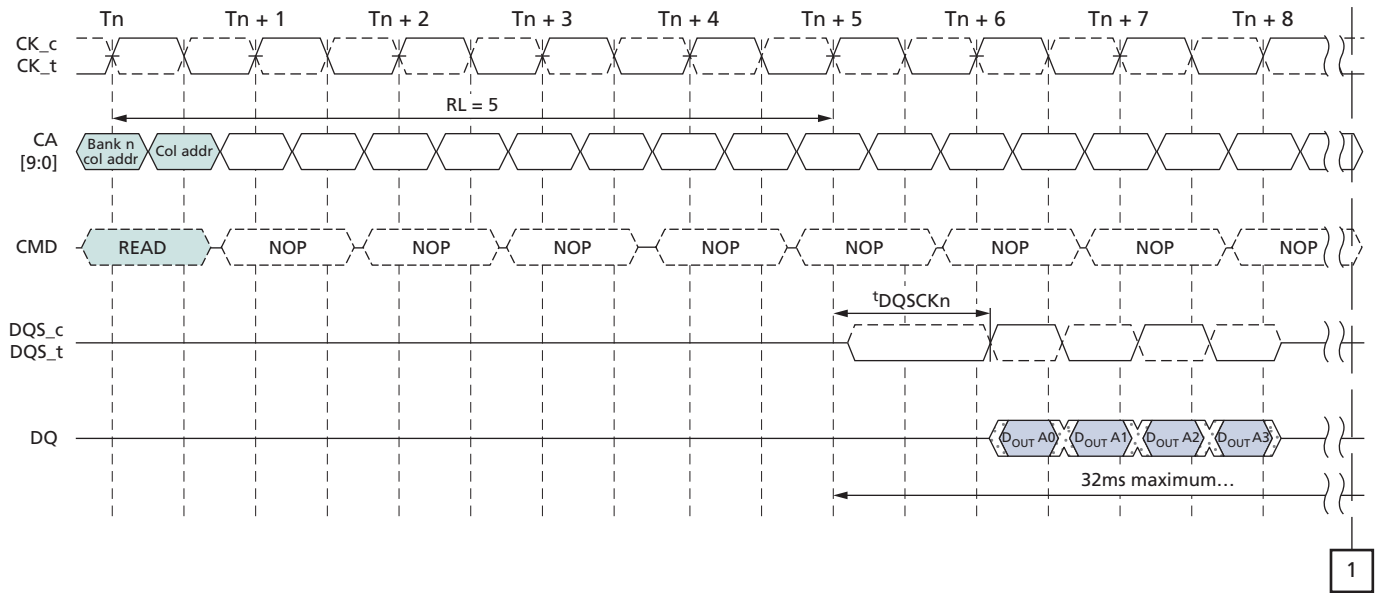
Figure 22: Burst READ – RL = 3, BL = 8, $t_{DQSCK} < t_{CK}$





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Burst READ Command

Figure 23: t_{DQSKDL} Timing

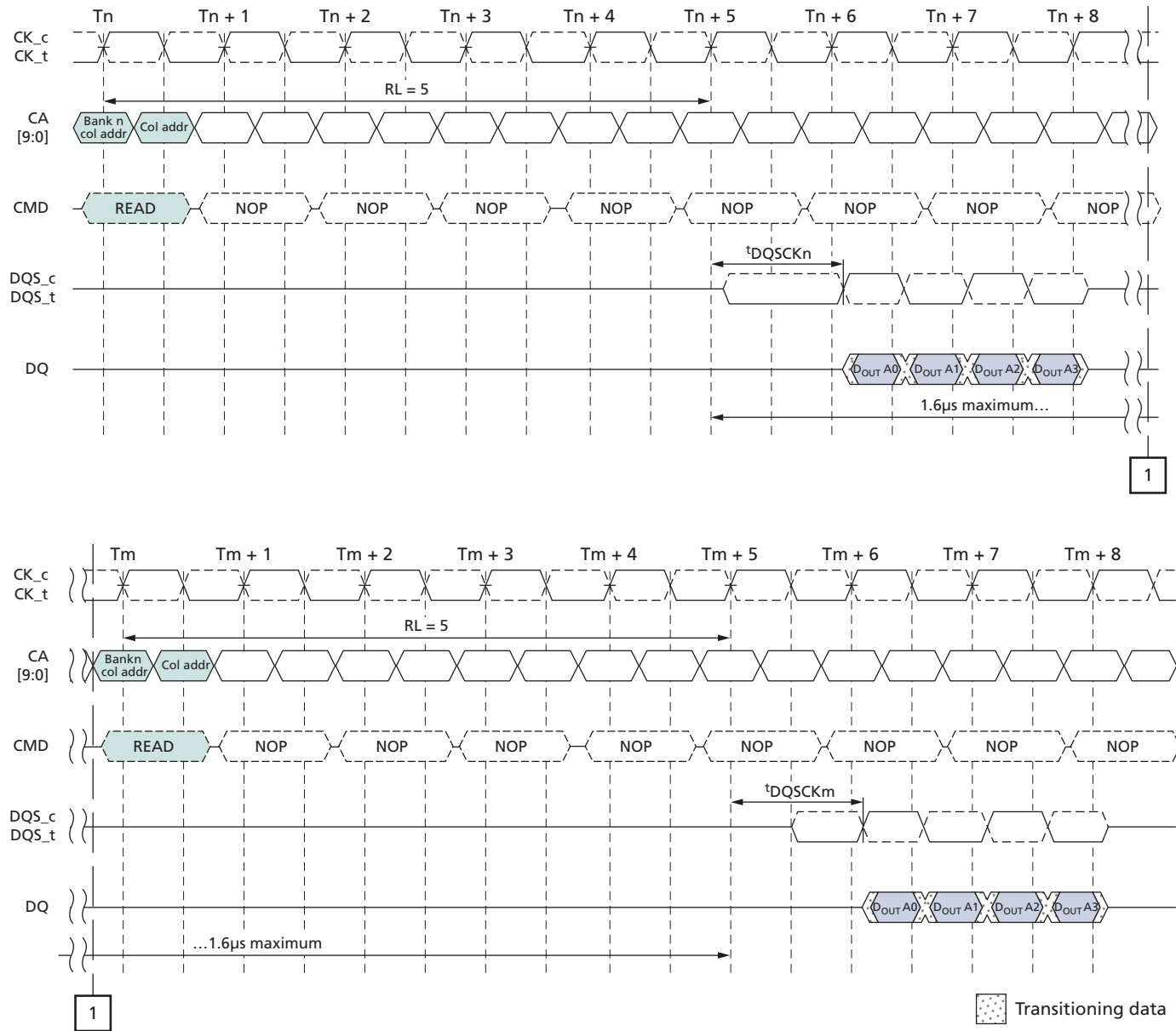


- Notes:
1. $t_{DQSKDL} = (t_{DQSKn} - t_{DQSKm})$.
 2. $t_{DQSKDL} (MAX)$ is defined as the maximum of ABS ($t_{DQSKn} - t_{DQSKm}$) for any (t_{DQSKn}, t_{DQSKm}) pair within any 32ms rolling window.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Burst READ Command

Figure 24: t_{DQSKDM} Timing

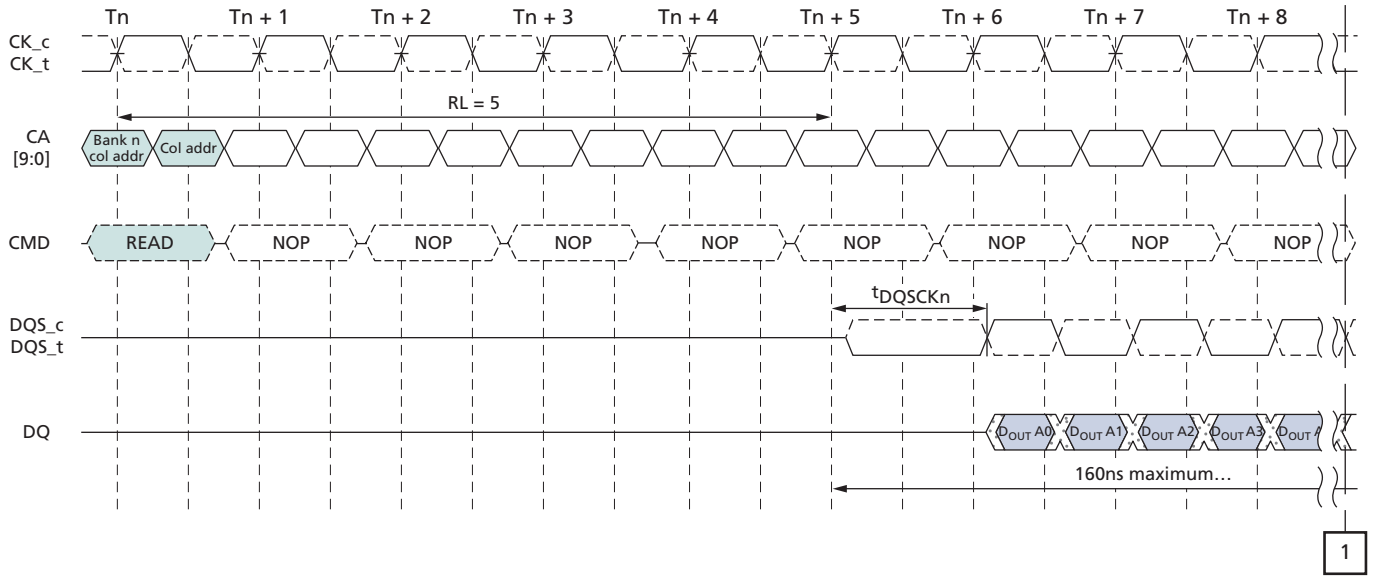


- Notes:
1. $t_{DQSKDM} = (t_{DQSKn} - t_{DQSKm})$.
 2. $t_{DQSKDM} (MAX)$ is defined as the maximum of ABS ($t_{DQSKn} - t_{DQSKm}$) for any (t_{DQSKn}, t_{DQSKm}) pair within any $1.6\mu s$ rolling window.

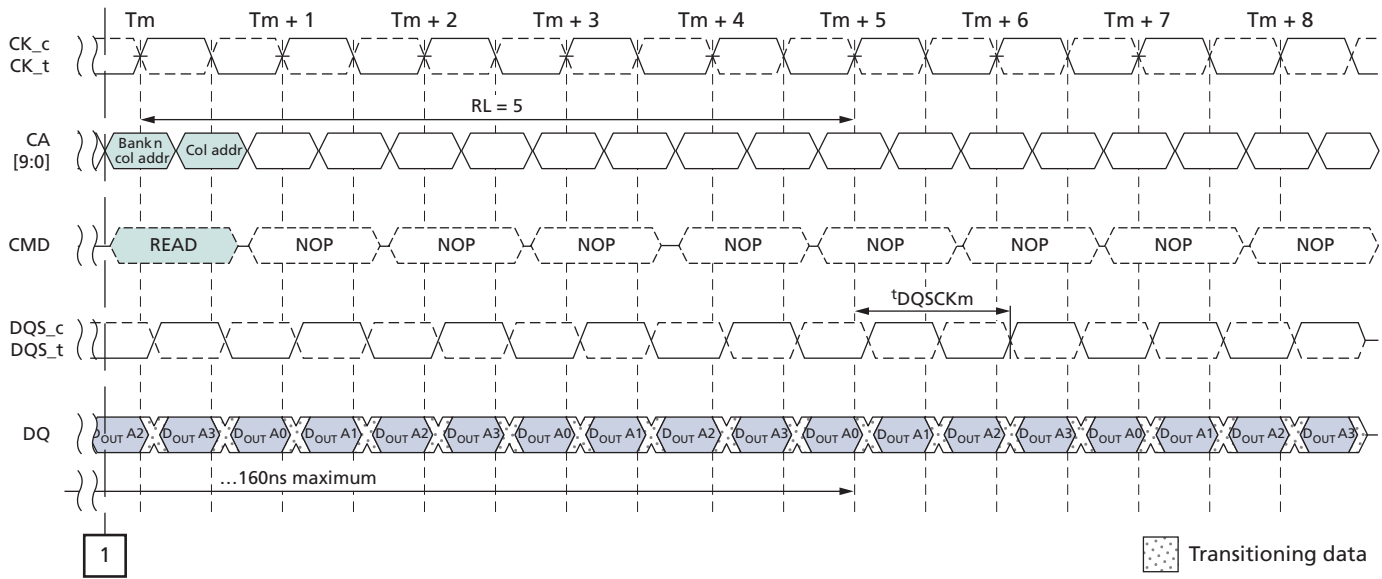


8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Burst READ Command

Figure 25: t_{DQSKDS} Timing



1



1

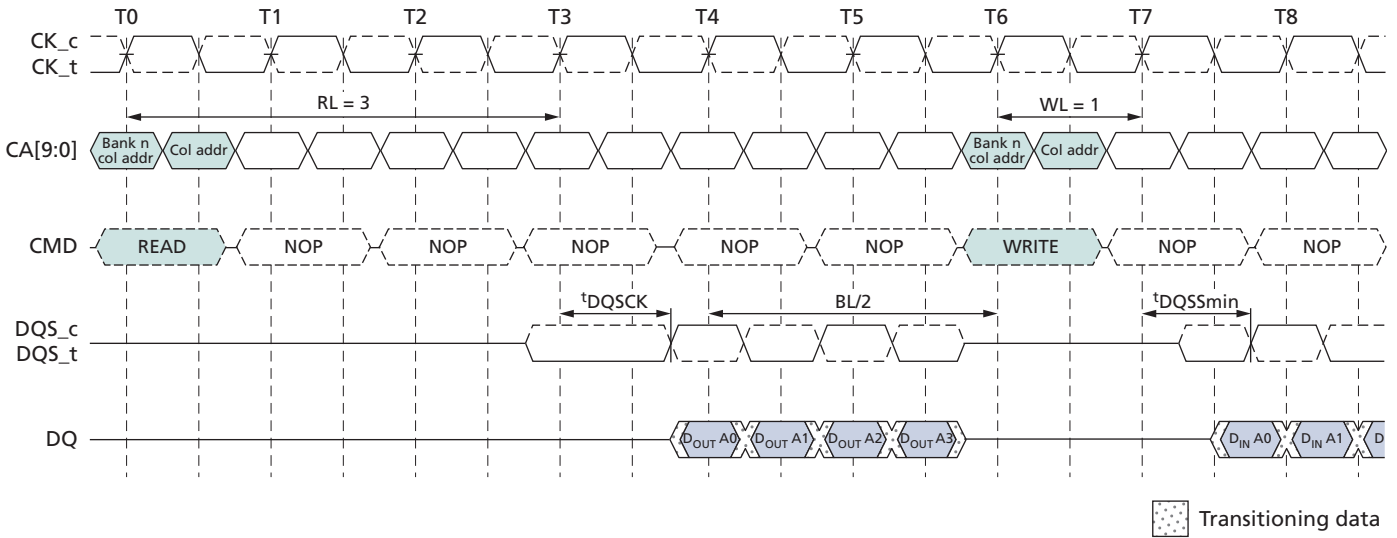
Transitioning data

- Notes:
1. $t_{DQSKDS} = (t_{DQSKn} - t_{DQSKm})$.
 2. $t_{DQSKDS} (MAX)$ is defined as the maximum of ABS ($t_{DQSKn} - t_{DQSKm}$) for any (t_{DQSKn} , t_{DQSKm}) pair for READs within a consecutive burst, within any 160ns rolling window.



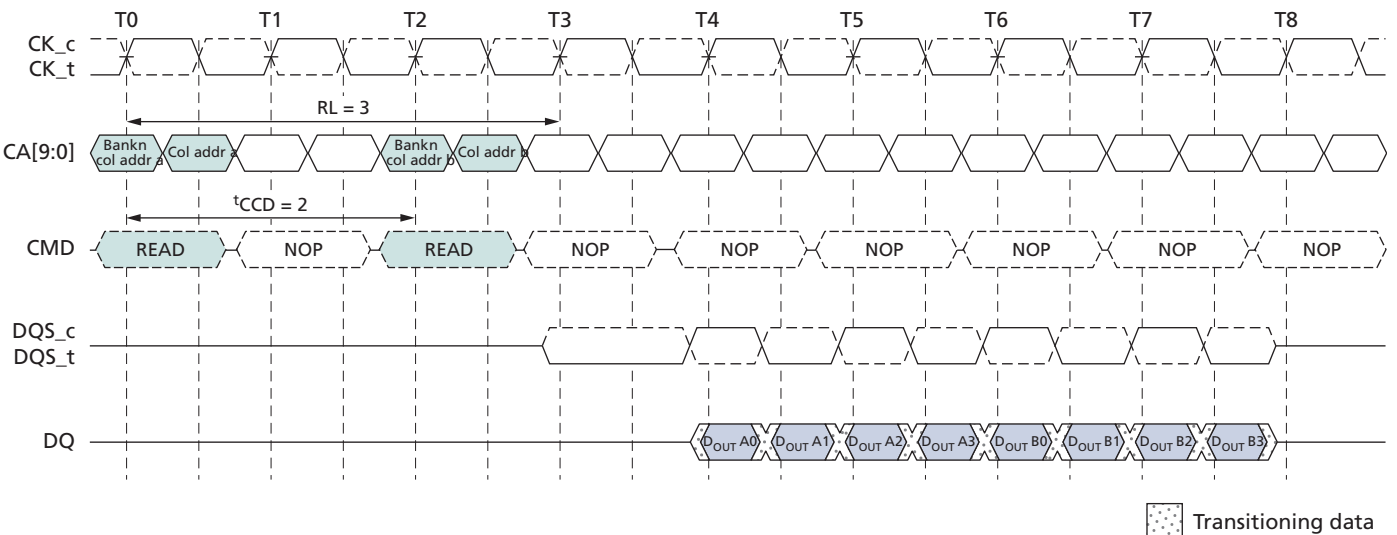
8Gb: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Burst READ Command

Figure 26: Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is $RL + RU(t_{DQSCK}(MAX)/t_{CK}) + BL/2 + 1 - WL$ clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used for BL when calculating the minimum READ-to-WRITE delay.

Figure 27: Seamless Burst READ – RL = 3, BL = 4, $t_{CCD} = 2$



A seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and



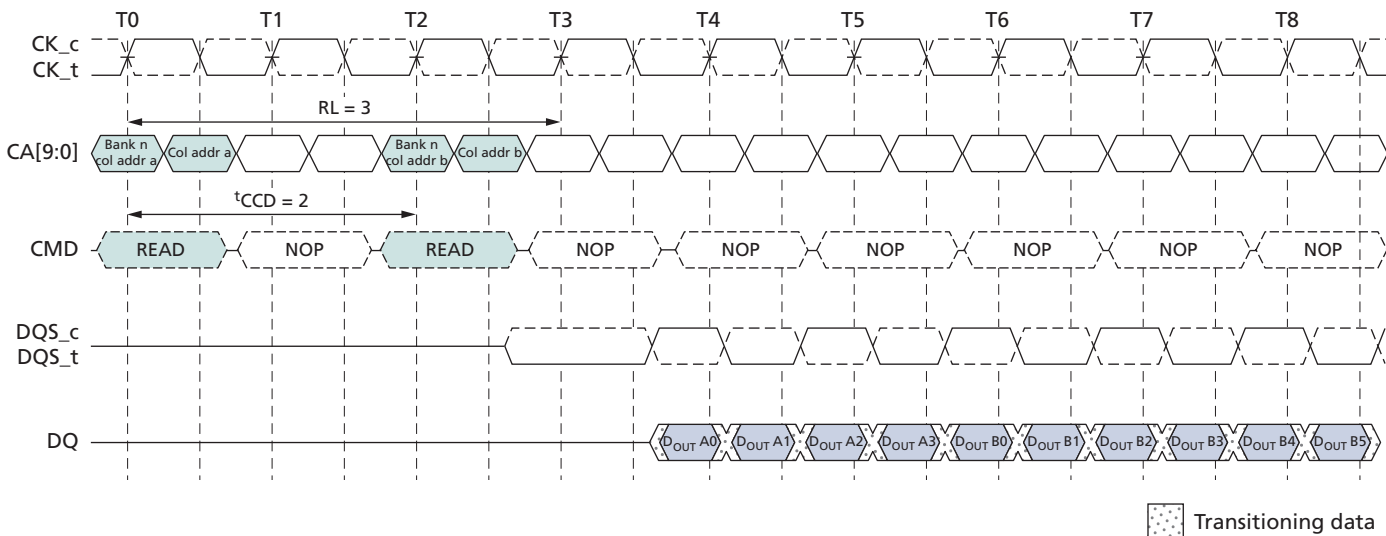
8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Burst WRITE Command

every eighth clock cycle for BL = 16 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

READs Interrupted by a READ

A burst READ can be interrupted by another READ with a 4-bit burst boundary, provided that t_{CCD} is met.

Figure 28: READ Burst Interrupt Example – RL = 3, BL = 8, $t_{CCD} = 2$



- Notes:
1. For DDR2 Mobile RAM-S4 devices, a READ burst interrupt function is allowed only on a burst of 8 and 16.
 2. For DDR2 Mobile RAM-S4 devices, a READ burst interrupt can occur only on even clock cycles after a previous READ command, provided that t_{CCD} is met.
 3. A READ can be interrupted only by other READ commands or by a BST command.
 4. A READ burst to any bank inside DRAM can be interrupted.
 5. A READ burst with auto-precharge cannot be interrupted.
 6. The effective burst length of the first READ equals two times the number of clock cycles between the first READ and the interrupting READ.

Burst WRITE Command

The burst WRITE command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the t_{DQSS} delay is measured. The first valid data must be driven $WL \times t_{CK} + t_{DQSS}$ from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS_t, DQS_c) must be driven LOW t_{WPRE} prior to data input. The burst cycle data bits must be applied to the DQ pins t_{DS} prior to the associated edge of the DQS_t, DQS_c and held valid until t_{DH} after that edge. Burst data is sampled on successive edges of the DQS_t, DQS_c until the 4-, 8-, or 16-bit burst length is completed. After a burst WRITE operation, t_{WR} must be satisfied before a PRECHARGE command to the same bank can be issued.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Burst WRITE Command

Pin input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

Figure 29: Data Input (WRITE) Timing

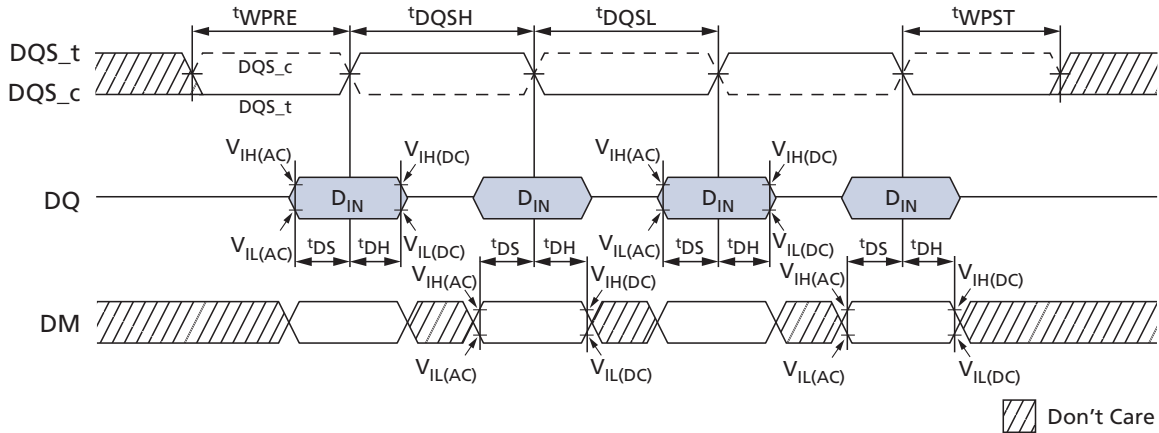
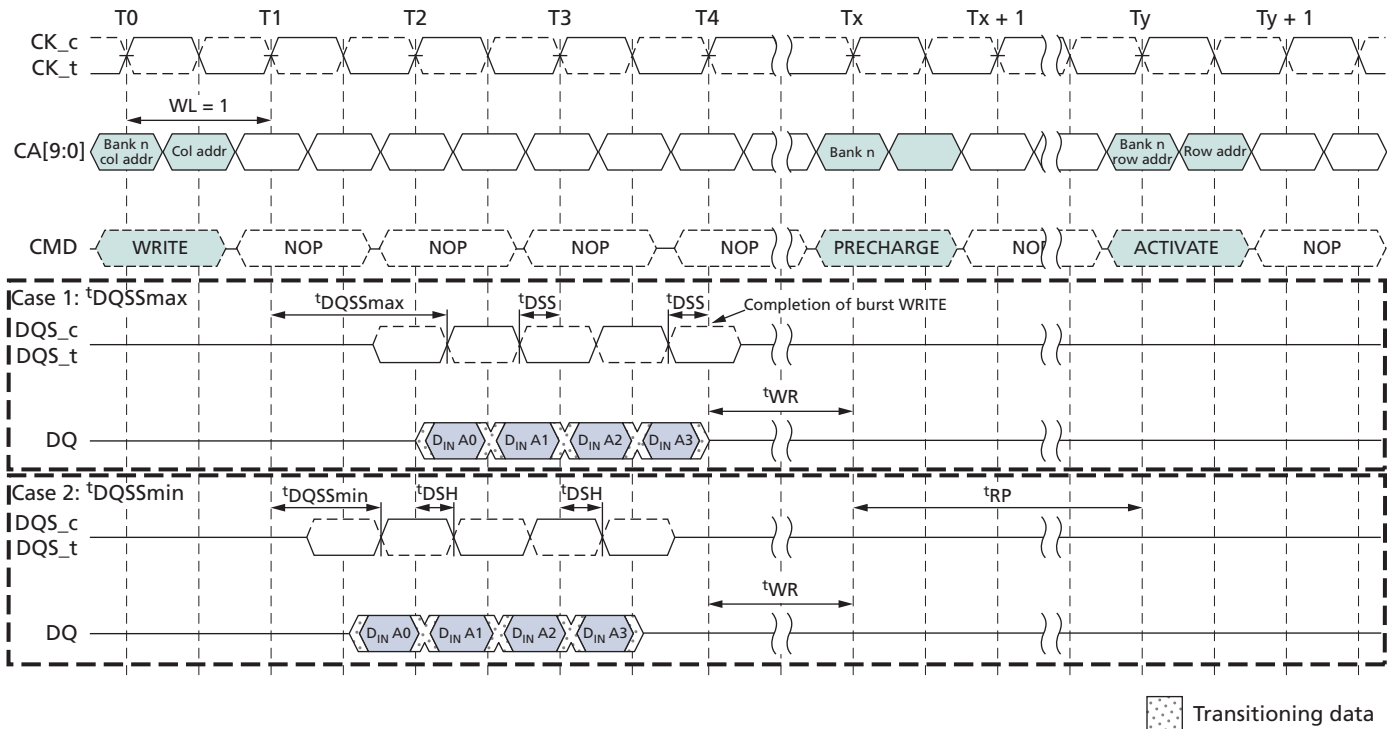


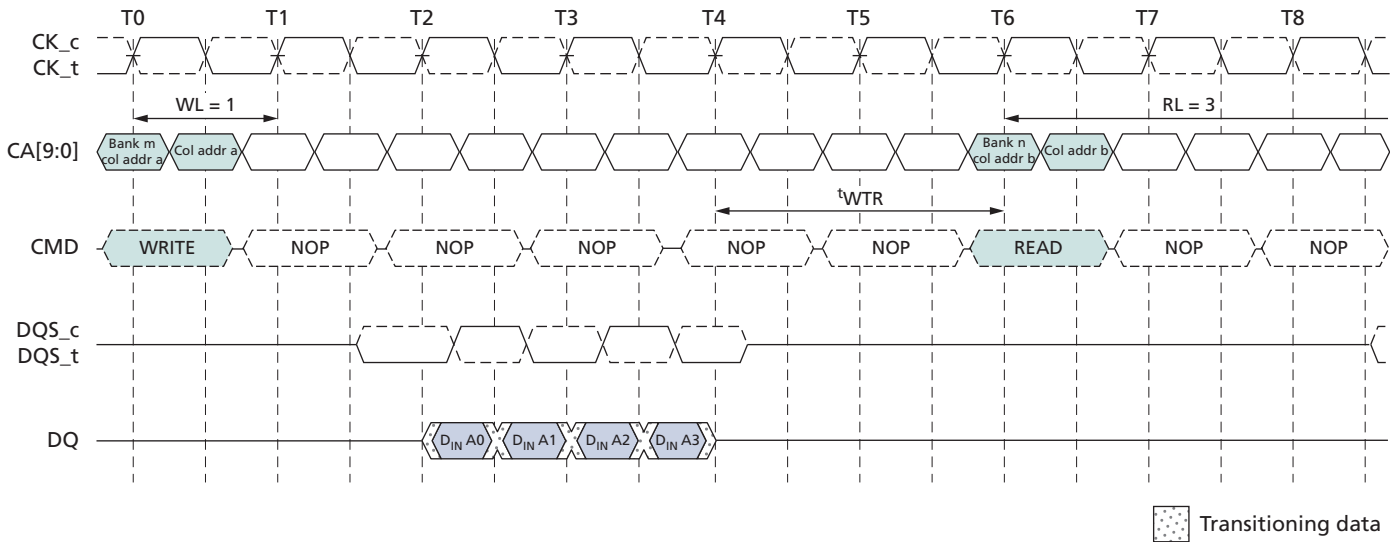
Figure 30: Burst WRITE - WL = 1, BL = 4





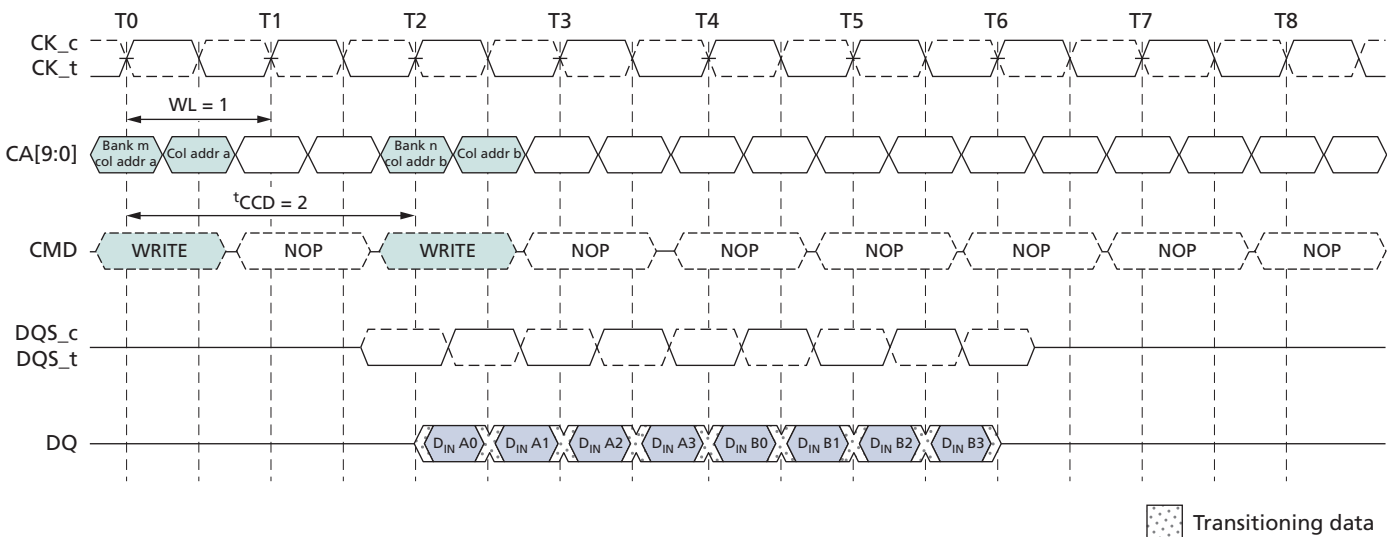
8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Burst WRITE Command

Figure 31: Burst WRITE Followed by Burst READ – RL = 3, WL = 1, BL = 4



- Notes:
1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$.
 2. t_{WTR} starts at the rising edge of the clock after the last valid input data.
 3. If a WRITE burst is truncated with a BST command, the effective burst length of the truncated WRITE burst should be used as BL to calculate the minimum WRITE-to-READ delay.

Figure 32: Seamless Burst WRITE – WL = 1, BL = 4, $t_{CCD} = 2$



- Note:
1. The seamless burst WRITE operation is supported by enabling a WRITE command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is supported for any activated bank.



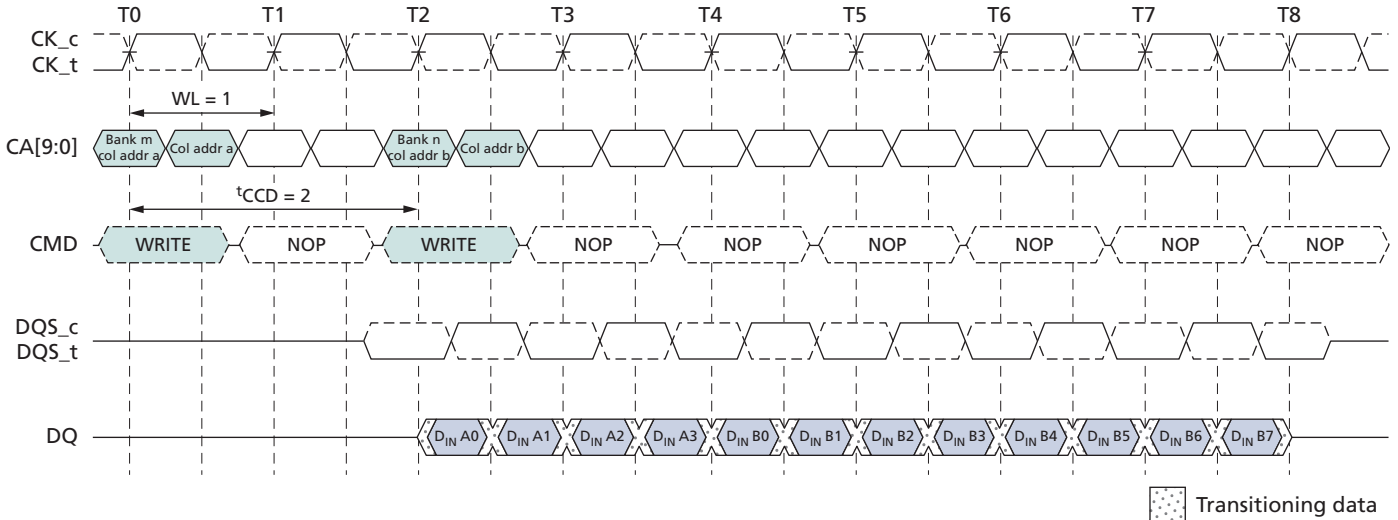
8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP BURST TERMINATE Command

WRITES Interrupted by a WRITE

A burst WRITE can be interrupted only by another WRITE with a 4-bit burst boundary, provided that t_{CCD} (MIN) is met.

A WRITE burst interrupt can occur on even clock cycles after the initial WRITE command, provided that t_{CCD} (MIN) is met.

Figure 33: WRITE Burst Interrupt Timing – WL = 1, BL = 8, $t_{CCD} = 2$



- Notes:
1. A WRITE operation can be interrupted only by another WRITE command or a BST command.
 2. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE.
 3. For DDR2 Mobile RAM-S4 devices, a WRITE burst interrupt function is allowed only on a burst of 8 and 16.
 4. For DDR2 Mobile RAM-S4 devices, a WRITE burst interrupt can occur only on even clock cycles after the previous WRITE command, provided that $t_{CCD}(\text{min})$ is met.
 5. A WRITE burst to any bank inside DRAM can be interrupted.
 6. A WRITE burst with auto-precharge cannot be interrupted.

BURST TERMINATE Command

The BURST TERMINATE (BST) command is initiated with CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can be issued only to terminate an active READ or WRITE burst. Therefore, a BST command can be issued only up to and including BL/2 - 1 clock cycles after a READ or WRITE command. The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

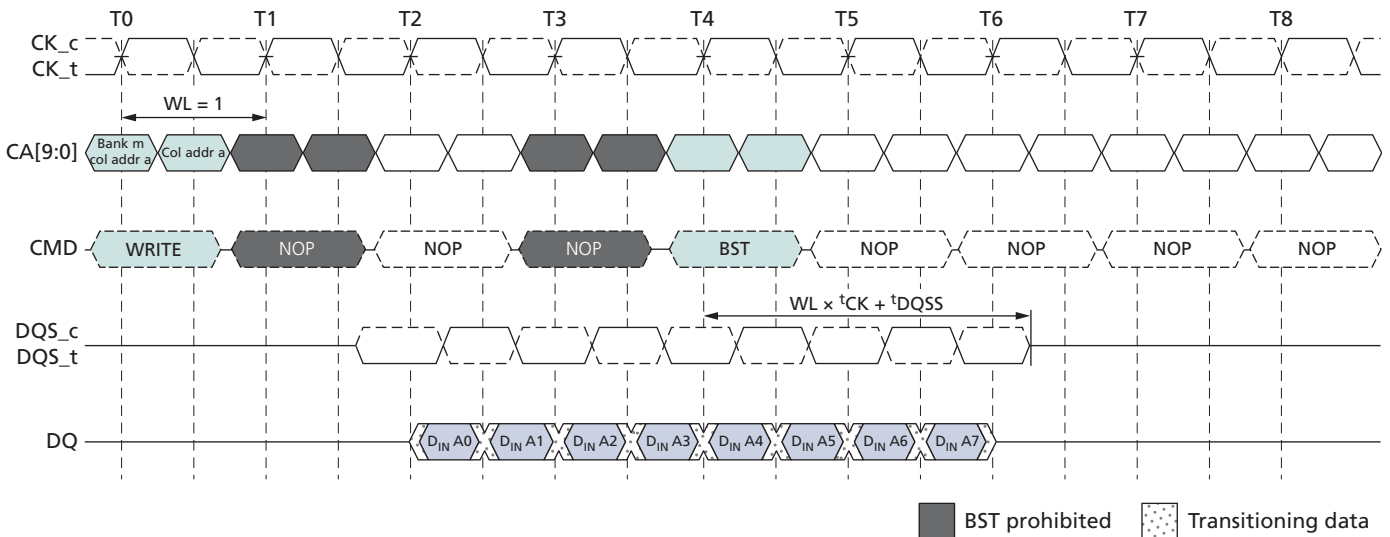
- Effective burst length = $2 \times$ (number of clock cycles from the READ or WRITE command to the BST command).
- If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for BL when calculating the minimum READ-to-WRITE or WRITE-to-READ delay.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP BURST TERMINATE Command

- The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst $RL \times {}^tCK + {}^tDQSK + {}^tDQSQ$ after the rising edge of the clock where the BST command is issued. The BST command truncates an ongoing WRITE burst $WL \times {}^tCK + {}^tDQSS$ after the rising edge of the clock where the BST command is issued.
- The 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of four.

Figure 34: Burst WRITE Truncated by BST – WL = 1, BL = 16

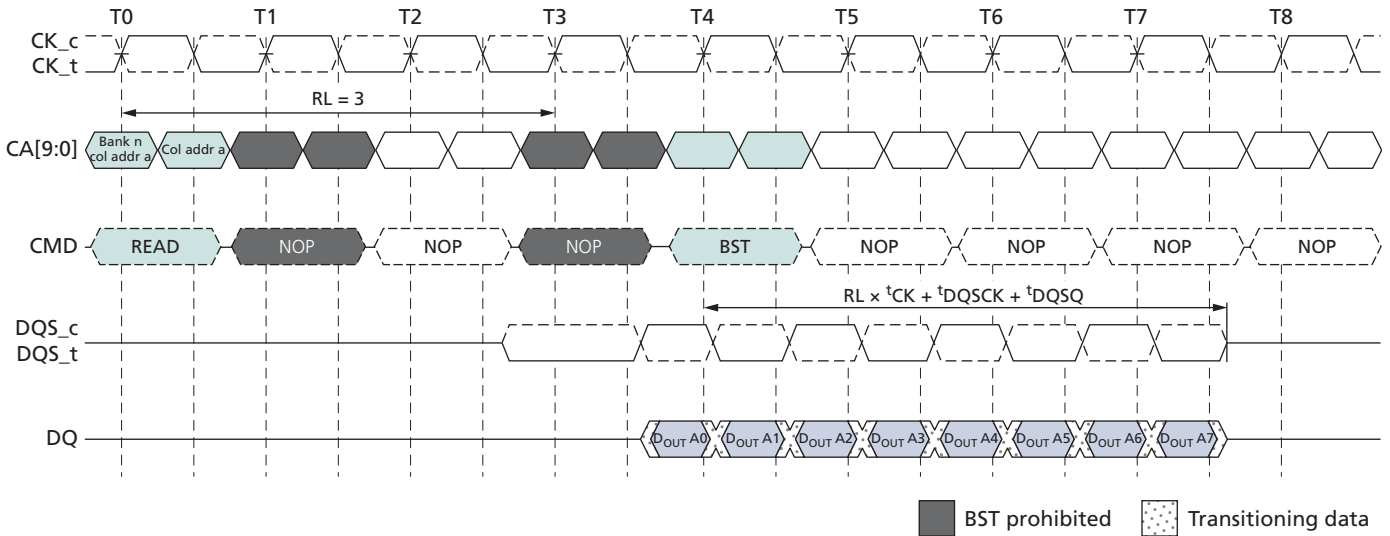


- Notes:
1. The BST command truncates an ongoing WRITE burst $WL \times {}^tCK + {}^tDQSS$ after the rising edge of the clock where the BST command is issued.
 2. BST can only be issued an even number of clock cycles after the WRITE command.
 3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Write Data Mask

Figure 35: Burst READ Truncated by BST – RL = 3, BL = 16

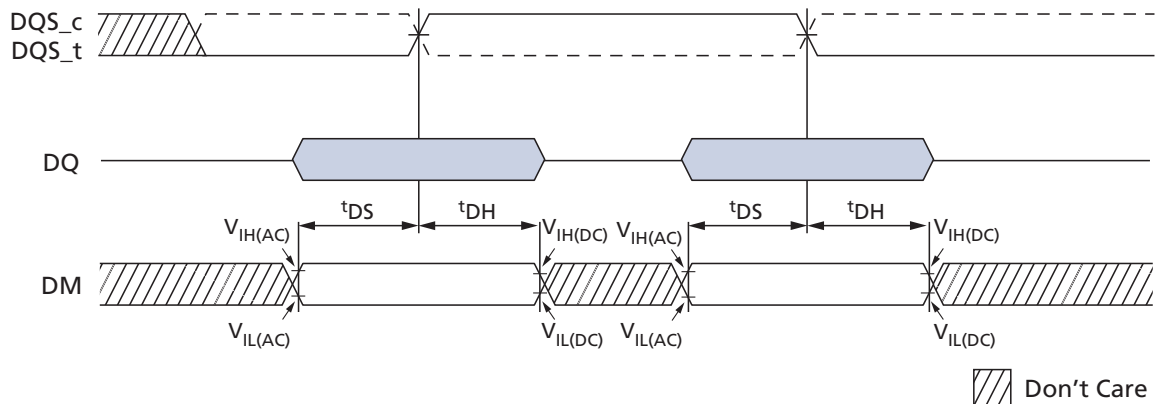


- Notes:
1. The BST command truncates an ongoing READ burst ($RL \times t_{CK} + t_{DQSK} + t_{DQSQ}$) after the rising edge of the clock where the BST command is issued.
 2. BST can only be issued an even number of clock cycles after the READ command.
 3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.

Write Data Mask

On the LPDDR2 device, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data mask loading is identical to data bit loading to ensure matched system timing.

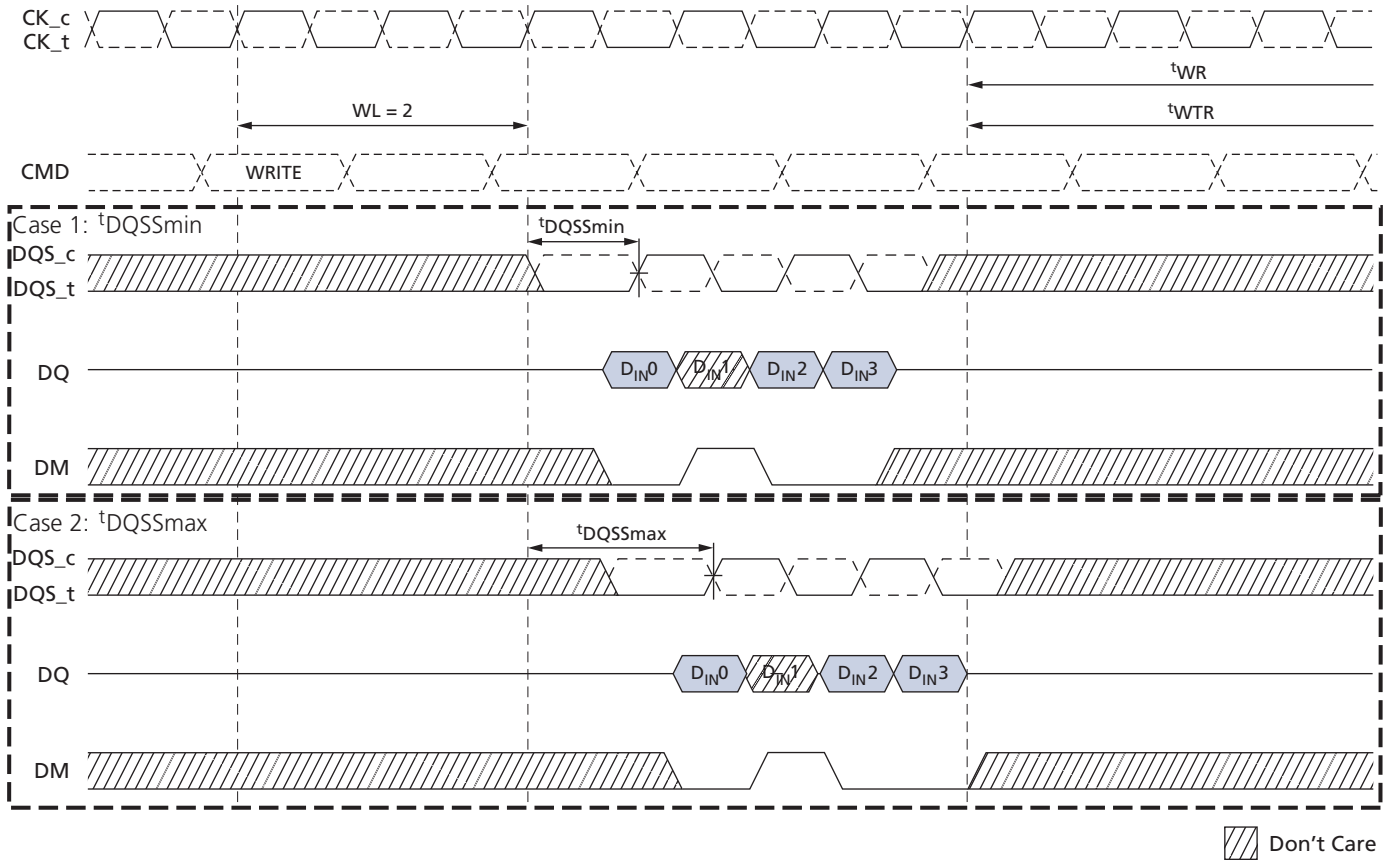
Figure 36: Data Mask Timing





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
PRECHARGE Command

Figure 37: Write Data Mask – Second Data Bit Masked



Note: 1. For the data mask function, $WL = 2$, $BL = 4$ is shown; the second data bit is masked.

PRECHARGE Command

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. For a 4-bank device, the AB flag and bank address bits BA0 and BA1 are used to determine which bank(s) to precharge. For an 8-bank device, the AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access t_{RPab} after an all bank PRECHARGE command is issued, or t_{RPpb} after a single-bank PRECHARGE command is issued.

To ensure that an 8-bank device can meet the instantaneous current demand required to operate, the row precharge time (t_{RP}) for an all bank PRECHARGE in an 8-bank device (t_{RPab}) will be longer than the row precharge time for a single-bank PRECHARGE (t_{RPpb}). For a 4-bank device, t_{RPab} is equal to t_{RPpb} .

ACTIVATE to PRECHARGE timing is shown in ACTIVATE Command.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
PRECHARGE Command

Table 55: Bank Selection for PRECHARGE by Address Bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-Bank Device	Precharged Bank(s) 8-Bank Device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	Don't Care	Don't Care	Don't Care	All banks	All banks

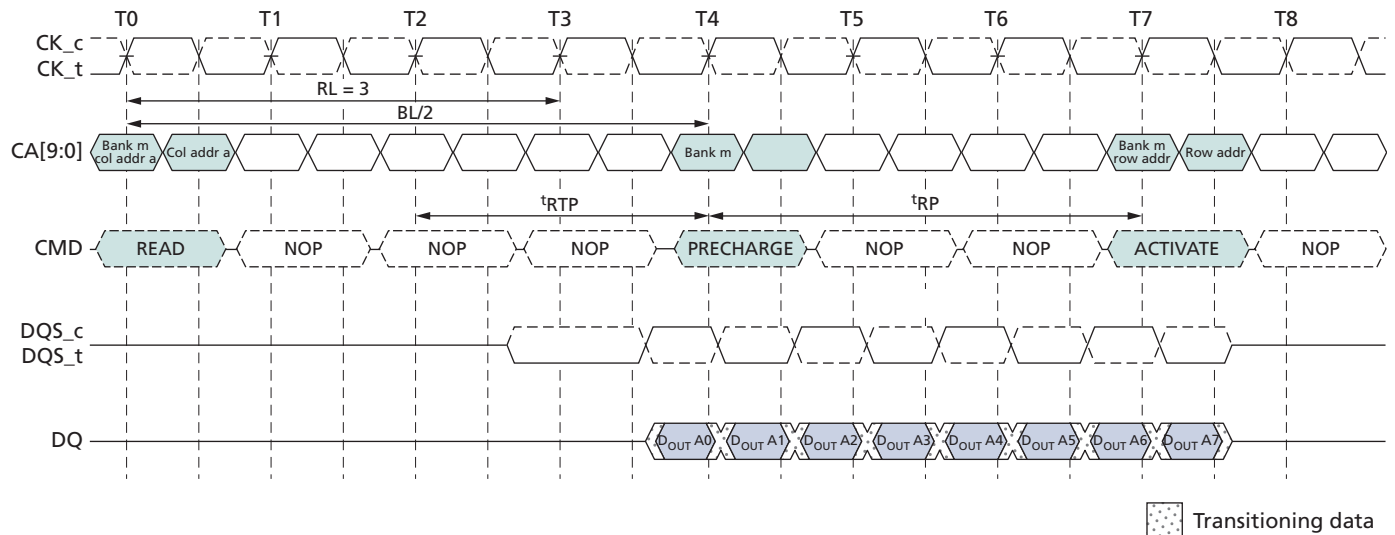
READ Burst Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (t_{RP}) has elapsed. A PRECHARGE command cannot be issued until after t_{RAS} is satisfied.

The minimum READ-to-PRECHARGE time (t_{RTP}) must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ command. t_{RTP} begins BL/2 - 2 clock cycles after the READ command.

If the burst is truncated by a BST command, the effective BL value is used to calculate when t_{RTP} begins.

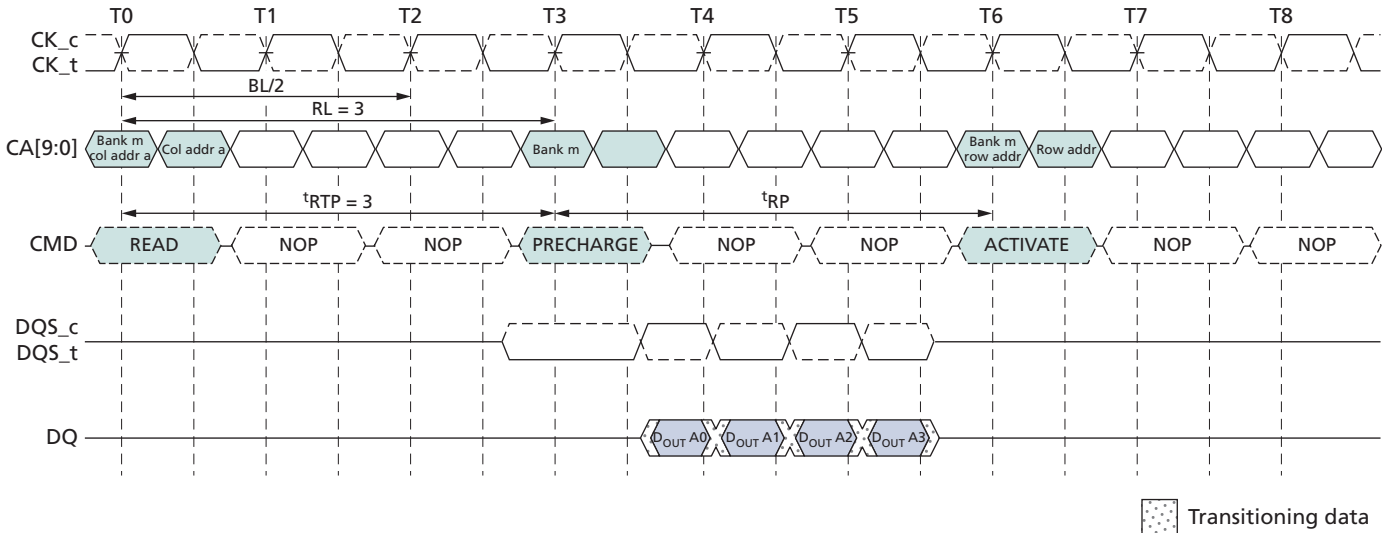
Figure 38: READ Burst Followed by PRECHARGE – RL = 3, BL = 8, $RU(t_{RTP(MIN)}/t_{CK}) = 2$





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP PRECHARGE Command

Figure 39: READ Burst Followed by PRECHARGE – RL = 3, BL = 4, $RU(t_{RTP(MIN)}/t_{CK}) = 3$



WRITE Burst Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (t_{WR}) must be provided before a PRECHARGE command can be issued. t_{WR} delay is referenced from the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the t_{WR} delay. For WRITE-to-PRECHARGE timings, see the PRECHARGE and Auto Precharge Clarification table.

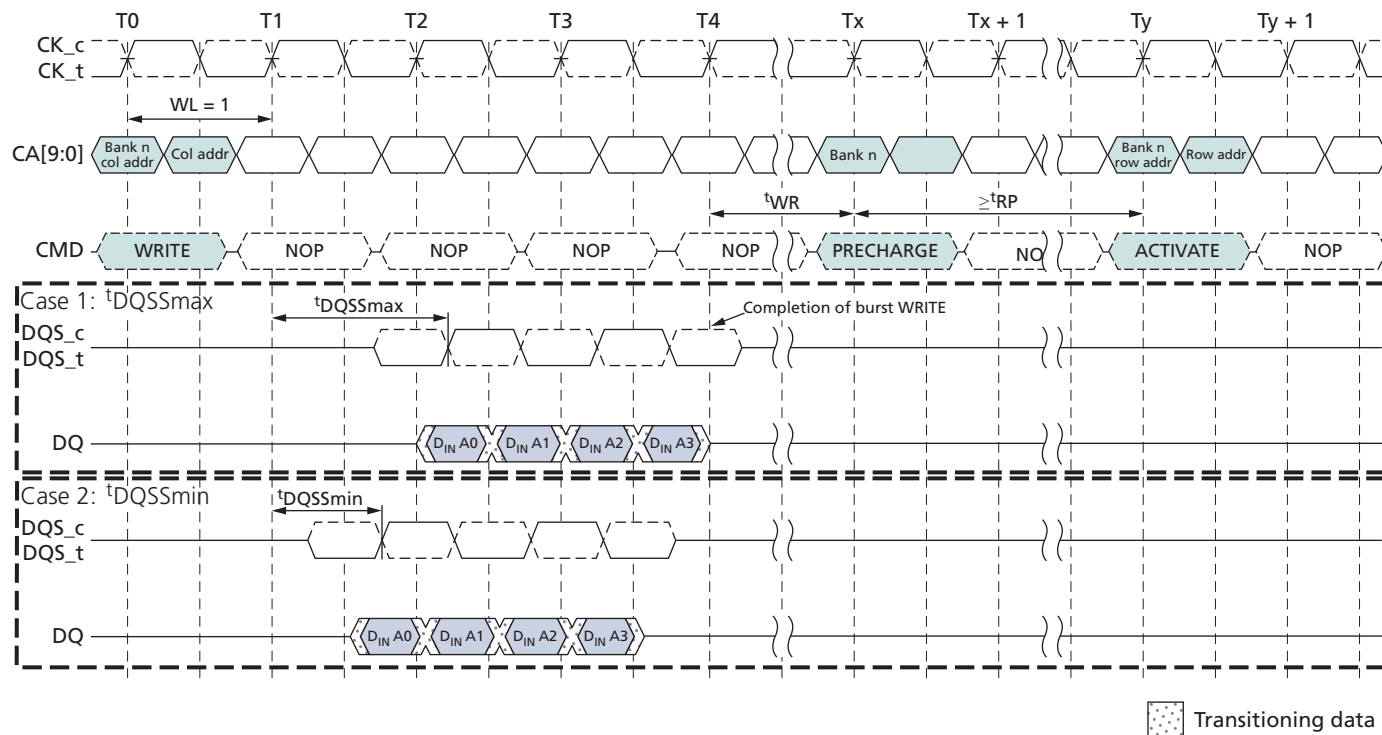
These devices write data to the array in prefetch quadruples (prefetch = 4). An internal WRITE operation can only begin after a prefetch group has been completely latched.

The minimum WRITE-to-PRECHARGE time for commands to the same bank is $WL + BL/2 + 1 + RU(t_{WR}/t_{CK})$ clock cycles. For untruncated bursts, BL is the value set in the mode register. For truncated bursts, BL is the effective burst length.



8Gb: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP PRECHARGE Command

Figure 40: WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4



Auto Precharge operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or WRITE command is issued to the device, the auto precharge bit (AP) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

READ Burst with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged.

This device starts an auto precharge on the rising edge of the clock BL/2 or BL/2 - 2 + RU (tRTP/tCK) clock cycles later than the READ with auto precharge command, whichever is greater. For auto precharge calculations, see the PRECHARGE and Auto Precharge Clarification table.

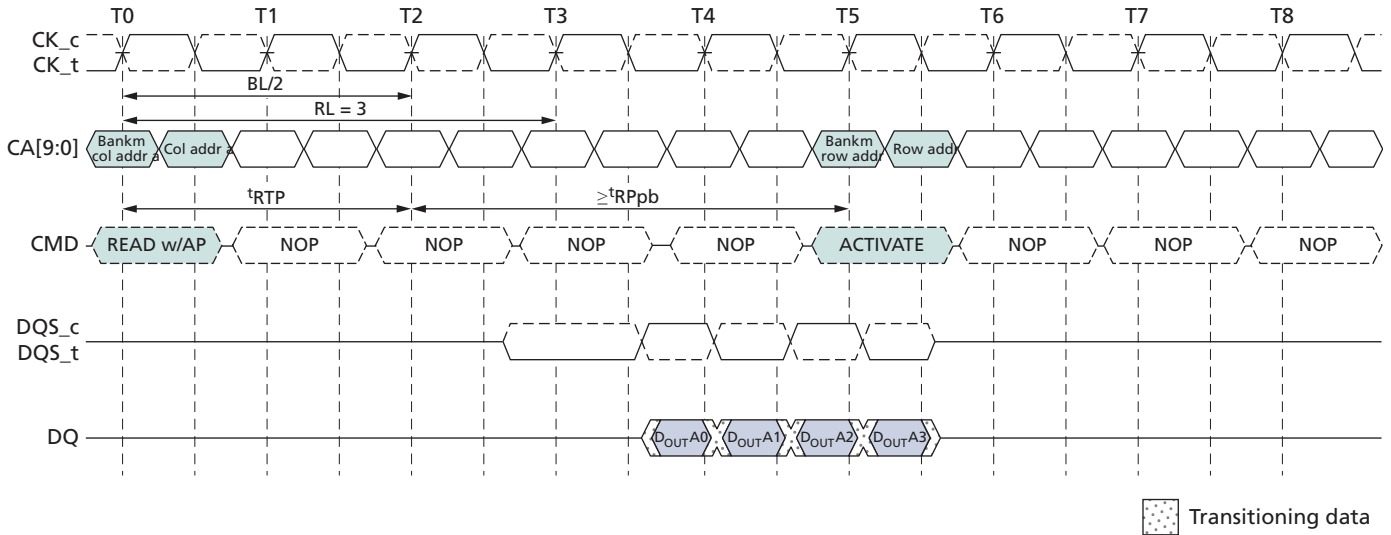


8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP PRECHARGE Command

Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

- The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Figure 41: READ Burst with Auto Precharge – RL = 3, BL = 4, $RU(t_{RTP(MIN)}/t_{CK}) = 2$



WRITE Burst with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge at the clock rising edge t_{WR} cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

- The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.



8Gb: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
PRECHARGE Command

Figure 42: WRITE Burst with Auto Precharge – WL = 1, BL = 4

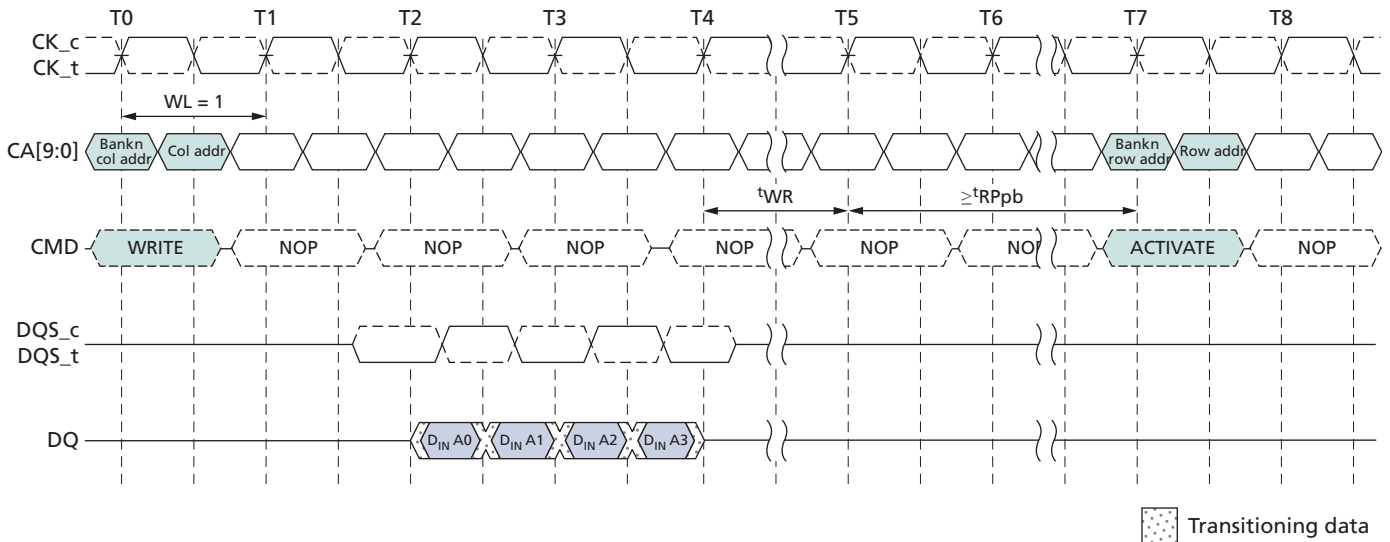


Table 56: PRECHARGE and Auto Precharge Clarification

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
READ	PRECHARGE to same bank as READ	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1
	PRECHARGE ALL	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1
BST	PRECHARGE to same bank as READ	1	CLK	1
	PRECHARGE ALL	1	CLK	1
READ w/AP	PRECHARGE to same bank as READ w/AP	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1, 2
	PRECHARGE ALL	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2$	CLK	1
	ACTIVATE to same bank as READ w/AP	$BL/2 + \text{MAX}(2, RU(t_{RTP}/t_{CK})) - 2 + RU(t_{RPpb}/t_{CK})$	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	$RL + BL/2 + RU(t_{DQSCkmax}/t_{CK}) - WL + 1$	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	BL/2	CLK	3
WRITE	PRECHARGE to same bank as WRITE	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	CLK	1
	PRECHARGE ALL	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	CLK	1
BST	PRECHARGE to same bank as WRITE	$WL + RU(t_{WR}/t_{CK}) + 1$	CLK	1
	PRECHARGE ALL	$WL + RU(t_{WR}/t_{CK}) + 1$	CLK	1


Table 56: PRECHARGE and Auto Precharge Clarification (Continued)

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
WRITE w/AP	PRECHARGE to same bank as WRITE w/AP	$WL + BL/2 + RU(t^{WR}/t^{CK}) + 1$	CLK	1, 2
	PRECHARGE ALL	$WL + BL/2 + RU(t^{WR}/t^{CK}) + 1$	CLK	1
	ACTIVATE to same bank as WRITE w/AP	$WL + BL/2 + RU(t^{WR}/t^{CK}) + 1 + RU(t^{RPpb}/t^{CK})$	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	BL/2	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	$WL + BL/2 + RU(t^{WTR}/t^{CK}) + 1$	CLK	3
PRECHARGE	PRECHARGE to same bank as PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1
PRECHARGE ALL	PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1

- Notes:
- For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command—either a one-bank PRECHARGE or PRECHARGE ALL—issued to that bank. The PRECHARGE period is satisfied after t^{RP} , depending on the latest PRECHARGE command issued to that bank.
 - Any command issued during the specified minimum delay time is illegal.
 - After READ with auto precharge, seamless READ operations to different banks are supported. After WRITE with auto precharge, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge must not be interrupted or truncated.

REFRESH Command

The REFRESH command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. A per-bank REFRESH command is initiated with CA3 LOW at the rising edge of the clock. The all-bank REFRESH command is initiated with CA3 HIGH at the rising edge of the clock. A per-bank REFRESH is only supported in devices with eight banks.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

- t^{RCab} has been satisfied after the prior REFab command
- t^{RCpb} has been satisfied after the prior REFpb command
- t^{RP} has been satisfied after the prior PRECHARGE command to that bank



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP REFRESH Command

t^{RRD} has been satisfied after the prior ACTIVATE command (when applicable, for example after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (t^{RFCpb}); however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or WRITE command.

When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- t^{RFCpb} must be satisfied before issuing a REFab command
- t^{RFCpb} must be satisfied before issuing an ACTIVATE command to the same bank
- t^{RRD} must be satisfied before issuing an ACTIVATE command to a different bank
- t^{RFCpb} must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- t^{RFCab} has been satisfied following the prior REFab command
- t^{RFCpb} has been satisfied following the prior REFpb command
- t^{RP} has been satisfied following the prior PRECHARGE commands

After an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- t^{RFCab} latency must be satisfied before issuing an ACTIVATE command
- t^{RFCab} latency must be satisfied before issuing a REFab or REFpb command

Table 57: REFRESH Command Scheduling Separation Requirements

Symbol	Minimum Delay From	To	Notes
t^{RFCab}	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
t^{RFCpb}	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	


Table 57: REFRESH Command Scheduling Separation Requirements (Continued)

Symbol	Minimum Delay From	To	Notes
t_{RRD}	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb affecting an idle bank (different bank than activate)	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note: 1. A bank must be in the idle state before it is refreshed, so REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

REFRESH Requirements

1. Minimum Number of REFRESH Commands

Mobile LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window ($t_{REFW} = 32 \text{ ms @ MR4}[2:0] = 011$ or $T_C \leq 85^\circ\text{C}$). For actual values per density and the resulting average refresh interval (t_{REFI}), see Refresh Requirements.

For t_{REFW} and t_{REFI} refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) table.

For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

2. Burst REFRESH Limitation

To limit current consumption, a maximum of eight REFab commands can be issued in any rolling t_{REFBW} ($t_{REFBW} = 4 \times 8 \times t_{RFCab}$). This condition does not apply if REFpb commands are used.

3. REFRESH Requirements and Self Refresh

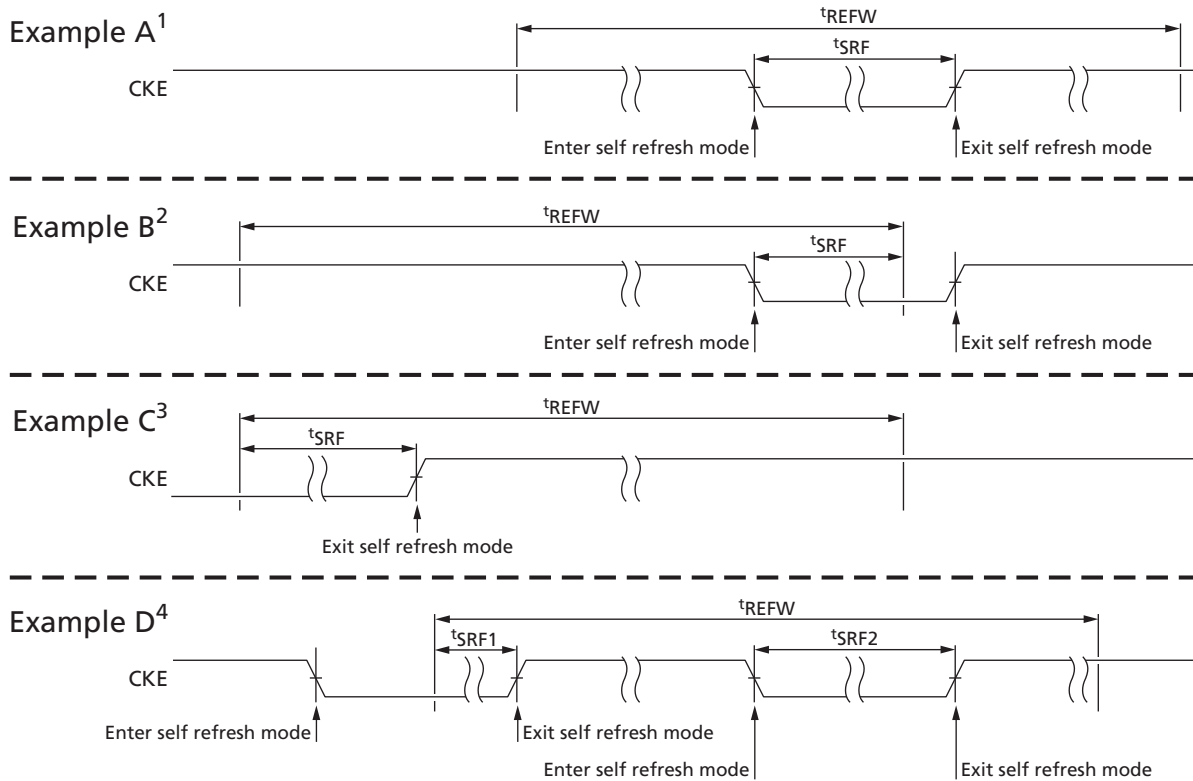
If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in that window is reduced to the following:

$$R' = R - RU \left(\frac{t_{SRF}}{t_{REFI}} \right) = R - RU \left(R \times \frac{t_{SRF}}{t_{REFW}} \right)$$

Where RU represents the round-up function



Figure 43: ^tSRF Definition



- Notes:
1. Time in self refresh mode is fully enclosed in the refresh window (t_{REFW}).
 2. At self refresh entry.
 3. At self refresh exit.
 4. Several intervals in self refresh during one t_{REFW} interval. In this example, $t_{SRF} = t_{SRF1} + t_{SRF2}$.

The mobile LPDDR2 device provides significant flexibility in scheduling a REFRESH command as long as the required boundary conditions are met (see the ^tSRF Definition figure).

In the most straightforward implementations, a REFRESH command should be scheduled every t_{REFI} . In this case, self refresh can be entered at any time.

Users may choose to deviate from this regular refresh pattern, for instance, to enable a period in which no refresh is required. As an example, using a 1Gb LPDDR2 device, the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by t_{REFBW}), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: $t_{REFW} - (R/8) \times t_{REFBW} = t_{REFW} - R \times 4 \times t_{RfCab}$.

For example, a 1Gb device at $T_C \leq 85^\circ\text{C}$ can be operated without a refresh for up to 32ms - $4096 \times 4 \times 130\text{ns} \approx 30\text{ms}$.

Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP REFRESH Command

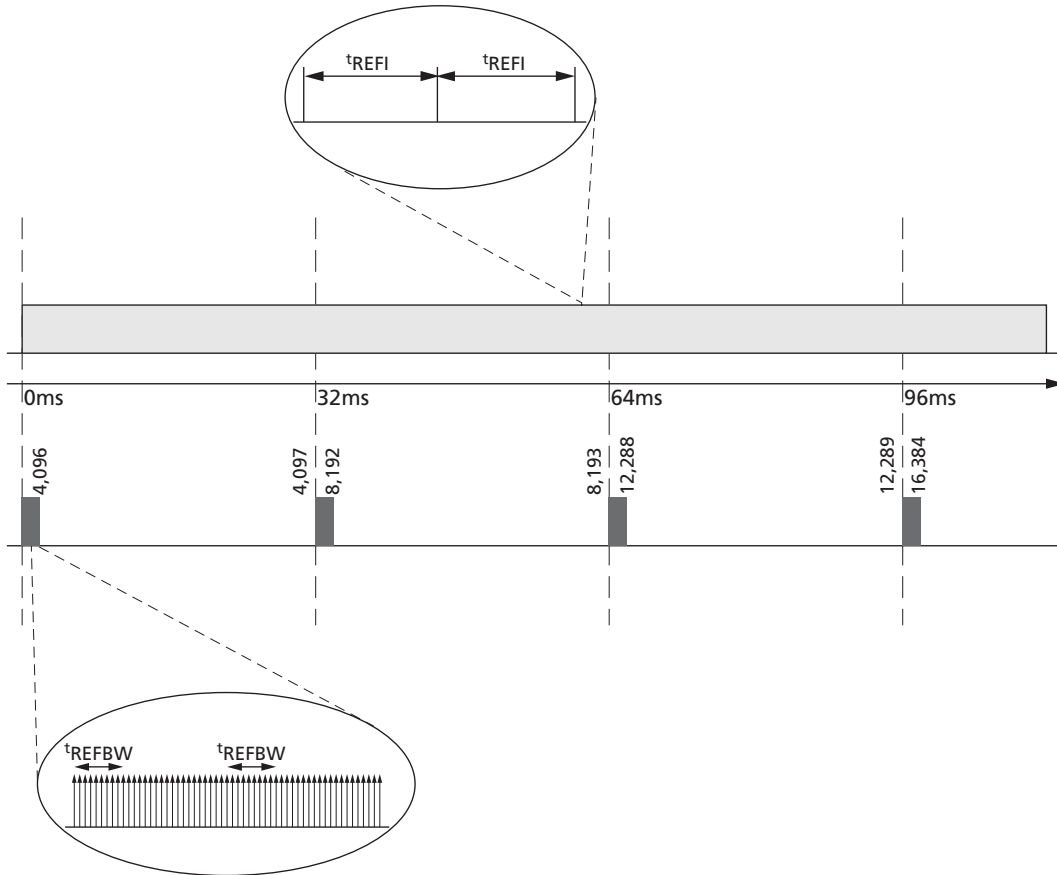
every rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern is shown in the Supported Transition from Repetitive REFRESH Burst figure. If this transition occurs immediately after the burst refresh phase, all rolling ^tREFW intervals will meet the minimum required number of REFRESH commands.

A nonsupported transition is shown below. In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling ^tREFW intervals, the minimum number of REFRESH commands is not satisfied.

Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed refresh pattern must be assumed. Micron recommends entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase (see the Recommended Self Refresh Entry and Exit figure).



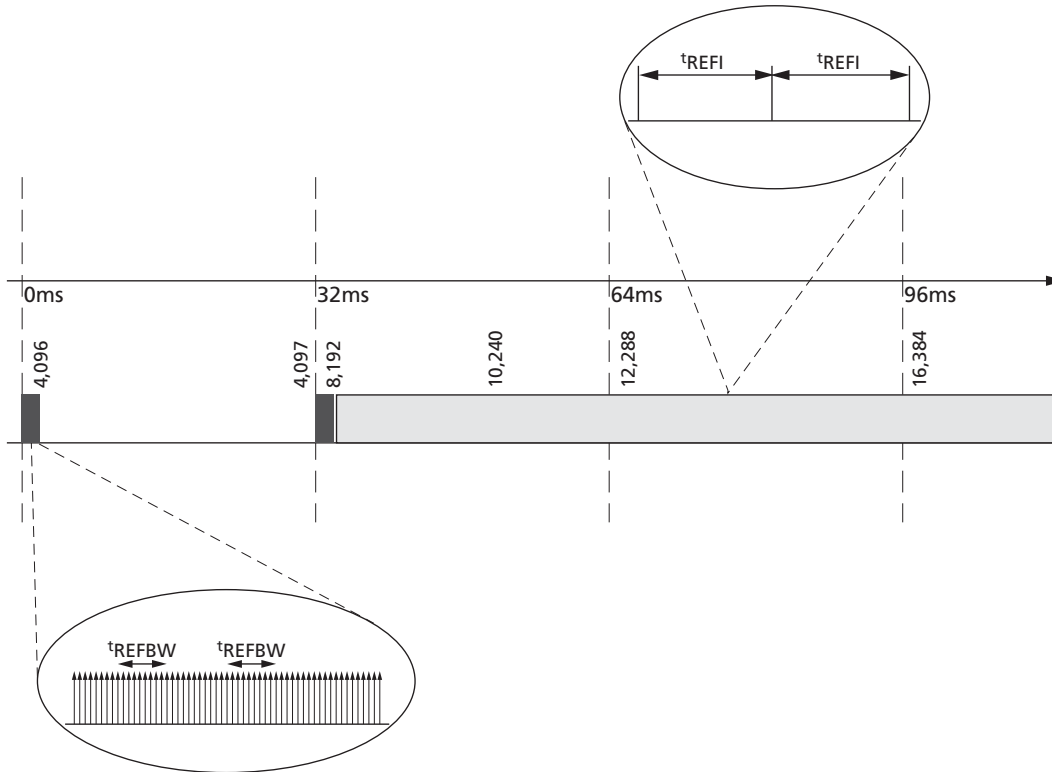
Figure 44: Regular Distributed Refresh Pattern



- Notes:
1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.
 2. As an example, in a 1Gb LPDDR2 device at $T_C \leq 85^\circ\text{C}$, the distributed refresh pattern has one REFRESH command per 7.8 μs ; the burst refresh pattern has one REFRESH command per 0.52 μs , followed by $\approx 30\text{ms}$ without any REFRESH command.



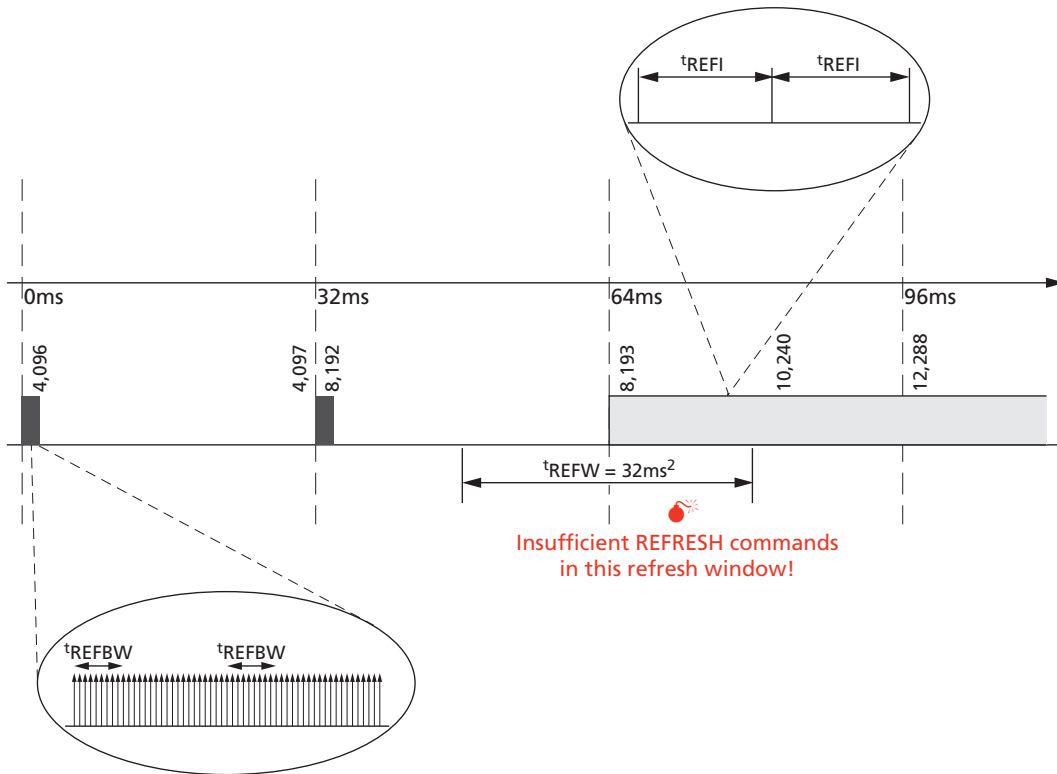
Figure 45: Supported Transition from Repetitive REFRESH Burst



- Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
 2. As an example, in a 1Gb LPDDR2 device at $T_C \leq 85^\circ\text{C}$, the distributed refresh pattern has one REFRESH command per $7.8\mu\text{s}$; the burst refresh pattern has one REFRESH command per $0.52\mu\text{s}$, followed by $\approx 30\text{ms}$ without any REFRESH command.



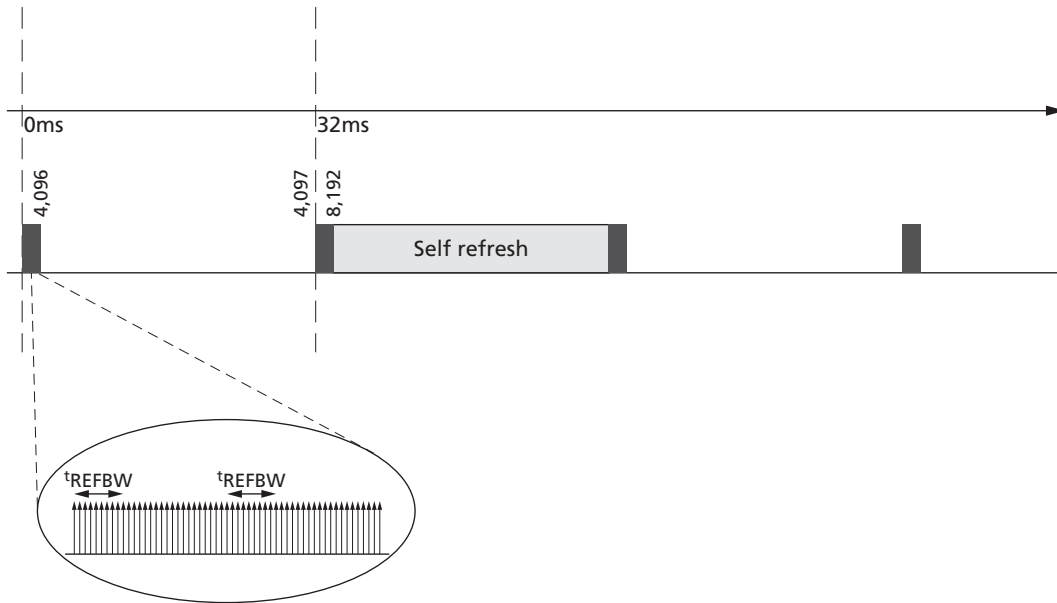
Figure 46: Nonsupported Transition from Repetitive REFRESH Burst



- Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
 2. There are only ≈ 2048 REFRESH commands in the indicated t_{REFW} window. This does not provide the required minimum number of REFRESH commands (R).



Figure 47: Recommended Self Refresh Entry and Exit



Note: 1. In conjunction with a burst/pause refresh pattern.



8Gb: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP SELF REFRESH Operation

Figure 48: All-Bank REFRESH Operation

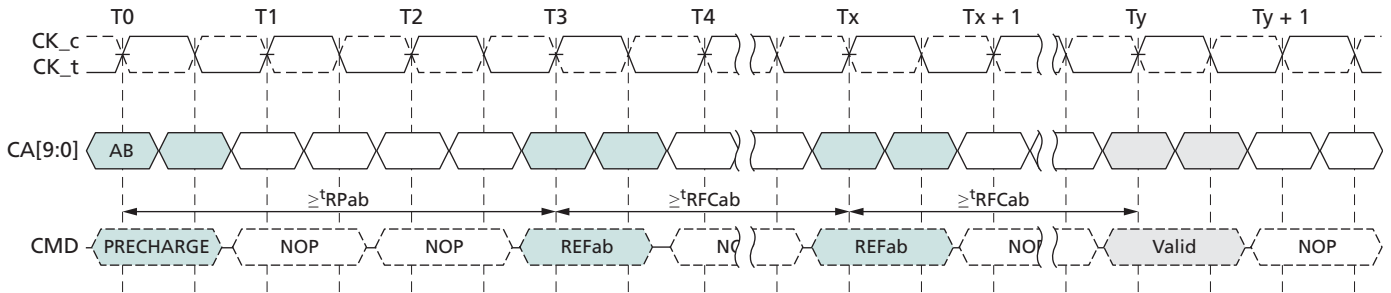
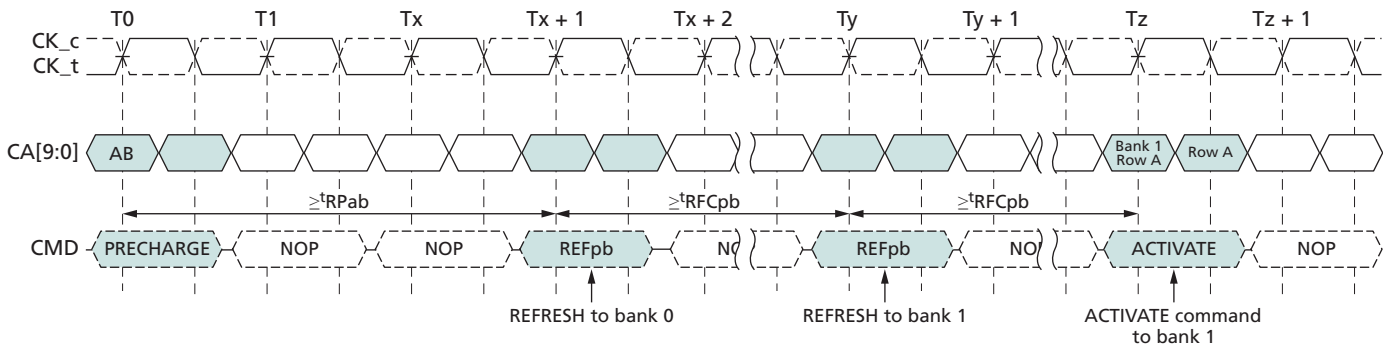


Figure 49: Per-Bank REFRESH Operation



- Notes:
1. Prior to T0, the REFpb bank counter points to bank 0.
 2. Operations to banks other than the bank being refreshed are supported during the t_{RFCpb} period.

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate the SELF REFRESH operation.

The SELF REFRESH command is executed by taking CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the POWER-DOWN command. Once the command is registered, CKE must be held LOW to keep the device in self-refresh mode.

The mobile LPDDR2 device can operate in self refresh mode in both the standard and extended temperature ranges. The device also manages self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range (See IDD Specifications for details).

After the device has entered self refresh mode, all external signals other than CKE are “Don’t Care.” For proper self refresh operation, power supply pins (V_{DD1} , V_{DD2} , and V_{DDQ}) must be at valid levels. V_{DDQ} can be turned off during self refresh. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting self refresh, both V_{DDQ} and



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP SELF REFRESH Operation

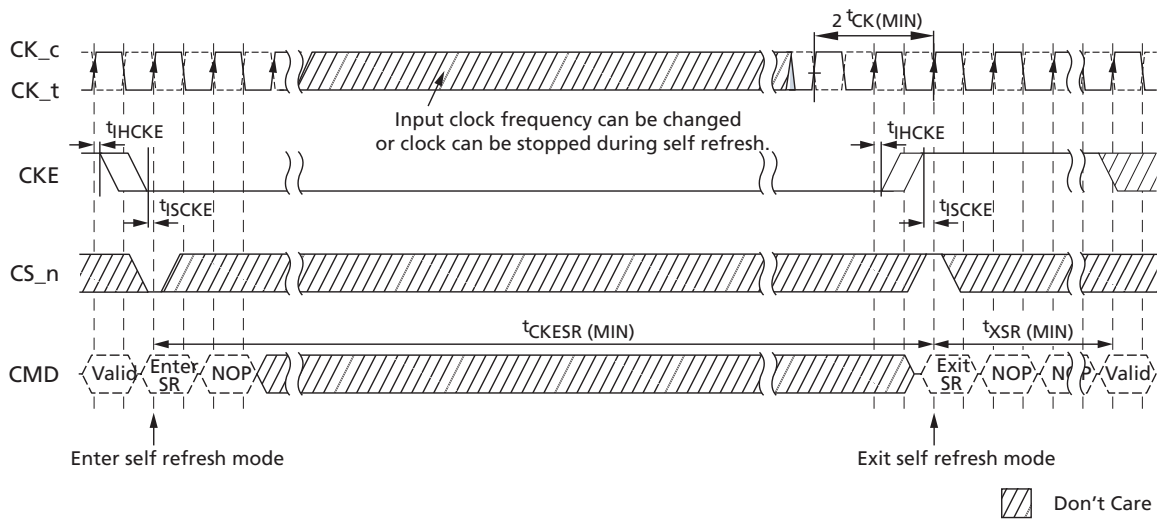
V_{REFDQ} must be within their respective minimum/maximum operating ranges (see the Single-Ended AC and DC Input Levels for DQ and DM table). V_{REFDQ} can be at any level between 0 and V_{DDQ} ; V_{REFCA} can be at any level between 0 and V_{DD2} during self refresh.

Before exiting self refresh, V_{REFDQ} and V_{REFCA} must be within specified limits (See AC and DC Logic Input Measurement Levels for Single-Ended Signals for details). After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during t_{CKESR} . The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least t_{CKESR} . The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.

Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval (t_{XSR}), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout t_{XSR} . NOP commands must be registered on each rising clock edge during t_{XSR} .

Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command or eight per-bank commands) must be issued before issuing a subsequent SELF REFRESH command.

Figure 50: SELF REFRESH Operation



- Notes:
1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of two cycles of stable clocks are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.
 2. The device must be in the all banks idle state prior to entering self refresh mode.
 3. t_{XSR} begins at the rising edge of the clock after CKE is driven HIGH.
 4. A valid command can be issued only after t_{XSR} is satisfied. NOPs must be issued during t_{XSR} .



Partial-Array Self Refresh – Bank Masking

Any device of densities of 64Mb–512Mb is comprised of four banks; a device of 1Gb density or higher is comprised of eight banks. Each bank can be configured independently whether or not a SELF REFRESH operation will occur in that bank. One 8-bit mode register (accessible via the MRW command) is assigned to program the bank-masking status of each bank up to eight banks. For bank masking assignments, see the MR16 PASR Bank Mask (MA[7:0] = 010h) and MR16 Op-Code Bit Definitions tables.

The mask bit to the bank enables or disables a refresh operation of the entire memory space within the bank. If a bank is masked using the bank mask register, a REFRESH operation to the entire bank is blocked and bank data retention is not guaranteed in self refresh mode. To enable a REFRESH operation to a bank, the corresponding bank mask bit must be programmed as “unmasked.” When a bank mask bit is unmasked, the array space being refreshed within that bank is determined by the programmed status of the segment mask bits.

Partial-Array Self Refresh – Segment Masking

Programming segment mask bits is similar to programming bank mask bits. For a density of 1Gb or higher, eight segments are used for masking (see the MR17 PASR Segment Mask (MA[7:0] = 011h) and MR17 PASR Segment Mask Definitions tables). A mode register is used for programming segment mask bits up to eight bits. For a density of less than 1Gb, segment masking is not supported.

When the mask bit to an address range (represented as a segment) is programmed as “masked,” a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled.

A segment masking scheme can be used in place of or in combination with a bank masking scheme. Each segment mask bit setting is applied across all banks. For segment masking bit assignments, see the tables noted above.

Table 58: Bank and Segment Masking Example

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0	–	M	–	–	–	–	–	M
Segment 1	0	–	M	–	–	–	–	–	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	–	M	–	–	–	–	–	M
Segment 4	0	–	M	–	–	–	–	–	M
Segment 5	0	–	M	–	–	–	–	–	M
Segment 6	0	–	M	–	–	–	–	–	M
Segment 7	1	M	M	M	M	M	M	M	M

Note: 1. This table provides values for an 8-bank device with REFRESH operations masked to banks 1 and 7, and segments 2 and 7.

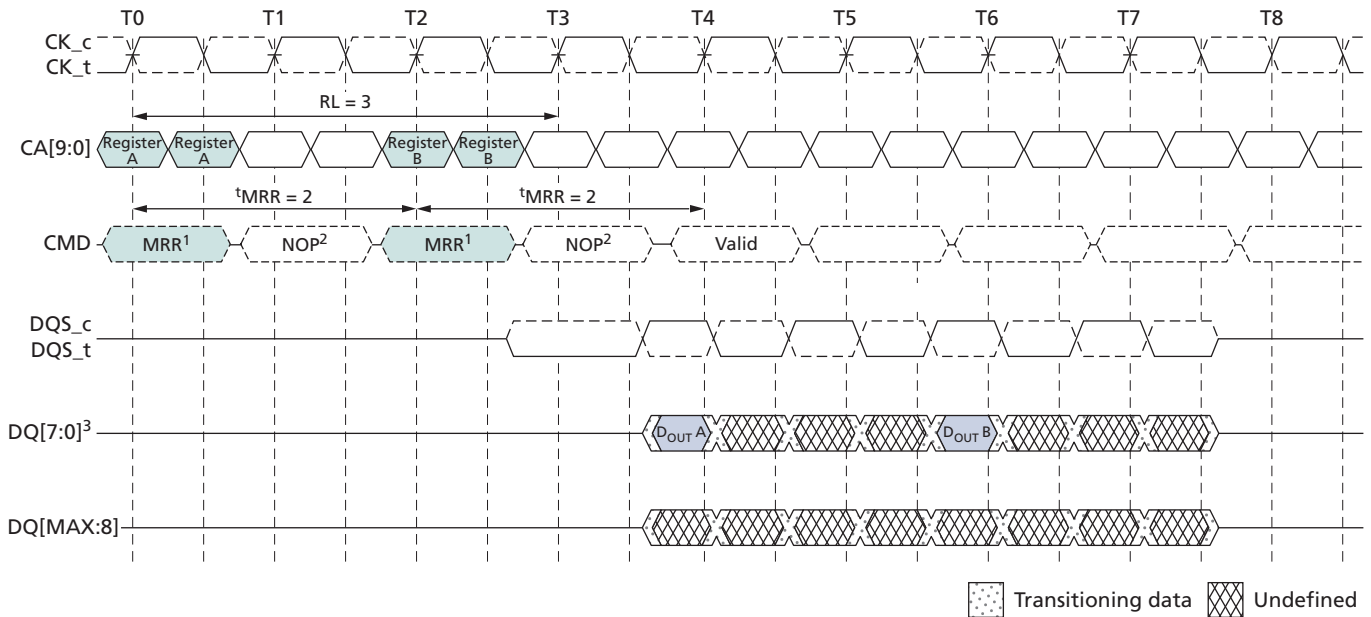


MODE REGISTER READ

The MODE REGISTER READ (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after $RL \times ^tCK + ^tDQSCK + ^tDQSQ$ and following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the Data Calibration Pattern Description table. All DQS_t, DQS_c are toggled for the duration of the mode register READ burst.

The MRR command has a burst length of four. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period (tMRR) is two clock cycles. The MRR command issued to reserved and write-only registers should return valid but undefined content on all data beats, and DQS_t, DQS_c should be toggled.

Figure 51: MRR Timing – RL = 3, $^tMRR = 2$



- Notes:
1. MRRs to DQ calibration registers MR32 and MR40 are described in the Data Calibration Pattern Description table.
 2. Only the NOP command is supported during tMRR .
 3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
 4. Minimum MRR to write latency is $RL + RU(^tDQSCK_{max}/^tCK) + 4/2 + 1 - WL$ clock cycles.
 5. Minimum MRR to MRW latency is $RL + RU(^tDQSCK_{max}/^tCK) + 4/2 + 1$ clock cycles.

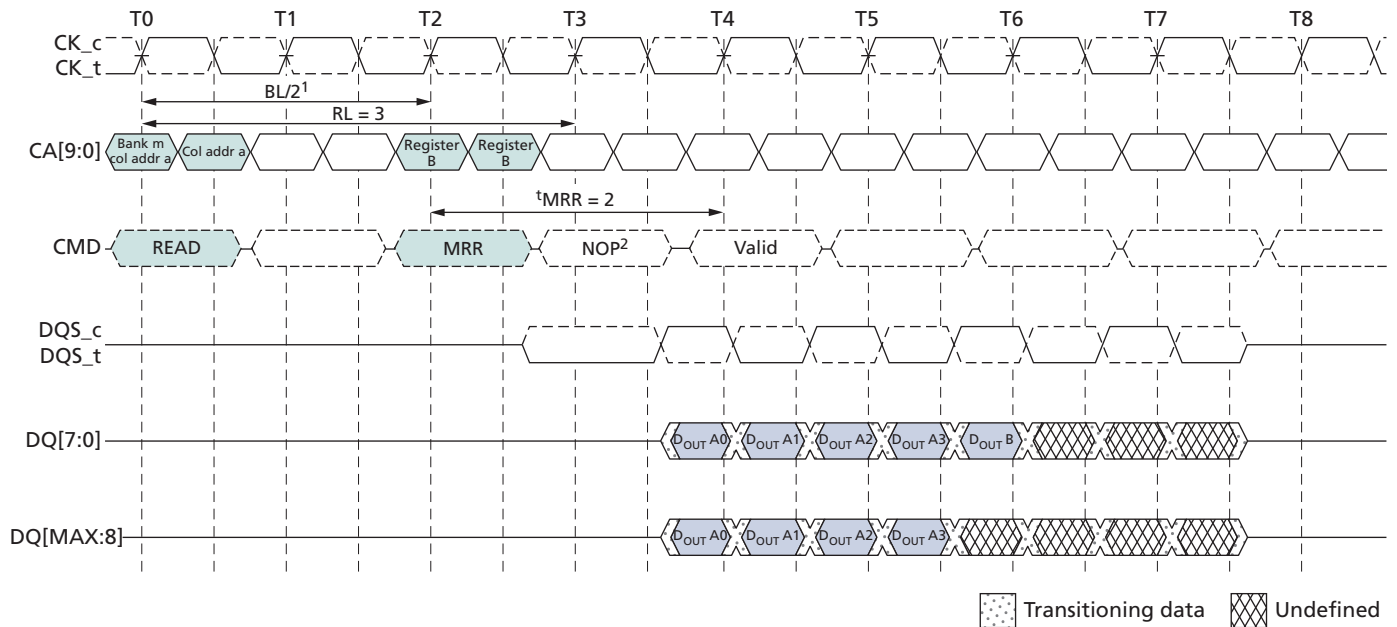
READ bursts and WRITE bursts cannot be truncated by MRR. Following a READ command, the MRR command must not be issued before BL/2 clock cycles have completed.



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Following a WRITE command, the MRR command must not be issued before $WL + 1 + BL/2 + RU$ (t_{WTR}/t_{CK}) clock cycles have completed. If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the BL value.

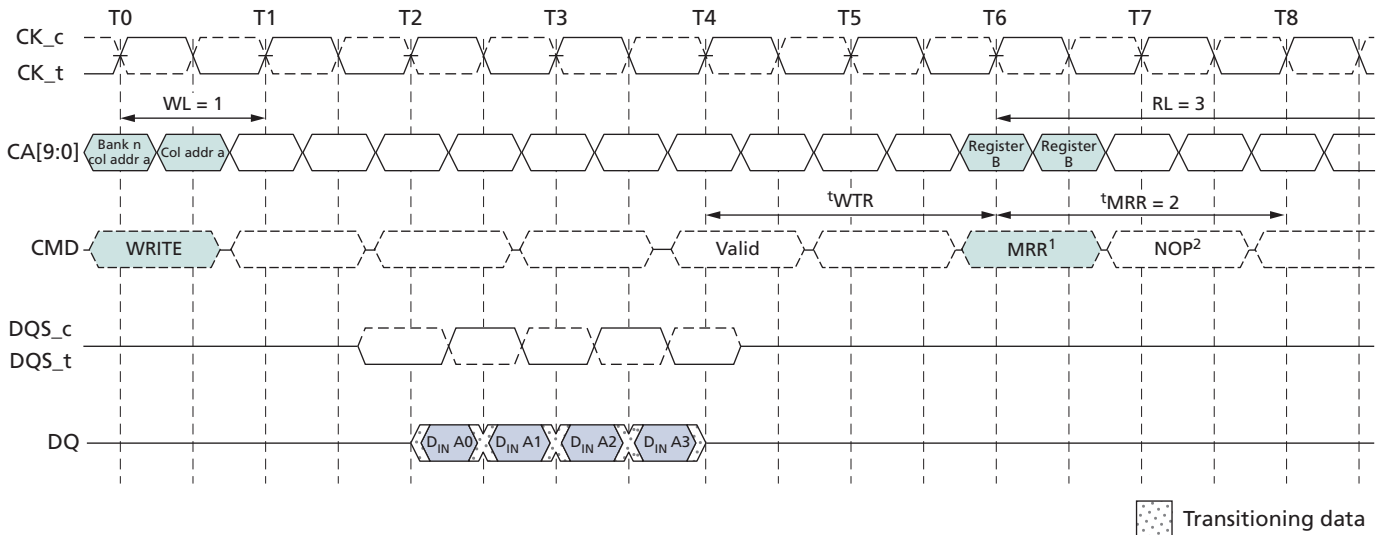
Figure 52: READ to MRR Timing – RL = 3, $t_{MRR} = 2$



- Notes:
1. The minimum number of clock cycles from the burst READ command to the MRR command is $BL/2$.
 2. Only the NOP command is supported during t_{MRR} .



Figure 53: Burst WRITE Followed by MRR – RL = 3, WL = 1, BL = 4



- Notes:
1. The minimum number of clock cycles from the burst WRITE command to the MRR command is $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$.
 2. Only the NOP command is supported during t_{MRR} .

Temperature Sensor

The mobile LPDDR2 device features a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine whether operating temperature requirements are being met (see Operating Temperature Range table).

Temperature sensor data can be read from MR4 using the mode register read protocol. Upon exiting self-refresh or power-down, the device temperature status bits will be no older than t_{TSI} .

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges (see table noted above). For example, T_{CASE} could be above 85°C when MR4[2:0] equals 011b.

To ensure proper operation using the temperature sensor, applications must accommodate the parameters in the temperature sensor definitions table.


Table 59: Temperature Sensor Definitions and Operating Conditions

Parameter	Description	Symbol	Min/Max	Value	Unit
System temperature gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C	TempGradient	MAX	System-dependent	°C/s
MR4 READ interval	Time period between MR4 READs from the system	ReadInterval	MAX	System-dependent	ms
Temperature sensor interval	Maximum delay between internal updates of MR4	^t TSI	MAX	32	ms
System response delay	Maximum response time from an MR4 READ to the system response	SysRespDelay	MAX	System-dependent	ms
Device temperature margin	Margin above maximum temperature to support controller response	TempMargin	MAX	2	°C

The mobile LPDDR2 device accommodates the temperature margin between the point at which the device temperature enters the extended temperature range and the point at which the controller reconfigures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system according to the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + {}^t\text{TSI} + \text{SysRespDelay}) \leq 2^\circ\text{C}$$

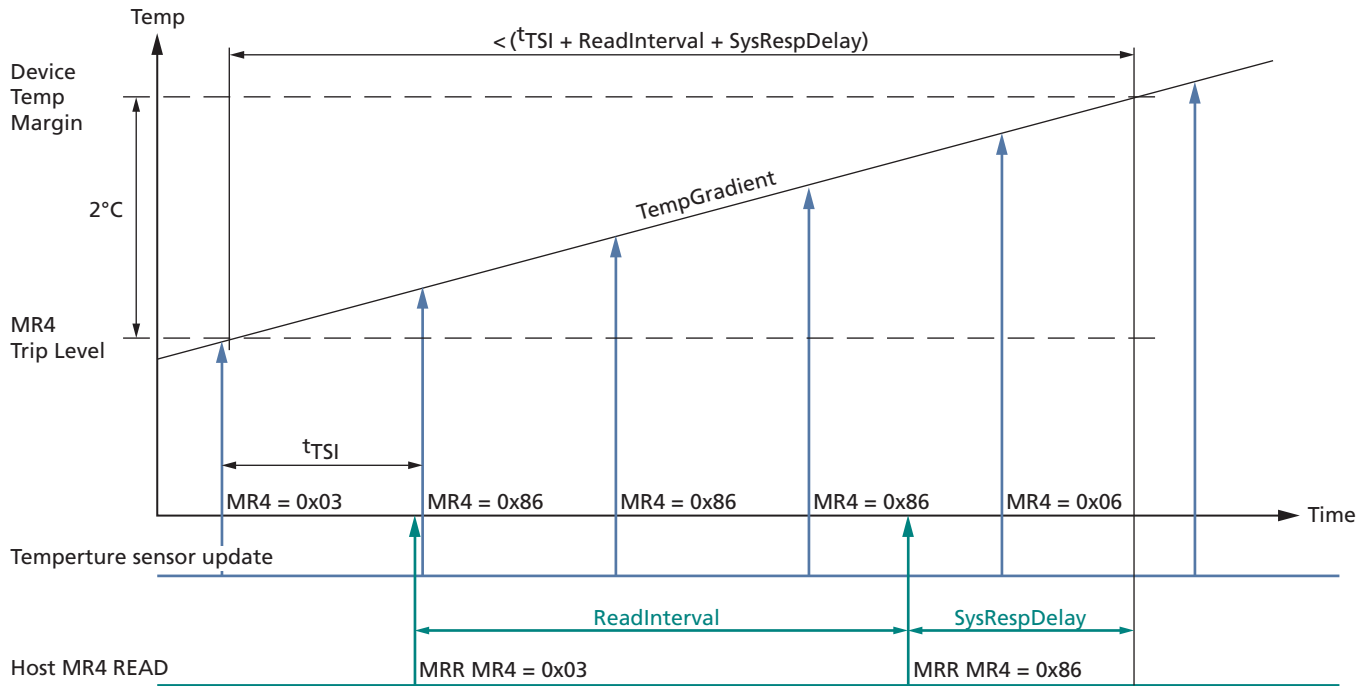
For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:

$$\frac{10^\circ\text{C}}{\text{s}} \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^\circ\text{C}$$

In this case, ReadInterval must not exceed 167ms.



Figure 54: Temperature Sensor Timing



DQ Calibration

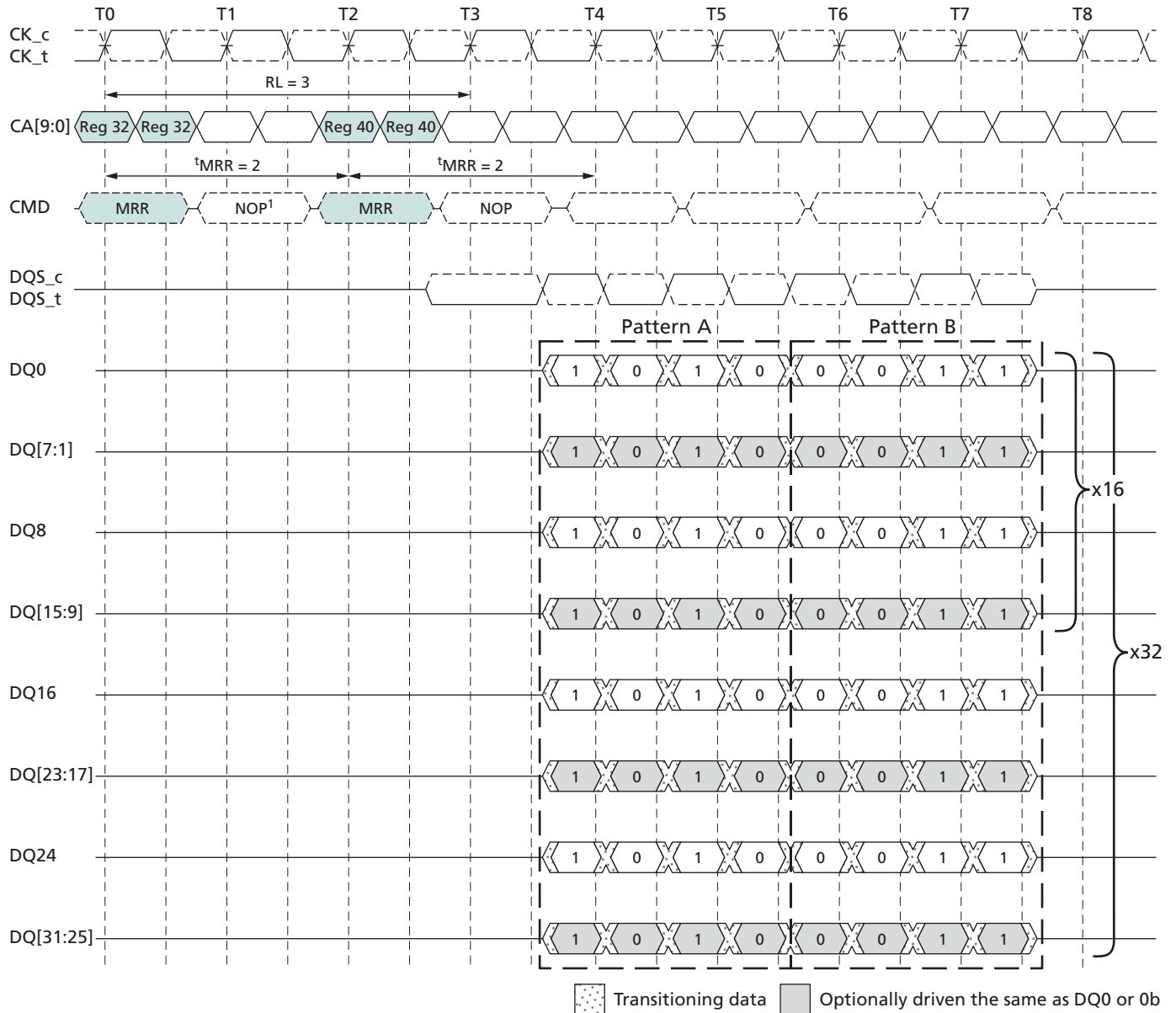
The mobile LPDDR2 device features a DQ calibration function that outputs one of two predefined system timing calibration patterns. For a x16 device, pattern A (MRR to MRR32), and pattern B (MRR to MRR40), will return the specified pattern on DQ0 and DQ8; a x32 device returns the specified pattern on DQ0, DQ8, DQ16, and DQ24.

For a x16 device, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For a x32 device, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.



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MODE REGISTER READ

Figure 55: MR32 and MR40 DQ Calibration Timing – RL = 3, $t_{MRR} = 2$



- Notes:
1. The MRR command has a burst length of four.
 2. The MRR operation must not be interrupted.
 3. A MRR to MR32 and MR40 drives valid data on DQ[0] during the entire burst. For a x16 device, DQ[8] drives the same information as DQ[0] during the burst. For a x32 device, DQ[8], DQ[16], and DQ[24] drive the same information as DQ[0] during the burst.
 4. For a x16 device, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0], or they may drive 0b during the burst. For a x32 device, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0], or they may drive 0b during the burst.
 5. The MODE REGISTER command period is t_{MRR} . No command (other than NOP) is allowed during this period.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP MODE REGISTER WRITE Command

Table 60: Data Calibration Pattern Description

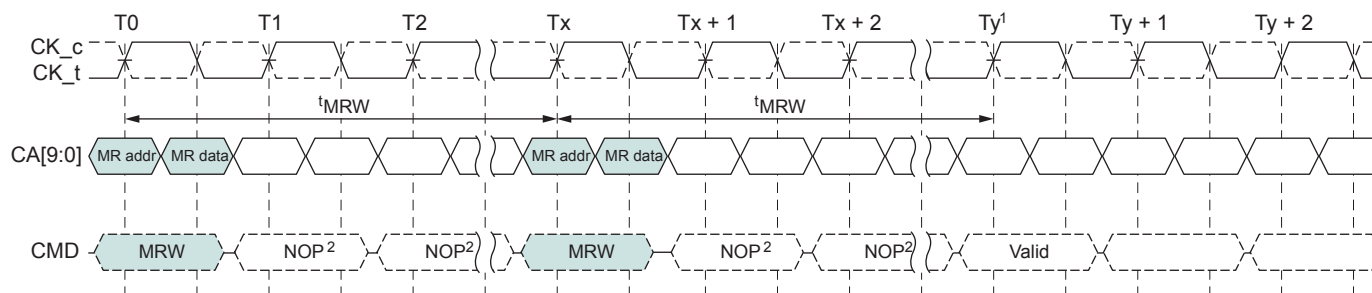
Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Description
Pattern A	MR32	1	0	1	0	Reads to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	Reads to MR40 return DQ calibration pattern B

MODE REGISTER WRITE Command

The MODE REGISTER WRITE (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f–CA0f, CA9r–CA4r. The data to be written to the mode register is contained in CA9f–CA2f. The MRW command period is defined by t_{MRW} . A MRW command to read-only registers has no impact on the functionality of the device.

MRW can be issued only when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE ALL command.

Figure 56: MODE REGISTER WRITE Timing – RL = 3, $t_{MRW} = 5$



- Notes: 1. At time T_y , the device is in the idle state.
2. Only the NOP command is supported during t_{MRW} .

Table 61: Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
	MRW (RESET)	Resetting, device auto initialization	All banks idle
Bank(s) active	MRR	Reading mode register, bank(s) active	Bank(s) active
	MRW	Not allowed	Not allowed
	MRW (RESET)	Not allowed	Not allowed

MRW RESET Command

The MRW RESET command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence (see step 2. of the RESET Command



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP MODE REGISTER WRITE Command

under Voltage Ramp and Initialization Sequence). The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during t_{INIT4} . After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command has completed. For MRW RESET timing, see Voltage Ramp and Initialization Sequence.

MRW ZQ Calibration Commands

The MRW command is used to initiate a ZQ calibration command that calibrates output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration. To achieve tighter tolerances, proper ZQ calibration must be performed.

There are four ZQ calibration commands and related timings: t_{ZQINIT} , $t_{ZQRESET}$, t_{ZQCL} , and t_{ZQCS} . t_{ZQINIT} is used for initialization calibration; $t_{ZQRESET}$ is used for resetting ZQ to the default output impedance; t_{ZQCL} is used for long calibration(s); and t_{ZQCS} is used for short calibration(s). See the MR10 Calibration (MA[7:0] = 0Ah) table for ZQ calibration command code definitions.

ZQINIT must be performed for LPDDR2 devices. ZQINIT provides an output impedance accuracy of $\pm 15\%$. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of $\pm 15\%$. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

ZQRESET resets the output impedance calibration to a default accuracy of $\pm 30\%$ across process, voltage, and temperature. This command is used to ensure output impedance accuracy to $\pm 30\%$ when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within t_{ZQCS} for all speed bins if maximum sensitivities are met as specified in Output Driver Sensitivity Definition and Output Driver Temperature and Voltage Sensitivity. The appropriate interval between ZQCS commands can be determined using these tables and system-specific parameters.

Mobile LPDDR2 devices are subject to temperature drift rate ($T_{driftrate}$) and voltage drift rate ($V_{driftrate}$) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQ_{correction}}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

Where $T_{sens} = \text{MAX}(dR_{ONdT})$ and $V_{sens} = \text{MAX}(dR_{ONdV})$ define temperature and voltage sensitivities.

For example, if $T_{sens} = 0.75\%/^{\circ}\text{C}$, $V_{sens} = 0.20\%/mV$, $T_{driftrate} = 1^{\circ}\text{C}/\text{sec}$, and $V_{driftrate} = 15\text{ mV}/\text{sec}$, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged.

No other activities can be performed on the data bus during calibration periods

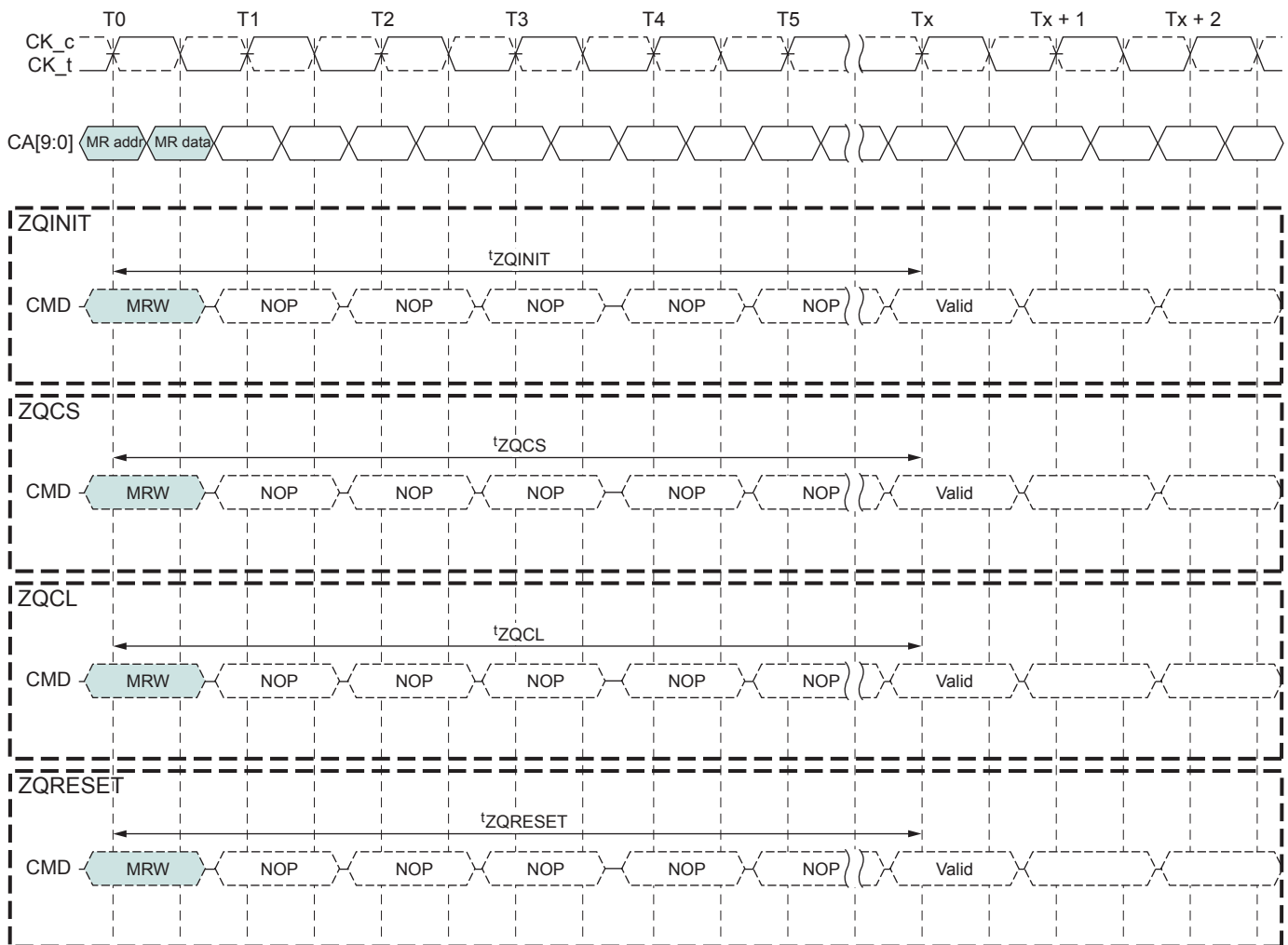


8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP MODE REGISTER WRITE Command

(t_{ZQINIT} , t_{ZQCL} , or t_{ZQCS}). The quiet time on the data bus helps to calibrate output impedance accurately. There is no required quiet time after the ZQRESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.

In systems sharing a ZQ resistor between devices, the controller must prevent t_{ZQINIT} , t_{ZQCS} , and t_{ZQCL} overlap between the devices. ZQRESET overlap is acceptable. If the ZQ resistor is absent from the system, ZQ must be connected to V_{DDQ} . In this situation, the device must ignore ZQ calibration commands and the device will use the default calibration settings.

Figure 57: ZQ Timings



- Notes: 1. Only the NOP command is supported during ZQ calibrations
 t_{ZQINIT} : ZQ calibration initialization period
 t_{ZQCS} : ZQ calibration short period
 t_{ZQCL} : ZQ calibration long period
 $t_{ZQRESET}$: ZQ calibration reset period



2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm ($\pm 1\%$ tolerance) external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see the Input/Output Capacitance table).

Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS_n is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operation such as ACTIVATE, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down I_{DD} specification will not be applied until such operations are complete.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, and CKE. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until t_{CKE} is satisfied. V_{REFCA} must be maintained at a valid level during power-down.

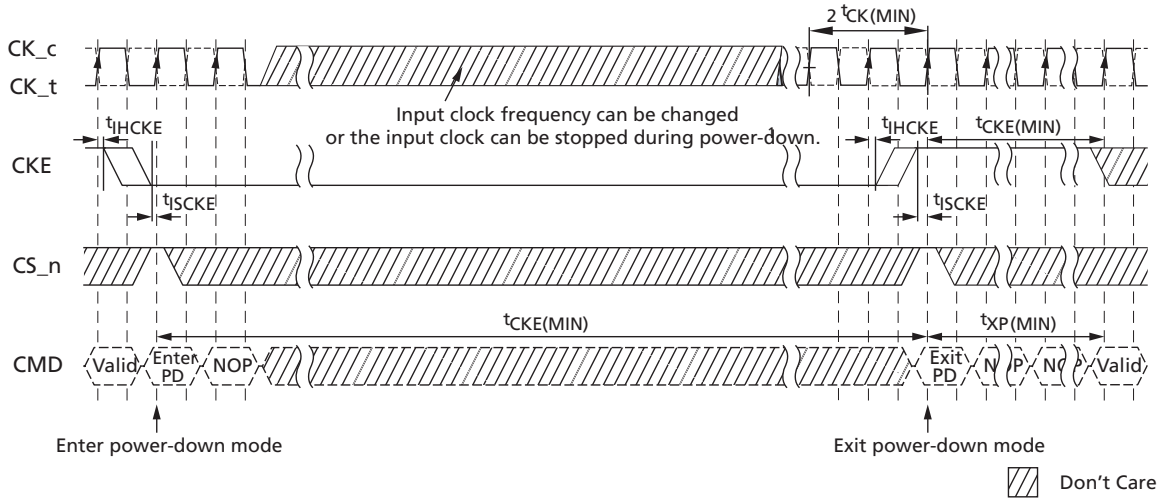
V_{DDQ} can be turned off during power-down. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting power-down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see AC and DC Operating Conditions).

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is limited only by the refresh requirements outlined in REFRESH Command.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until t_{CKE} is satisfied. A valid, executable command can be applied with power-down exit latency t_{XP} after CKE goes HIGH. Power-down exit latency is defined in the AC Timing section.



Figure 58: Power-Down Entry and Exit Timing



Note: 1. Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of two stable clocks complete.

Figure 59: CKE Intensive Environment

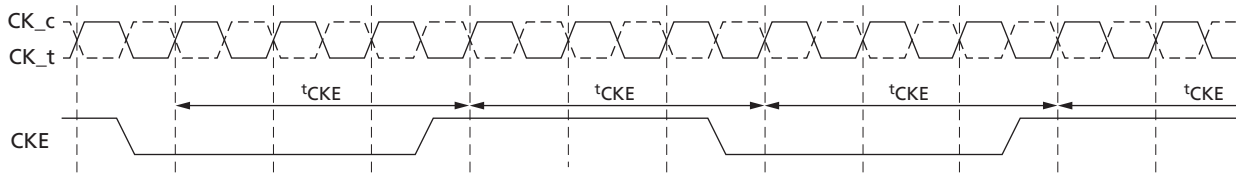
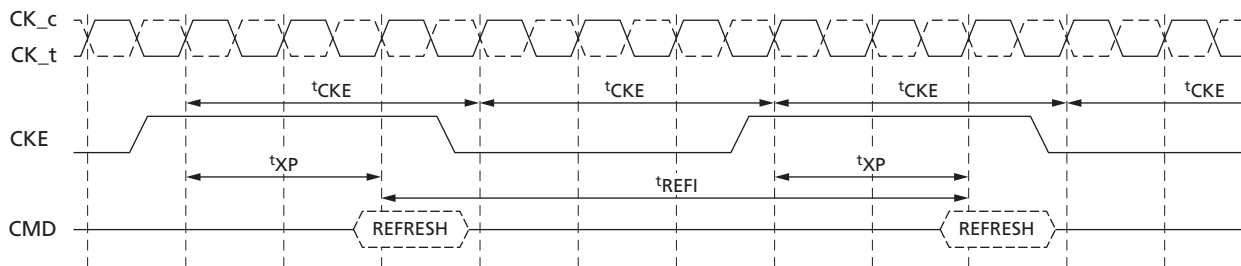


Figure 60: REFRESH-to-REFRESH Timing in CKE Intensive Environments

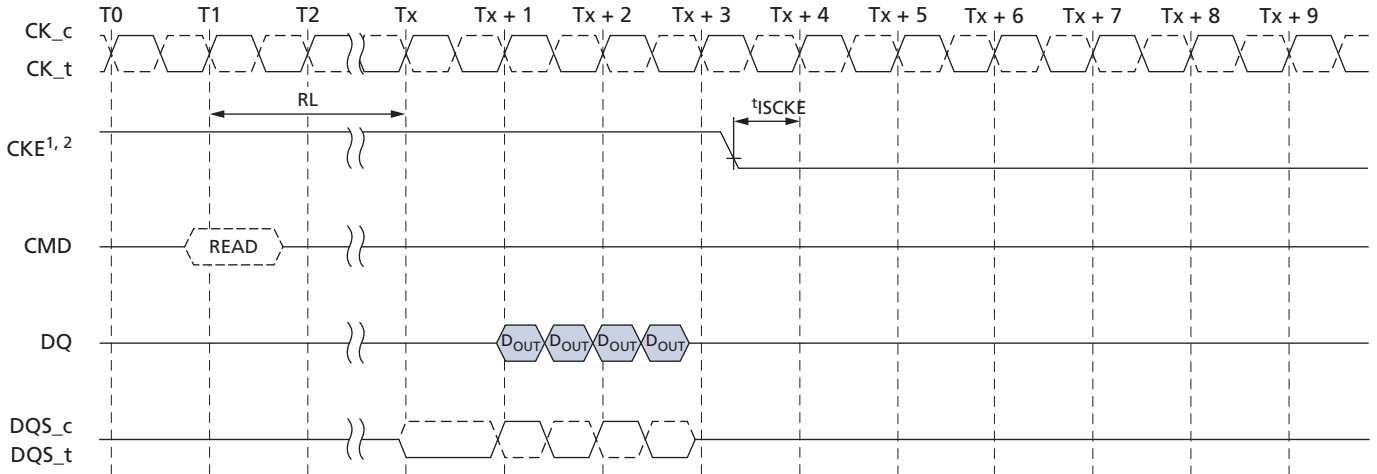


Note: 1. The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

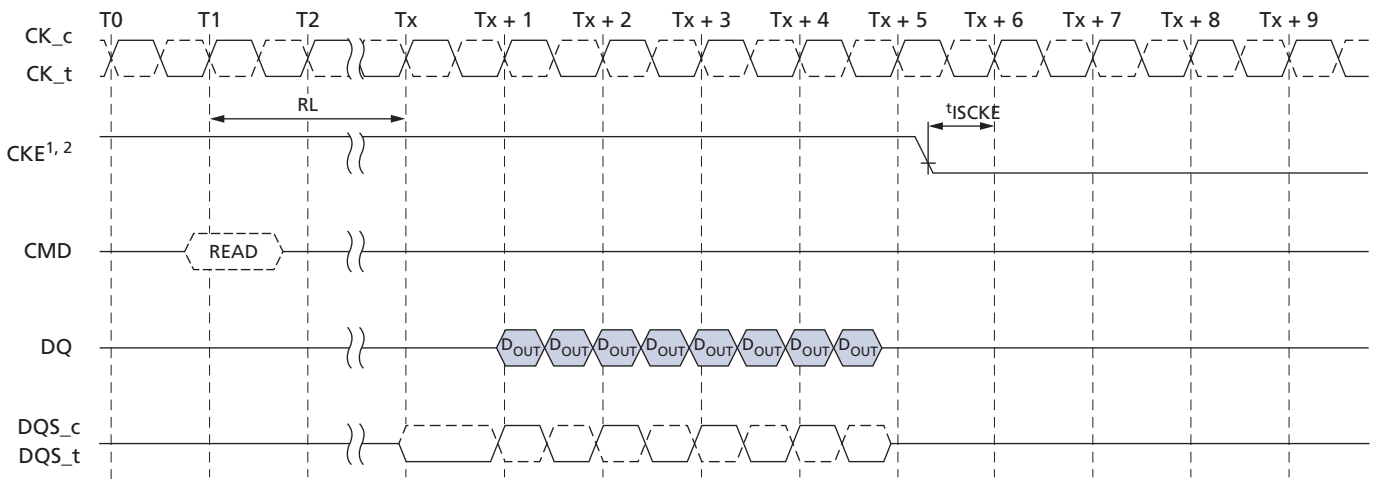


Figure 61: READ to Power-Down Entry

BL = 4



BL = 8

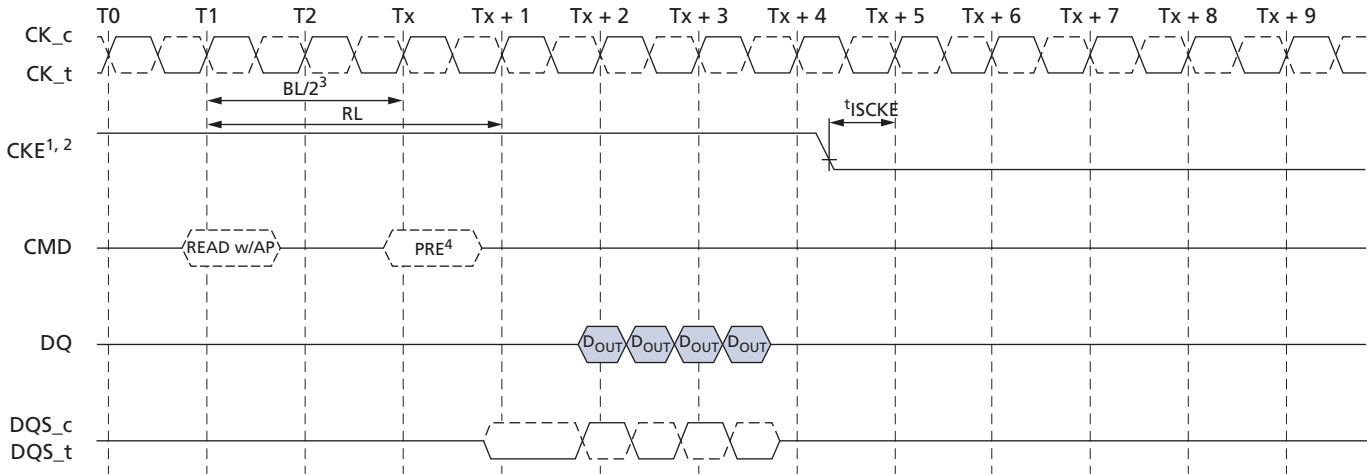


- Notes:
1. CKE must be held HIGH until the end of the burst operation.
 2. CKE can be registered LOW at $(RL + RU(t_{DQSCK}(MAX)/t_{CK}) + BL/2 + 1)$ clock cycles after the clock on which the READ command is registered.

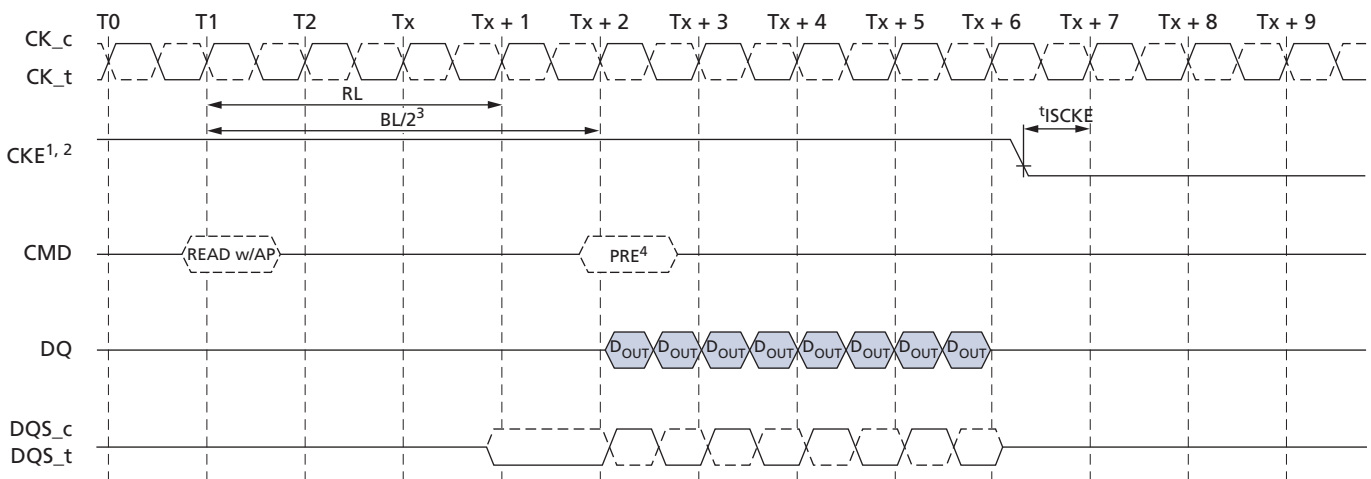


Figure 62: READ with Auto Precharge to Power-Down Entry

BL = 4



BL = 8

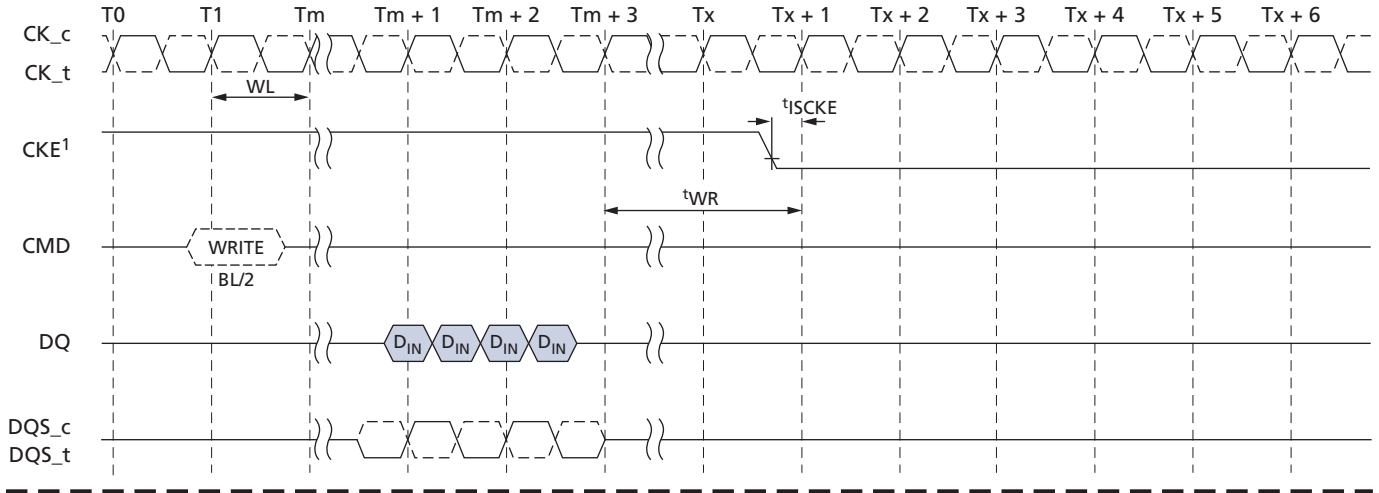


- Notes:
1. CKE must be held HIGH until the end of the burst operation.
 2. CKE can be registered LOW at $(RL + RU(t_{DQSCK}/t_{CK}) + BL/2 + 1)$ clock cycles after the clock on which the READ command is registered.
 3. $BL/2$ with $t_{RTP} = 7.5\text{ns}$ and $t_{RAS}(\text{MIN})$ is satisfied.
 4. Start internal PRECHARGE.

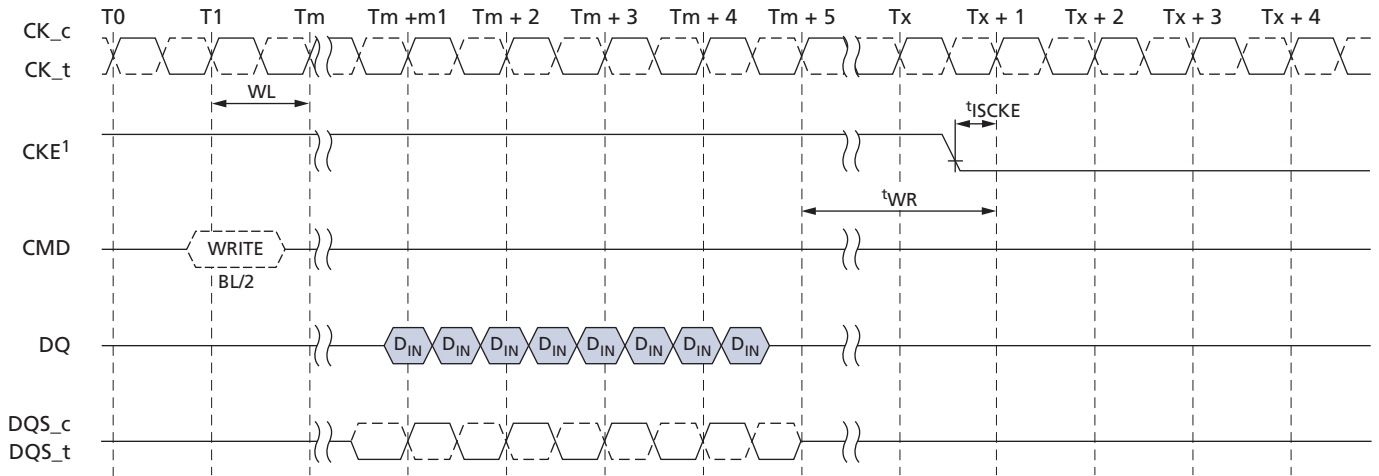


Figure 63: WRITE to Power-Down Entry

BL = 4



BL = 8

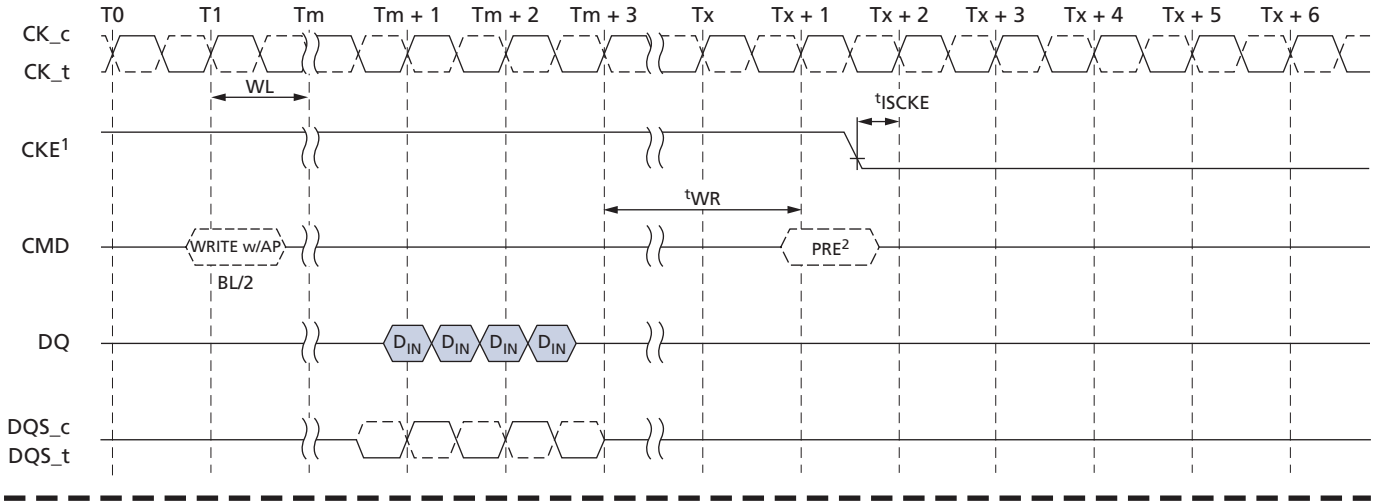


Note: 1. CKE can be registered LOW at $(WL + 1 + BL/2 + RU(tWR/tCK))$ clock cycles after the clock on which the WRITE command is registered.

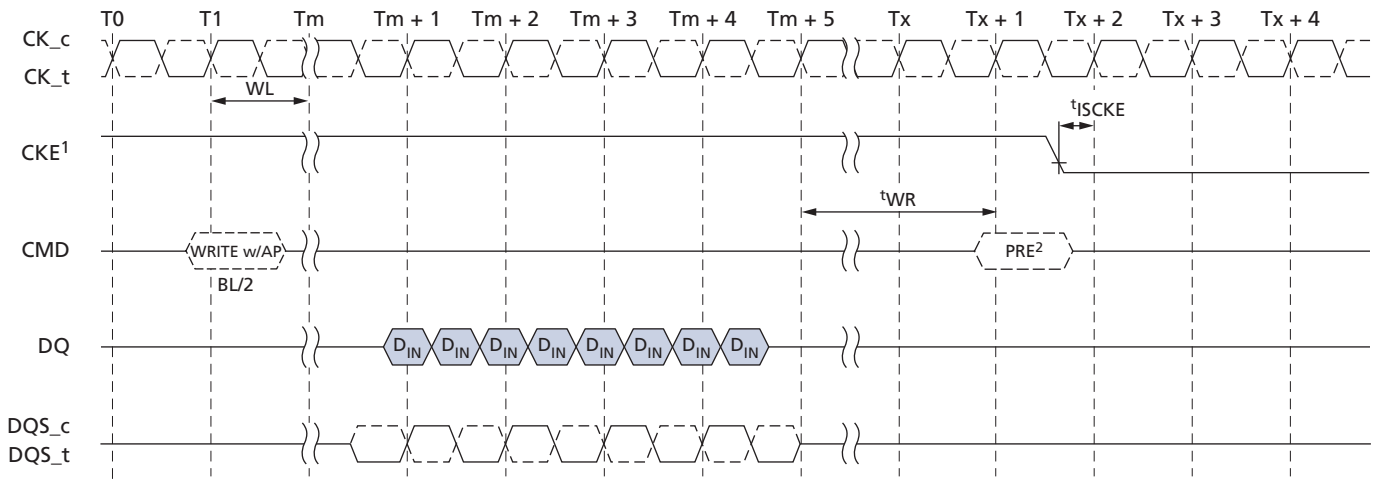


Figure 64: WRITE with Auto Precharge to Power-Down Entry

BL = 4



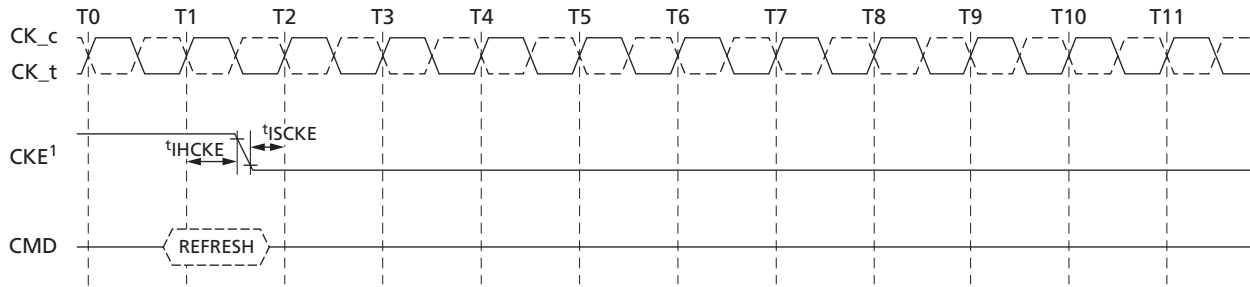
BL = 8



- Notes:
1. CKE can be registered LOW at $(WL + 1 + BL/2 + RU(tWR/tCK + 1))$ clock cycles after the WRITE command is registered.
 2. Start internal PRECHARGE.

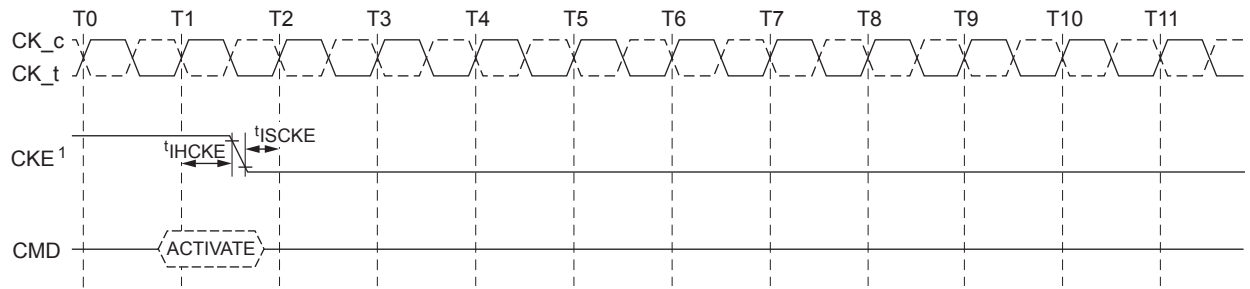


Figure 65: REFRESH Command to Power-Down Entry



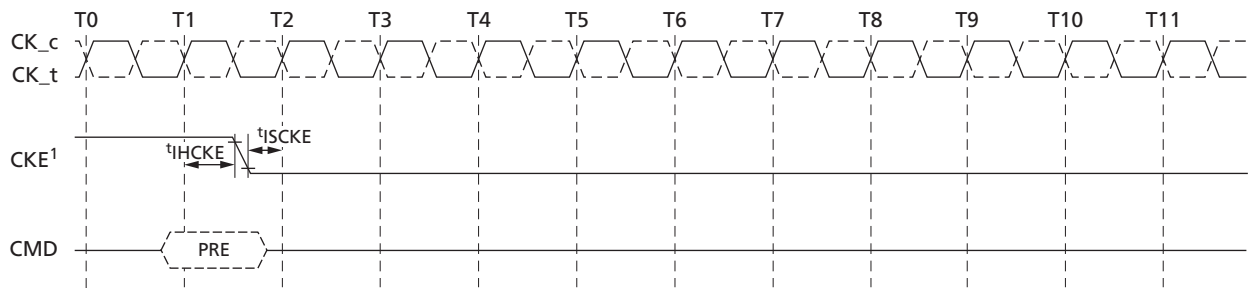
Note: 1. CKE can go LOW t_{IHCKE} after the clock on which the REFRESH command is registered.

Figure 66: ACTIVATE Command to Power-Down Entry



Note: 1. CKE can go LOW at t_{IHCKE} after the clock on which the ACTIVATE command is registered.

Figure 67: PRECHARGE Command to Power-Down Entry

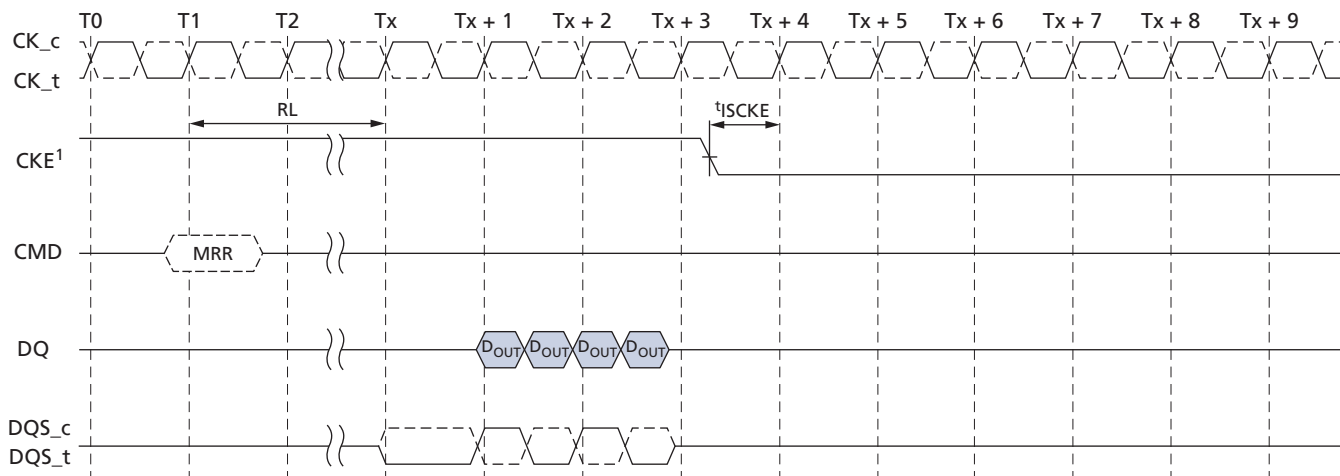


Note: 1. CKE can go LOW t_{IHCKE} after the clock on which the PRECHARGE command is registered.



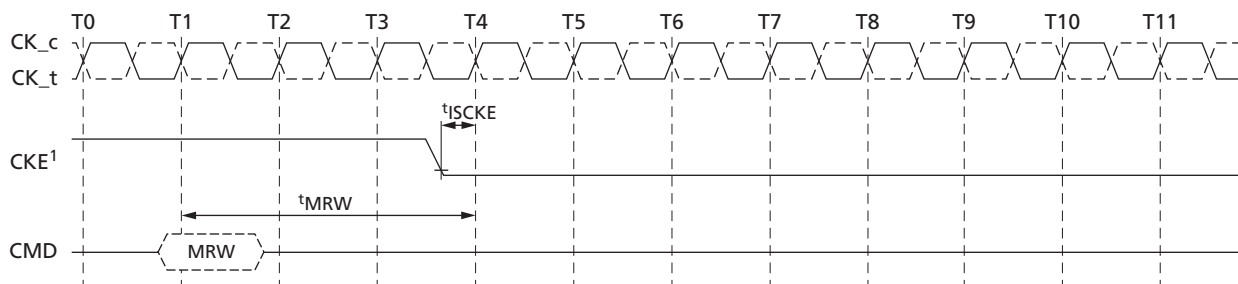
8Gb: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Deep Power-Down

Figure 68: MRR Command to Power-Down Entry



Note: 1. CKE can be registered LOW at $(RL + RU(t_{DQSC}/t_{CK}) + BL/2 + 1)$ clock cycles after the clock on which the MRR command is registered.

Figure 69: MRW Command to Power-Down Entry



Note: 1. CKE can be registered LOW t_{MRW} after the clock on which the MRW command is registered.

Deep Power-Down

Deep power-down (DPD) is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. The NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR or MRW operations are in progress. CKE can go LOW while other operations such as ACTIVATE, auto precharge, PRECHARGE, or REFRESH are in progress; however, deep power-down I_{DD} specifications will not be applied until those operations complete. The contents of the array will be lost upon entering DPD mode.

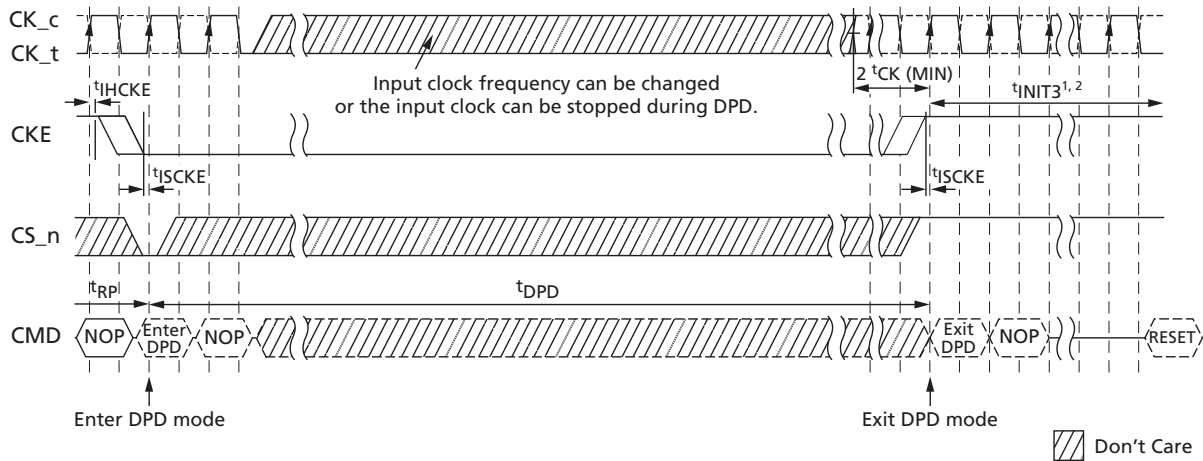
In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. V_{REFDQ} can be at any level between 0 and V_{DDQ}, and V_{REFCA} can be at any level between 0 and V_{DD2} during DPD. All power supplies (including V_{REF}) must be within the specified limits prior to exiting DPD (see AC and DC Operating Conditions).



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Input Clock Frequency Changes and Stop Events

To exit DPD, CKE must be HIGH, t_{ISCKE} must be complete, and the clock must be stable. To resume operation, the device must be fully reinitialized using the power-up initialization sequence.

Figure 70: Deep Power-Down Entry and Exit Timing



- Notes:
1. The initialization sequence can start at any time after $T_x + 1$.
 2. t_{INIT3} and $T_x + 1$ refer to timings in the initialization sequence. For details, see Mode Register Definition.

Input Clock Frequency Changes and Stop Events

Input Clock Frequency Changes and Clock Stop with CKE LOW

During CKE LOW, the mobile LPDDR2 device supports input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions, t_{RCD} and t_{RP} , have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of two clock cycles after CKE goes LOW
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of two clock cycles prior to CKE going HIGH

For input clock frequency changes, $t_{CK(MIN)}$ and $t_{CK(MAX)}$ must be met for each clock cycle.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK_t is held LOW and CK_c is held HIGH.



Input Clock Frequency Changes and Clock Stop with CKE HIGH

During CKE HIGH, the LPDDR2 device supports input clock frequency changes and clock stop under the following conditions:

- REFRESH requirements are met
- Any ACTIVATE, READ, WRITE, PRECHARGE, MRW, or MRR commands must have completed, including any associated data bursts, prior to changing the frequency
- Related timing conditions, t_{RCD} , t_{WR} , t_{RP} , t_{MRW} , and t_{MRR} , etc., are met
- CS_n must be held HIGH
- Only REFab or REFpb commands can be in process

The device is ready for normal operation after the clock satisfies $t_{CH(ABS)}$ and $t_{CL(ABS)}$ for a minimum of $2 \times t_{CK} + t_{XP}$.

For input clock frequency changes, $t_{CK(MIN)}$ and $t_{CK(MAX)}$ must be met for each clock cycle.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK_t is held LOW and CK_c is held HIGH.

NO OPERATION Command

The NO OPERATION (NOP) command prevents the device from registering any unwanted commands issued between operations. A NOP command can be issued only at clock cycle N when the CKE level is constant for clock cycle N-1 and clock cycle N. The NOP command has two possible encodings: CS_n HIGH at the clock rising edge N; and CS_n LOW with CA0, CA1, CA2 HIGH at the clock rising edge N.

The NOP command will not terminate a previous operation that is still in process, such as a READ burst or WRITE burst cycle.

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be powered down and then restarted using the specified initialization sequence before normal operation can continue.

Table 62: Command Truth Table

Notes 1–13 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE		CS _n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
	H	H	X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Truth Tables

Table 62: Command Truth Table (Continued)

Notes 1–13 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE		CS _n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(n-1)	CK(n)												
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
	H	H	X	MA6	MA7	X								
REFRESH (per bank)	H	H	L	L	L	H	L	X						
	H	H	X	X										
REFRESH (all banks)	H	H	L	L	L	H	H	X						
	H	H	X	X										
Enter self refresh	H	L	L	L	L	H	X							
	X	L	X	X										
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	
	H	H	X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	
WRITE (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
READ (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
PRECHARGE (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	
	H	H	X	X										
BST	H	H	L	H	H	L	L	X						
	H	H	X	X										
Enter DPD	H	L	L	H	H	L	X							
	X	L	X	X										
NOP	H	H	L	H	H	H	X							
	H	H	X	X										
Maintain PD, SREF, DPD, (NOP)	L	L	L	H	H	H	X							
	L	L	X	X										
NOP	H	H	H	X										
	H	H	X	X										
Maintain PD, SREF, DPD, (NOP)	L	L	H	X										
	L	L	X	X										
Enter power-down	H	L	H	X										
	X	L	X	X										



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Truth Tables

Table 62: Command Truth Table (Continued)

Notes 1–13 apply to all parameters conditions

Command	Command Pins			CA Pins									CK Edge	
	CKE		CS _n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA9
	CK(n-1)	CK(n)												
Exit PD, SREF, DPD	L	H	H	X										
	X	H	X	X										

- Notes:
1. All commands are defined by the current state of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
 2. Bank addresses (BA) determine which bank will be operated upon.
 3. AP HIGH during a READ or WRITE command indicates that an auto precharge will occur to the bank associated with the READ or WRITE command.
 4. X indicates a "Don't Care" state, with a defined logic level, either HIGH (H) or LOW (L).
 5. Self refresh exit and DPD exit are asynchronous.
 6. V_{REF} must be between 0 and V_{DDQ} during self refresh and DPD operation.
 7. CA_{xr} refers to command/address bit "x" on the rising edge of clock.
 8. CA_{xf} refers to command/address bit "x" on the falling edge of clock.
 9. CS_n and CKE are sampled on the rising edge of the clock.
 10. Per-bank refresh is supported only in devices with eight banks.
 11. The least-significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.
 12. RFU needs to input "H" or "L" (but a defined logic level).
 13. AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is don't care.

Table 63: CKE Truth Table

Notes 1–5 apply to all parameters and conditions; L = LOW, H = HIGH, X = "Don't Care"

Current State	CKEn-1	CKEn	CS _n	Command n	Operation n	Next State	Notes
Active power-down	L	L	X	X	Maintain active power-down	Active power-down	
	L	H	H	NOP	Exit active power-down	Active	6, 7
Idle power-down	L	L	X	X	Maintain idle power-down	Idle power-down	
	L	H	H	NOP	Exit idle power-down	Idle	6, 7
Resetting idle power-down	L	L	X	X	Maintain resetting power-down	Resetting power-down	
	L	H	H	NOP	Exit resetting power-down	Idle or resetting	6, 7, 8
Deep power-down	L	L	X	X	Maintain deep power-down	Deep power-down	
	L	H	H	NOP	Exit deep power-down	Power-on	9
Self refresh	L	L	X	X	Maintain self refresh	Self refresh	
	L	H	H	NOP	Exit self refresh	Idle	10, 11
Bank(s) active	H	L	H	NOP	Enter active power-down	Active power-down	



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Truth Tables

Table 63: CKE Truth Table (Continued)

Notes 1–5 apply to all parameters and conditions; L = LOW, H = HIGH, X = “Don’t Care”

Current State	CKEn-1	CKEn	CS_n	Command n	Operation n	Next State	Notes	
All banks idle	H	L	H	NOP	Enter idle power-down	Idle power-down		
	H	L	L	Enter self refresh	Enter self refresh	Self refresh		
	H	L	L	DPD	Enter deep power-down	Deep power-down		
Resetting	H	L	H	NOP	Enter resetting power-down	Resetting power-down		
Other states	H	H	Refer to the command truth table					

- Notes:
1. Current state = the state of the device immediately prior to the clock rising edge n .
 2. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
 3. CKEn = the logic state of CKE at clock rising edge n ; CKEn-1 was the state of CKE at the previous clock edge.
 4. CS_n = the logic state of CS_n at the clock rising edge n .
 5. Command n = the command registered at clock edge n , and operation n is a result of command n .
 6. Power-down exit time (t^{XP}) must elapse before any command other than NOP is issued.
 7. The clock must toggle at least twice prior to the t^{XP} period.
 8. Upon exiting the resetting power-down state, the device will return to the idle state if t^{INIT5} has expired.
 9. The DPD exit procedure must be followed as described in Deep Power Down.
 10. Self refresh exit time (t^{XSR}) must elapse before any command other than NOP is issued.
 11. The clock must toggle at least twice prior to the t^{XSR} time.

Table 64: Current State Bank n to Command to Bank n Truth Table

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current state	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (per bank)	Begin to refresh	Refreshing (per bank)	6
	Refresh (all banks)	Begin to refresh	Refreshing (all banks)	7
	MRW	Load value to mode register	MR writing	7
	MRR	Read value from mode register	Idle, MR reading	
	RESET	Begin device auto initialization	Resetting	7, 8
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9, 10
Row active	READ	Select column and start read burst	Reading	
	WRITE	Select column and start write burst	Writing	
	MRR	Read value from mode register	Active MR reading	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9


Table 64: Current State Bank *n* to Command to Bank *n* Truth Table (Continued)

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Reading	READ	Select column and start new read burst	Reading	11, 12
	WRITE	Select column and start write burst	Writing	11, 12, 13
	BST	Read burst terminate	Active	14
Writing	WRITE	Select column and start new write burst	Writing	11, 12
	READ	Select column and start read burst	Reading	11, 12, 15
	BST	Write burst terminate	Active	14
Power-on	RESET	Begin device auto initialization	Resetting	7, 9
Resetting	MRR	Read value from mode register	Resetting MR reading	

- Notes:
- Values in this table apply when both $CKEn - 1$ and $CKEn$ are HIGH, and after t_{XSR} or t_{XP} has been met, if the previous state was power-down.
 - All states and sequences not shown are illegal or reserved.
 - Current state definitions:
 - Idle: The bank or banks have been precharged, and t_{RP} has been met.
 - Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts or accesses and no register accesses are in progress.
 - Reading: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
 - Writing: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
 - These states must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank must be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state and the definitions given here.
 - Precharge: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. After t_{RP} is met, the bank is in the idle state.
 - Row activate: Starts with registration of an ACTIVATE command and ends when t_{RCD} is met. After t_{RCD} is met, the bank is in the active state.
 - READ with AP enabled: Starts with registration of a READ command with auto precharge enabled and ends when t_{RP} is met. After t_{RP} is met, the bank is in the idle state.
 - WRITE with AP enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} is met. After t_{RP} is met, the bank is in the idle state.
 - These states must not be interrupted by any executable command. NOP commands must be applied to each rising clock edge during these states.
 - Refresh (per bank): Starts with registration of a REFRESH (per bank) command and ends when t_{RFCpb} is met. After t_{RFCpb} is met, the bank is in the idle state.
 - Refresh (all banks): Starts with registration of a REFRESH (all banks) command and ends when t_{RFCab} is met. After t_{RFCab} is met, the device is in the all banks idle state.
 - Idle MR reading: Starts with registration of the MRR command and ends when t_{MRR} is met. After t_{MRR} is met, the device is in the all banks idle state.



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Resetting MR reading: Starts with registration of the MRR command and ends when t^{MRR} is met. After t^{MRR} is met, the device is in the all banks idle state.

Active MR reading: Starts with registration of the MRR command and ends when t^{MRR} is met. After t^{MRR} is met, the bank is in the active state.

MR writing: Starts with registration of the MRW command and ends when t^{MRW} is met. After t^{MRW} is met, the device is in the all banks idle state.

Precharging all: Starts with registration of a PRECHARGE ALL command and ends when t^{RP} is met. After t^{RP} is met, the device is in the all banks idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. If a PRECHARGE command is issued to a bank in the idle state, t^{RP} still applies.
11. A command other than NOP should not be issued to the same bank while a burst READ or burst WRITE with auto precharge is enabled.
12. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
13. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.
14. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ/WRITE command, regardless of bank.
15. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

Table 65: Current State Bank n to Command to Bank m Truth Table

Notes 1–6 apply to all parameters and conditions

Current State of Bank n	Command to Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current state of bank m	
Idle	Any	Any command supported to bank m	–	7
Row activating, active, or pre-charging	ACTIVATE	Select and activate row in bank m	Active	8
	READ	Select column and start READ burst from bank m	Reading	9
	WRITE	Select column and start WRITE burst to bank m	Writing	9
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
	MRR	READ value from mode register	Idle MR reading or active MR reading	11, 12, 13
	BST	READ or WRITE burst terminates an on-going READ/WRITE from/to bank m	Active	7


Table 65: Current State Bank *n* to Command to Bank *m* Truth Table (Continued)

Notes 1–6 apply to all parameters and conditions

Current State of Bank <i>n</i>	Command to Bank <i>m</i>	Operation	Next State for Bank <i>m</i>	Notes
Reading (auto precharge disabled)	READ	Select column and start READ burst from bank <i>m</i>	Reading	9
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9, 14
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing (auto precharge disabled)	READ	Select column and start READ burst from bank <i>m</i>	Reading	9, 15
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Reading with auto precharge	READ	Select column and start READ burst from bank <i>m</i>	Reading	9, 16
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9, 14, 16
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing with auto precharge	READ	Select column and start READ burst from bank <i>m</i>	Reading	9, 15, 16
	WRITE	Select column and start WRITE burst to bank <i>m</i>	Writing	9, 16
	ACTIVATE	Select and activate row in bank <i>m</i>	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Power-on	RESET	Begin device auto initialization	Resetting	17, 18
Resetting	MRR	Read value from mode register	Resetting MR reading	

- Notes:
- This table applies when: the previous state was self refresh or power-down; after t_{XSR} or t_{XP} has been met; *and* both $CKEn - 1$ and $CKEn$ are HIGH.
 - All states and sequences not shown are illegal or reserved.
 - Current state definitions:
 - Idle: The bank has been precharged and t_{RP} has been met.
 - Active: A row in the bank has been activated, t_{RCD} has been met, no data bursts or accesses and no register accesses are in progress.
 - Read: A READ burst has been initiated with auto precharge disabled and the READ has not yet terminated or been terminated.
 - Write: A WRITE burst has been initiated with auto precharge disabled and the WRITE has not yet terminated or been terminated.
 - Refresh, self refresh, and MRW commands can be issued only when all banks are idle.



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5. A BST command cannot be issued to another bank; it applies only to the bank represented by the current state.
6. These states must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:

Idle MRR: Starts with registration of the MRR command and ends when t^{MRR} has been met. After t^{MRR} is met, the device is in the all banks idle state.

Reset MRR: Starts with registration of the MRR command and ends when t^{MRR} has been met. After t^{MRR} is met, the device is in the all banks idle state.

Active MRR: Starts with registration of the MRR command and ends when t^{MRR} has been met. After t^{MRR} is met, the bank is in the active state.

MRW: Starts with registration of the MRW command and ends when t^{MRW} has been met. After t^{MRW} is met, the device is in the all banks idle state.
7. BST is supported only if a READ or WRITE burst is ongoing.
8. t^{RRD} must be met between the ACTIVATE command to bank n and any subsequent ACTIVATE command to bank m .
9. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
10. This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.
11. MRR is supported in the row-activating state.
12. MRR is supported in the precharging state.
13. The next state for bank m depends on the current state of bank m (idle, row-activating, precharging, or active).
14. A WRITE command can be issued after the completion of the READ burst; otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. A READ command can be issued after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.
16. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided that the timing restrictions in the PRECHARGE and Auto Precharge Clarification table are met.
17. Not bank-specific; requires that all banks are idle and no bursts are in progress.
18. RESET command is achieved through MODE REGISTER WRITE command.

Table 66: DM Truth Table

Functional Name	DM	DQ	Notes
Write enable	L	Valid	1
Write inhibit	H	X	1

Note: 1. Used to mask write data, and is provided simultaneously with the corresponding input data.

Electrical Conditions

- All voltages are referenced to VSS (GND).
- Power-up and Initialization sequence must be executed before proper device operation is achieved.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Absolute Maximum Ratings

Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 67: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V _{DD1} supply voltage relative to V _{SS}	V _{DD1}	-0.4	+2.3	V	1
V _{DD2} supply voltage relative to V _{SS}	V _{DD2} (1.2V)	-0.4	+1.6	V	1
V _{DDQ} supply voltage relative to V _{SSQ}	V _{DDQ}	-0.4	+1.6	V	1, 3
Voltage on any ball relative to V _{SS}	V _{IN} , V _{OUT}	-0.4	+1.6	V	
Storage temperature	T _{STG}	-55	+125	°C	4

- Notes:
- See 1. Voltage Ramp under Power Up.
 - V_{REFCA} 0.6 ≤ V_{DD2}; however, V_{REFCA} may be ≥ V_{DD2} provided that V_{REFCA} ≤ 300mV.
 - V_{REFDQ} 0.6 ≤ V_{DDQ}; however, V_{REFDQ} may be ≥ V_{DDQ} provided that V_{REFDQ} ≤ 300mV.
 - Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JE5D51-2 standard.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Input/Output Capacitance

Input/Output Capacitance

Table 68: Input/Output Capacitance

Notes 1 and 2 apply to all parameters and conditions; $T_A = +25^\circ\text{C}$, $V_{DD1} = 1.70\text{V}$ to 1.95V , V_{DD2} , $V_{DDQ} = 1.14\text{V}$ to 1.30V

Parameter	Symbol	MIN	MAX	Unit	Notes
Input capacitance, CK_t and CK_c	C_{CK}	1.0	2.0	pF	
Input capacitance delta, CK_t and CK_c	C_{DCK}	0	0.2	pF	3
Input capacitance, all other LPDDR2 input only balls	C_I	1.0	2.0	pF	4
Input capacitance delta, all other LPDDR2 input only balls	C_{DI}	-0.4	0.4	pF	5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	C_{IO}	1.25	2.5	pF	6, 7
Input/output capacitance, DQS_t, DQS_c	C_{DDQS}	0	0.25	pF	7, 8
Input/output capacitance, DQ, DM	C_{DIO}	-0.5	0.5	pF	7, 9
Input/output capacitance, ZQ	C_{ZQ}	0	2.5	pF	

- Notes:
1. This parameter applies to die device only (does not include package capacitance).
 2. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with V_{DD1} , V_{DD2} , V_{DDQ} , V_{SS} , and V_{SSQ} applied; all other pins are left floating.
 3. Absolute value of $C_{CK_t} - C_{CK_c}$
 4. C_I applies to CS_n, CE, CA[9:0].
 5. $C_{DI} = C_I - 0.5 \times (C_{CK_t} + C_{CK_c})$.
 6. DM loading matches DQ and DQS.
 7. MR3 I/O configuration DS OP[3:0] = 0001B (34.3Ω typical).
 8. Absolute value of C_{DQS_t} and C_{DQS_c} .
 9. $C_{DIO} = C_{IO} - 0.5 \times (C_{DQS_t} + C_{DQS_c})$ in byte-lane.

AC and DC Operating Conditions

An operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 69: Recommended DC Operating Conditions

Symbol	LPDDR2-S4B			Power Supply	Unit
	Min	Typ	Max		
V_{DD1}^1	1.70	1.80	1.95	Core power 1	V
V_{DD2}	1.14	1.20	1.30	Core power 2	V
V_{DDQ}	1.14	1.20	1.30	I/O buffer power	V

Note: 1. V_{DD1} uses significantly less power than V_{DD2} .



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP AC and DC Logic Input Measurement Levels for Single-Ended Signals

Table 70: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current: For CA, CKE, CS_n, CK_t, CK_c; Any input $0V \leq V_{IN} \leq V_{DD2}$; (All other pins not under test = 0V)	I_L	-2	2	μA	1
V_{REF} supply leakage current: $V_{REFDQ} = V_{DDQ}/2$, or $V_{REFCA} = V_{DD2}/2$; (All other pins not under test = 0V)	I_{VREF}	-1	1	μA	2

- Notes:
- Although DM is for input only, the DM leakage must match the DQ and DQS_t/DQS_c output leakage specification.
 - The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

Table 71: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard (WT) temperature range	T_{CASE}^1	-30	+85	$^{\circ}C$
Wide temperature range		-30	+105	$^{\circ}C$

- Notes:
- Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JE5D51-2 standard.
 - Some applications require operation in the maximum case temperature range, between 85 $^{\circ}C$ and 105 $^{\circ}C$. For some LPDDR2 devices, derating may be necessary to operate in this range (see the MR4 Device Temperature (MA[7:0] = 04h) table).
 - Either the device operating temperature or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the T_{CASE} rating that applies for the operating temperature range. For example, T_{CASE} could be above 85 $^{\circ}C$ when the temperature sensor indicates a temperature of less than 85 $^{\circ}C$.

AC and DC Logic Input Measurement Levels for Single-Ended Signals

Table 72: Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHCA(AC)}$	AC input logic HIGH	$V_{REF} + 0.220$	Note 2	$V_{REF} + 0.300$	Note 2	V	1, 2
$V_{ILCA(AC)}$	AC input logic LOW	Note 2	$V_{REF} - 0.220$	Note 2	$V_{REF} - 0.300$	V	1, 2
$V_{IHCA(DC)}$	DC input logic HIGH	$V_{REF} + 0.130$	V_{DD2}	$V_{REF} + 0.200$	V_{DD2}	V	1
$V_{ILCA(DC)}$	DC input logic LOW	V_{SS}	$V_{REF} - 0.130$	V_{SS}	$V_{REF} - 0.200$	V	1
$V_{REFCA(DC)}$	Reference voltage for CA and CS_n inputs	$0.49 \times V_{DD2}$	$0.51 \times V_{DD2}$	$0.49 \times V_{DD2}$	$0.51 \times V_{DD2}$	V	3, 4

- Notes:
- For CA and CS_n input-only pins. $V_{REF} = V_{REFCA(DC)}$.
 - See Overshoot and Undershoot Definition.
 - The AC peak noise on V_{REFCA} could prevent V_{REFCA} from deviating more than $\pm 1\% V_{DD2}$ from $V_{REFCA(DC)}$ (for reference, approximately $\pm 12mV$).



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP AC and DC Logic Input Measurement Levels for Single-Ended Signals

4. For reference, approximately $V_{DD2}/2 \pm 12\text{mV}$.

Table 73: Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE input HIGH level	$0.8 \times V_{DD2}$	Note 1	V	1
V_{ILCKE}	CKE input LOW level	Note 1	$0.2 \times V_{DD2}$	V	1

Note: 1. See Overshoot and Undershoot Definition.

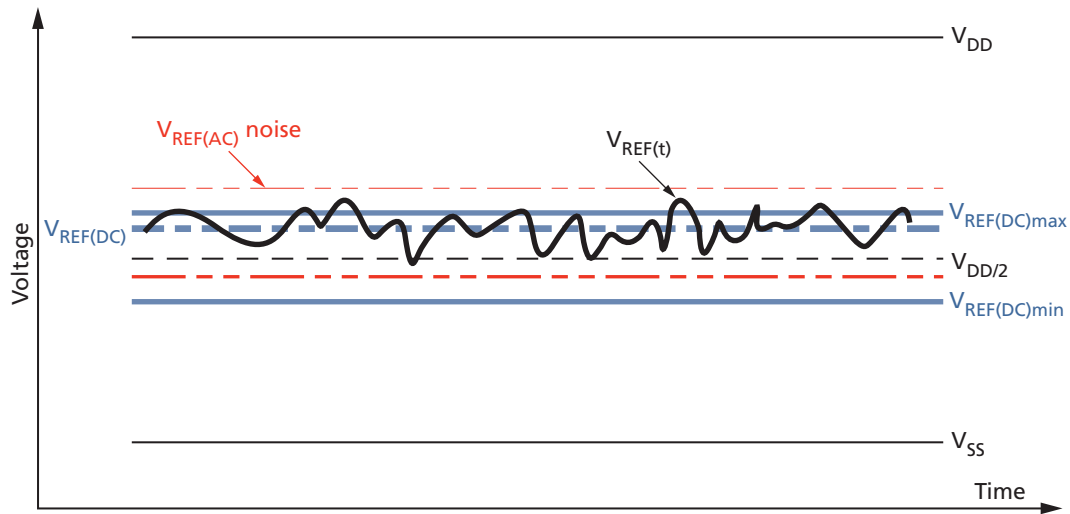
Table 74: Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHDQ(AC)}$	AC input logic HIGH	$V_{REF} + 0.220$	Note 2	$V_{REF} + 0.300$	Note 2	V	1, 2
$V_{ILDQ(AC)}$	AC input logic LOW	Note 2	$V_{REF} - 0.220$	Note 2	$V_{REF} - 0.300$	V	1, 2
$V_{IHDQ(DC)}$	DC input logic HIGH	$V_{REF} + 0.130$	V_{DDQ}	$V_{REF} + 0.200$	V_{DDQ}	V	1
$V_{ILDQ(DC)}$	DC input logic LOW	V_{SS}	$V_{REF} - 0.130$	V_{SS}	$V_{REF} - 0.200$	V	1
$V_{REFDQ(DC)}$	Reference voltage for DQ and DM inputs	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	3, 4

- Notes:
1. For DQ input-only pins. $V_{REF} = V_{REFDQ(DC)}$.
 2. See Overshoot and Undershoot Definition.
 3. The AC peak noise on V_{REFDQ} could prevent V_{REFDQ} from deviating more than $\pm 1\% V_{DDQ}$ from $V_{REFDQ(DC)}$ (for reference, approximately $\pm 12\text{mV}$).
 4. For reference, approximately $V_{DDQ}/2 \pm 12\text{mV}$.

V_{REF} Tolerances

The DC tolerance limits and AC noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrated below. This figure shows a valid reference voltage $V_{REF}(t)$ as a function of time. V_{DD} is used in place of V_{DD2} for V_{REFCA} , and V_{DDQ} for V_{REFDQ} . $V_{REF(DC)}$ is the linear average of $V_{REF}(t)$ over a very long period of time (for example, 1 second) and is specified as a fraction of the linear average of V_{DDQ} or V_{DD2} , also over a very long period of time (for example, 1 second). This average must meet the MIN/MAX requirements in the Single-Ended AC and DC Input Levels for CA and CS_n Inputs table. Additionally, $V_{REF}(t)$ can temporarily deviate from $V_{REF(DC)}$ by no more than $\pm 1\% V_{DD}$. $V_{REF}(t)$ cannot track noise on V_{DDQ} or V_{DD2} if doing so would force V_{REF} outside these specifications.


Figure 71: V_{REF} DC Tolerance and V_{REF} AC Noise Limits


The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{REF} .

V_{REF} DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When V_{REF} is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

- V_{REF} is maintained between $0.44 \times V_{DDQ}$ (or V_{DD2}) and $0.56 \times V_{DDQ}$ (or V_{DD2}), *and*
- the controller achieves the required single-ended AC and DC input levels from instantaneous V_{REF} (see the Single-Ended AC and DC Input Levels for CA and CS_n Inputs table).

System timing and voltage budgets must account for V_{REF} deviations outside this range.

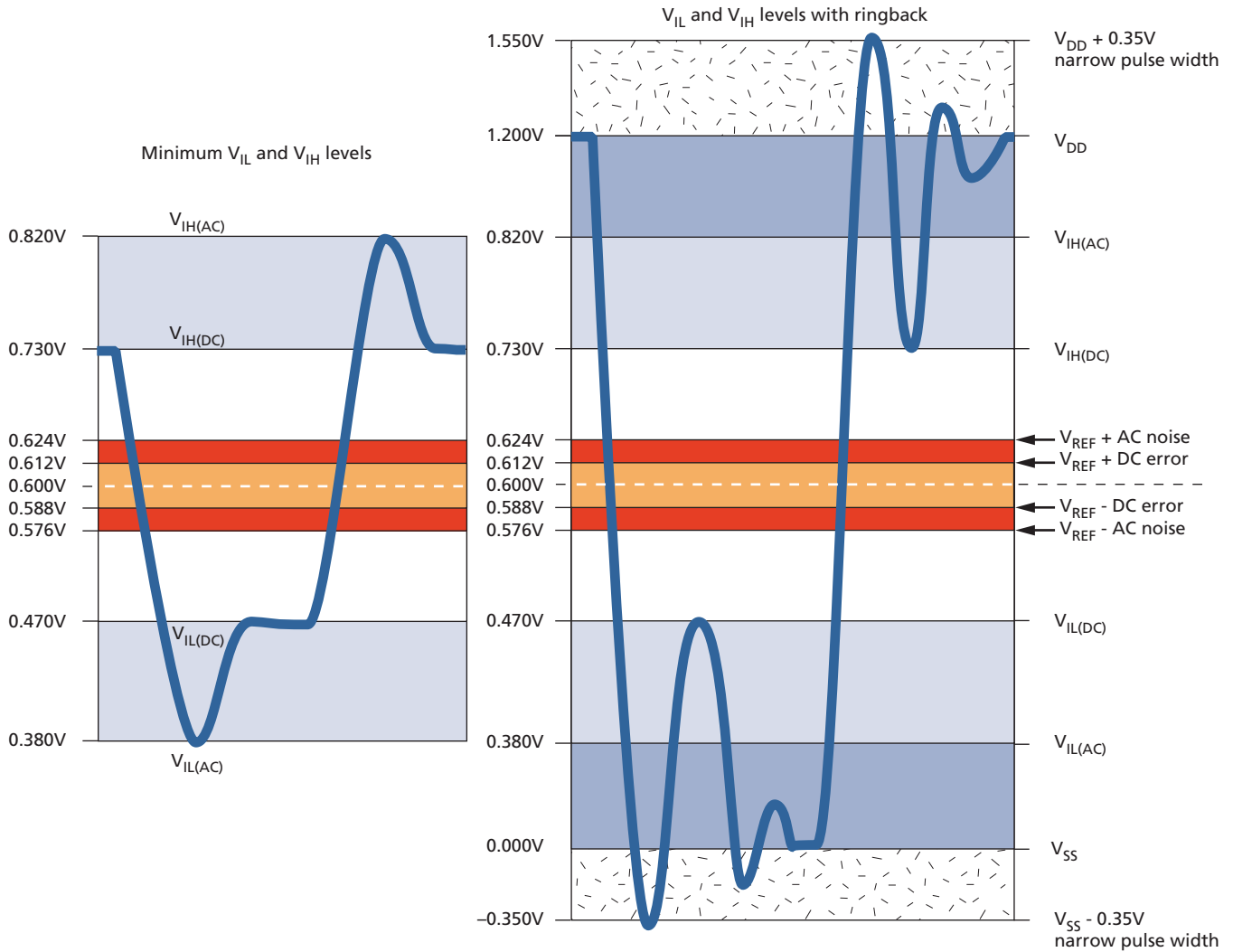
The setup/hold specification and derating values must include time and voltage associated with V_{REF} AC noise. Timing and voltage effects due to AC noise on V_{REF} up to the specified limit ($\pm 1\% V_{DD}$) are included in LPDDR2 timings and their associated deratings.



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Input Signal

Figure 72: LPDDR2-466 to LPDDR2-1066 Input Signal

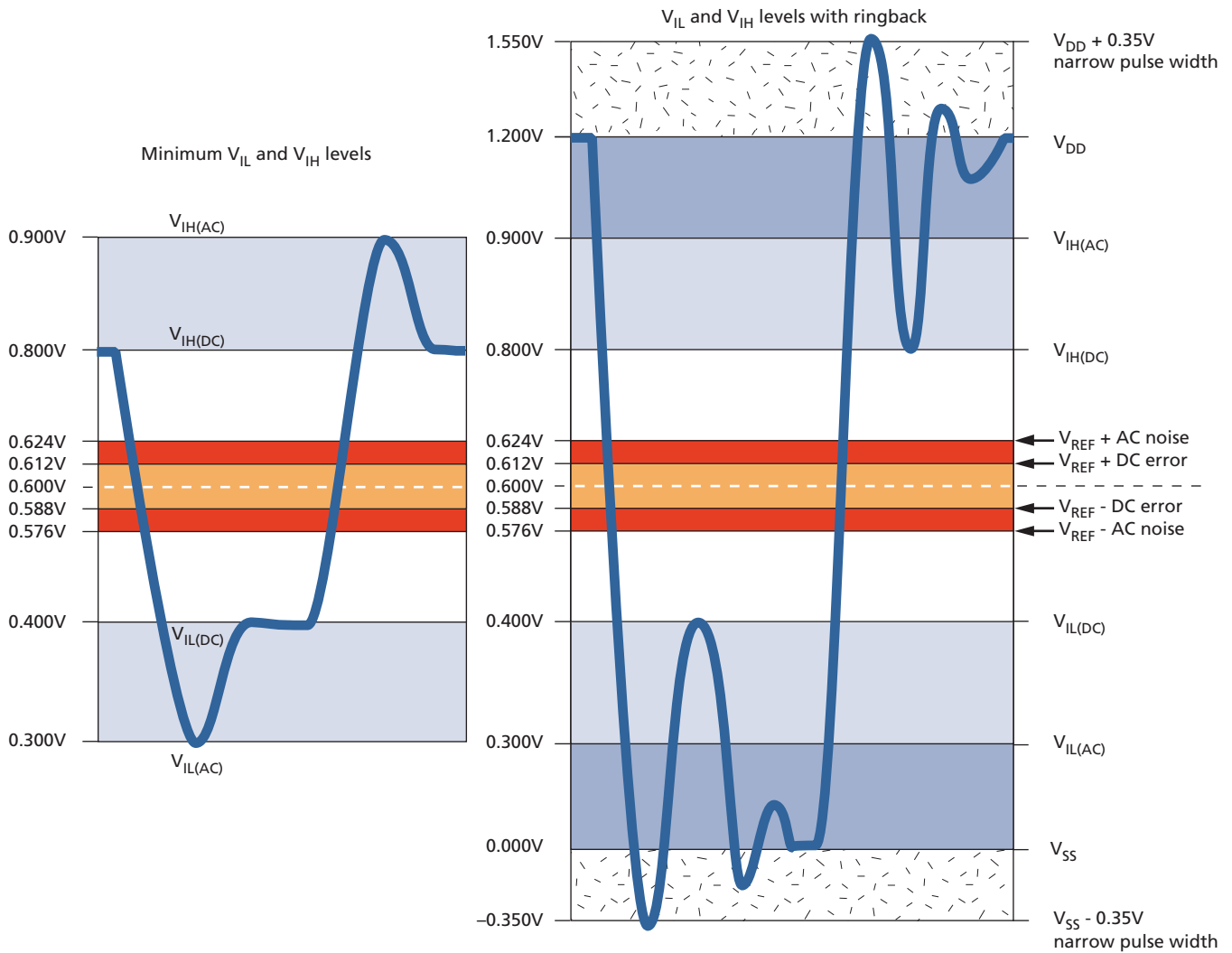


- Notes:
1. Numbers reflect typical values.
 2. For CA[9:0], CK_t, CK_c, and CS_n V_{DD} stands for V_{DD2} . For DQ, DM, DQS_t, and DQS_c, V_{DD} stands for V_{DDQ} .
 3. For CA[9:0], CK_t, CK_c, and CS_n are V_{SS} . For DQ, DM, DQS_t, and DQS_c, V_{SS} stands for V_{SSQ} .



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AC and DC Logic Input Measurement Levels for Single-Ended
Signals**

Figure 73: LPDDR2-200 to LPDDR2-400 Input Signal



- Notes:
1. Numbers reflect typical values.
 2. For CA[9:0], CK_t, CK_c, and CS_n V_{DD} stands for V_{DD2} . For DQ, DM, DQS_t, and DQS_c, V_{DD} stands for V_{DDQ} .
 3. For CA[9:0], CK_t, CK_c, and CS_n are V_{SS} . For DQ, DM, DQS_t, and DQS_c, V_{SS} stands for V_{SSQ} .



AC and DC Logic Input Measurement Levels for Differential Signals

Figure 74: Differential AC Swing Time and t_{DVAC}

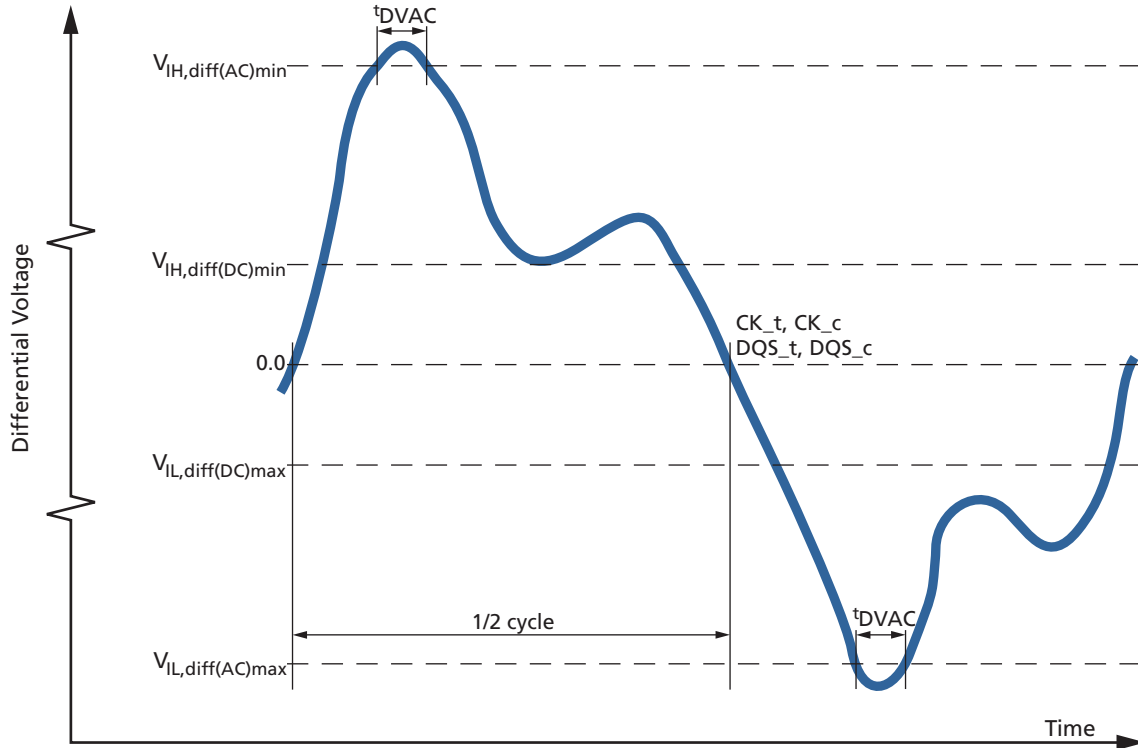


Table 75: Differential AC and DC Input Levels

For CK_t and CK_c, $V_{REF} = V_{REFCA(DC)}$; For DQS_t and DQS_c $V_{REF} = V_{REFDQ(DC)}$

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IH,diff(AC)}$	Differential input HIGH AC	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	V	2
$V_{IL,diff(AC)}$	Differential input LOW AC	Note 1	$2 \times (V_{IL(AC)} - V_{REF})$	Note 1	$2 \times (V_{IL(AC)} - V_{REF})$	V	2
$V_{IH,diff(DC)}$	Differential input HIGH	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	V	3
$V_{IL,diff(DC)}$	Differential input LOW	Note 1	$2 \times (V_{IL(DC)} - V_{REF})$	Note 1	$2 \times (V_{IL(DC)} - V_{REF})$	V	3

Notes: 1. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals and must comply with the specified limitations for overshoot and undershoot (see Overshoot and Undershoot Definitions).



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP AC and DC Logic Input Measurement Levels for Differential Signals

- For CK_t and CK_c, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA} ; for DQS_t and DQS_c, use $V_{IH}/V_{IL(AC)}$ of DQ and V_{REFDQ} . If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
- Used to define a differential signal slew rate. For CK_t - CK_c use $V_{IH}/V_{IL(dc)}$ of CA and V_{REFCA} ; for DQS_t - DQS_c, use $V_{IH}/V_{IL(dc)}$ of DQs and V_{REFDQ} ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

Table 76: CK_t/CK_c and DQS_t/DQS_c Time Requirements Before Ringback (t_{DVAC})

Slew Rate (V/ns)	t_{DVAC} (ps) at $V_{IH}/V_{ILdiff(AC)} = 440mV$	t_{DVAC} (ps) at $V_{IH}/V_{ILdiff(AC)} = 600mV$
	Min	Min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

Single-Ended Requirements for Differential Signals

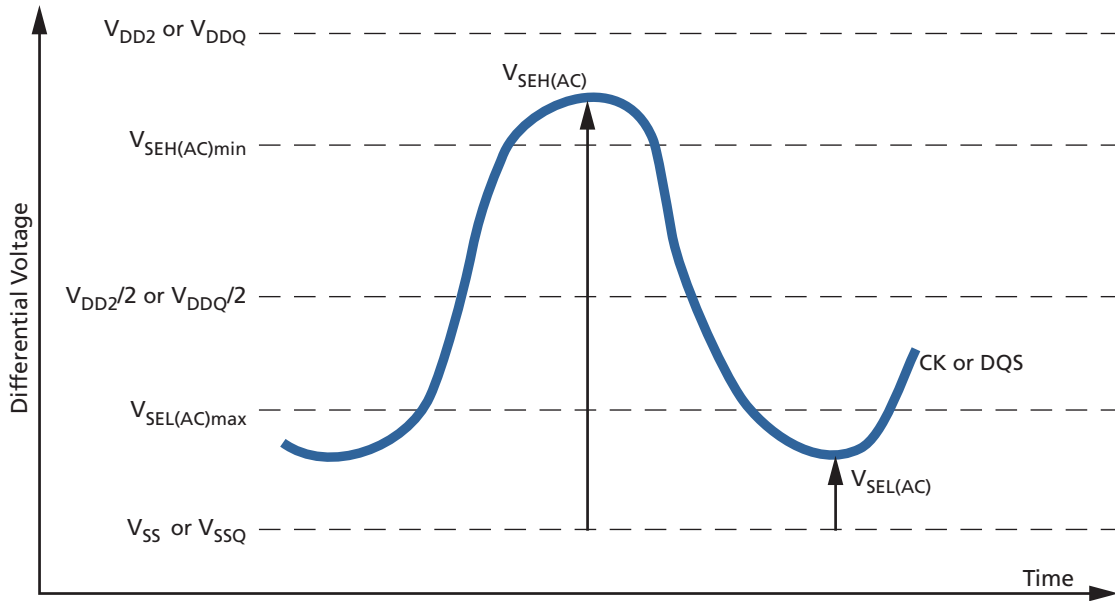
Each individual component of a differential signal (CK_t, CK_c, DQS_t, and DQS_c) must also comply with certain requirements for single-ended signals.

CK_t and CK_c must meet $V_{SEH(AC)min}/V_{SEL(AC)max}$ in every half cycle. DQS_t, DQS_c must meet $V_{SEH(AC)min}/V_{SEL(AC)max}$ in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed bin.



Figure 75: Single-Ended Requirements for Differential Signals



While CA and DQ signal requirements are referenced to V_{REF} , the single-ended components of differential signals also have a requirement with respect to $V_{DDQ}/2$ for DQS, and $V_{DD2}/2$ for CK.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach $V_{SEL(AC)max}$ or $V_{SEH(AC)min}$ has no bearing on timing. This requirement does, however, add a restriction on the common mode characteristics of these signals (see Single-Ended AC and DC Input Levels for CA and CS_n Inputs for CK_t/CK_c single-ended requirements, and Single-Ended AC and DC Input Levels for DQ and DM for DQ and DQM single-ended requirements).

Table 77: Single-Ended Levels for CK_t, CK_c, DQS_t, DQS_c

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	$(V_{DDQ}/2) + 0.220$	Note 1	$(V_{DDQ}/2) + 0.300$	Note 1	V	2, 3
	Single-ended HIGH level for CK_t, CK_c	$(V_{DD2}/2) + 0.220$	Note 1	$(V_{DD2}/2) + 0.300$	Note 1	V	2, 3
$V_{SEL(AC)}$	Single-ended LOW level for strobes	Note 1	$(V_{DDQ}/2) - 0.220$	Note 1	$(V_{DDQ}/2) + 0.300$	V	2, 3
	Single-ended LOW level for CK_t, CK_c	Note 1	$(V_{DD2}/2) - 0.220$	Note 1	$(V_{DD2}/2) + 0.300$	V	2, 3

Notes: 1. These values are not defined; however, the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c must be within the respective limits ($V_{IH(DC)max}/V_{IL(DC)min}$) for single-ended signals, and must comply with the



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP AC and DC Logic Input Measurement Levels for Differential Signals

specified limitations for overshoot and undershoot (see Overshoot and Undershoot Definition).

- For CK_t and CK_c, use $V_{SEH}/V_{SEL(AC)}$ of CA; for strobes (DQS[3:0]_t and DQS[3:0]_c), use $V_{IH}/V_{IL(AC)}$ of DQ.
- $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ} ; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA} . If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.

Differential Input Crosspoint Voltage

To ensure tight setup and hold times as well as output skew parameters with respect to clock and strobe, each crosspoint voltage of differential input signals (CK_t, CK_c, DQS_t, and DQS_c) must meet the specifications listed in the Single-Ended Levels for CK_t, CK_c, DQS_t, DQS_c table. The differential input crosspoint voltage (V_{IX}) is measured from the actual crosspoint of the true signal and its complement to the midlevel between V_{DD} and V_{SS} .

Figure 76: V_{IX} Definition

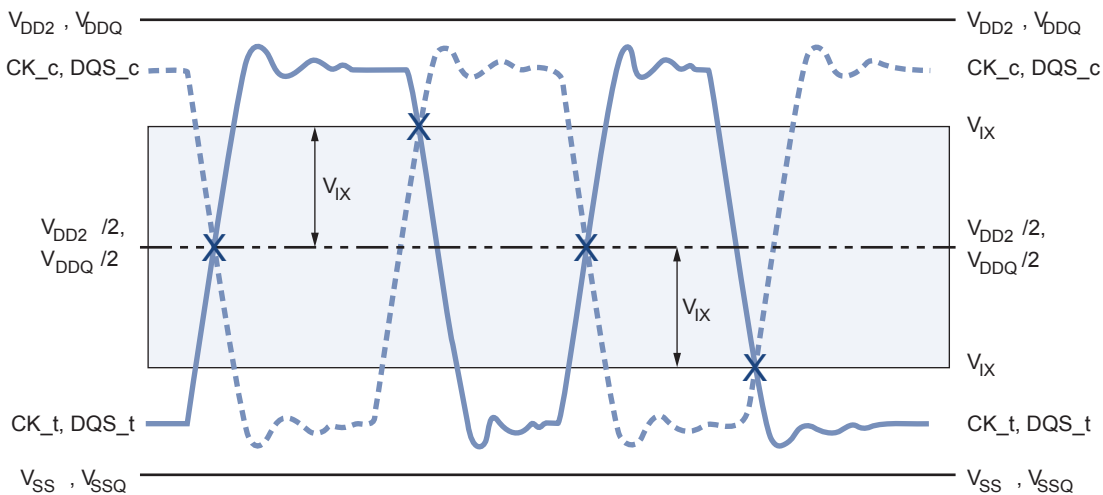


Table 78: Crosspoint Voltage for Differential Input Signals (CK_t, CK_c, DQS_t, DQS_c)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Notes
		Min	Max		
$V_{IXCA(AC)}$	Differential input crosspoint voltage relative to $V_{DD2}/2$ for CK_t and CK_c	-120	120	mV	1, 2
$V_{IXDQ(AC)}$	Differential input crosspoint voltage relative to $V_{DDQ}/2$ for DQS_t and DQS_c	-120	120	mV	1, 2

- Notes:
- The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{DD}$ of the transmitting device, and it is expected to track variations in V_{DD} . $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
 - For CK_t and CK_c, $V_{REF} = V_{REFCA(DC)}$. For DQS_t and DQS_c, $V_{REF} = V_{REFDQ(DC)}$.



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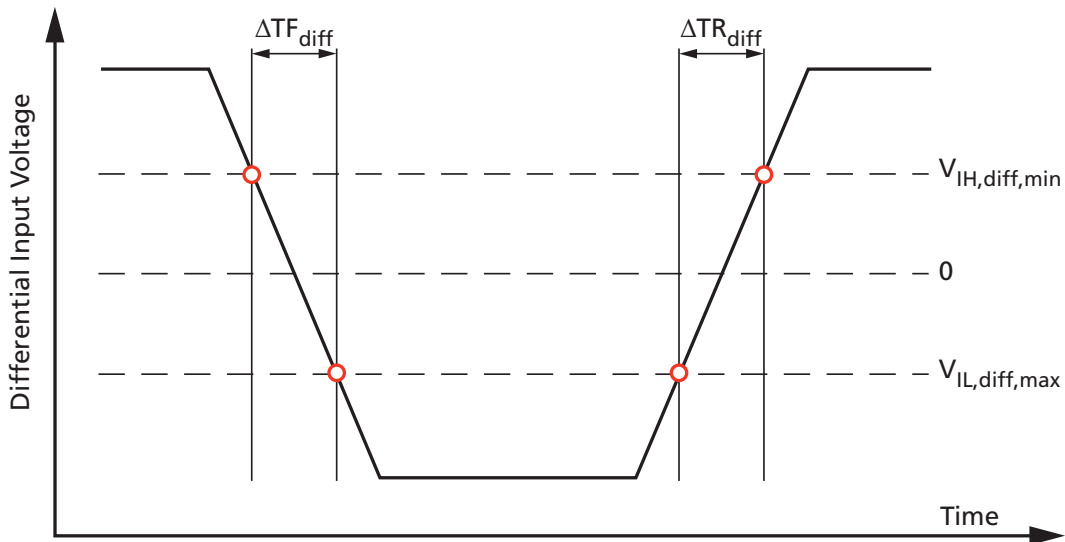
Input Slew Rate

Table 79: Differential Input Slew Rate Definition

Description	Measured ¹		Defined by
	From	To	
Differential input slew rate for rising edge (CK_t/CK_c and DQS_t/DQS_c)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK_t/CK_c and DQS_t/DQS_c)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TF_{diff}$

Note: 1. The differential signals (CK_t/CK_c and DQS_t/DQS_c) must be linear between these thresholds.

Figure 77: Differential Input Slew Rate Definition for CK_t, CK_c, DQS_t, and DQS_c



Output Characteristics and Operating Conditions

Table 80: Single-Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OH(AC)}$	AC output HIGH measurement level (for output slew rate)	$V_{REF} + 0.12$	V	
$V_{OL(AC)}$	AC output LOW measurement level (for output slew rate)	$V_{REF} - 0.12$	V	
$V_{OH(DC)}$	DC output HIGH measurement level (for I-V curve linearity)	$0.9 \times V_{DDQ}$	V	1
$V_{OL(DC)}$	DC output LOW measurement level (for I-V curve linearity)	$0.1 \times V_{DDQ}$	V	2
I_{OZ}	Output leakage current (DQ, DM, DQS_t, DQS_c); DQ, DQS_t, DQS_c are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$	MIN	-5	μA
		MAX	+5	μA



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Table 80: Single-Ended AC and DC Output Levels (Continued)

Symbol	Parameter		Value	Unit	Notes
MMpupd	Delta output impedance between pull-up and pull-down for DQ/DM	MIN	-15	%	
		MAX	+15	%	

- Notes: 1. $I_{OH} = -0.1\text{mA}$.
2. $I_{OL} = 0.1\text{mA}$.

Table 81: Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit
$V_{OH\text{diff}(AC)}$	AC differential output HIGH measurement level (for output SR)	$+ 0.2 \times V_{DDQ}$	V
$V_{OL\text{diff}(AC)}$	AC differential output LOW measurement level (for output SR)	$- 0.2 \times V_{DDQ}$	V

Single-Ended Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 82: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{SE}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{SE}$

- Note: 1. Output slew rate is verified by design and characterization and may not be subject to production testing.



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Figure 78: Single-Ended Output Slew Rate Definition

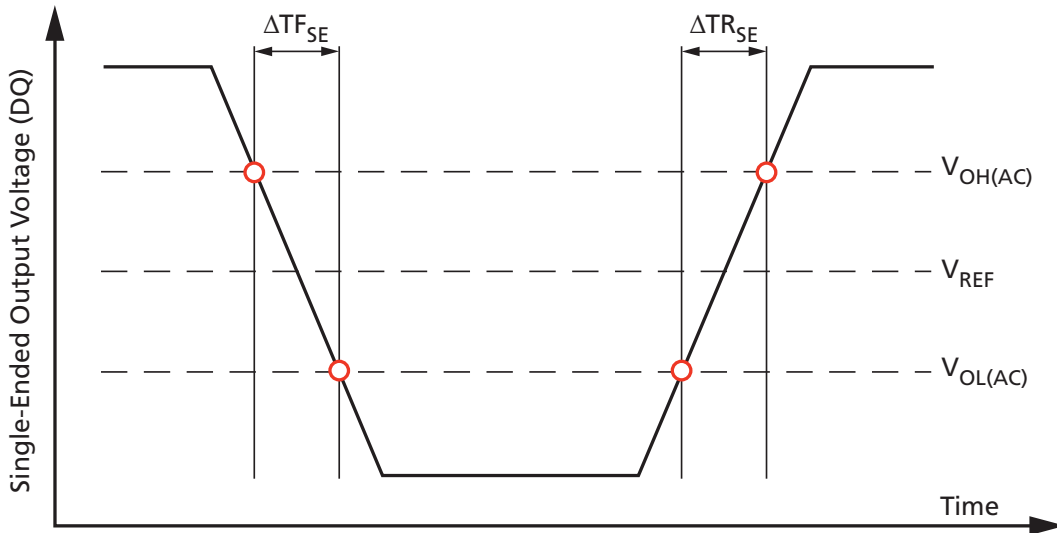


Table 83: Single-Ended Output Slew Rate

Notes 1–5 apply to all parameters conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended output slew rate (output impedance = 40Ω ±30%)	$SR_{Q_{SE}}$	1.5	3.5	V/ns
Single-ended output slew rate (output impedance = 60Ω ±30%)	$SR_{Q_{SE}}$	1.0	2.5	V/ns
Output slew-rate-matching ratio (pull-up to pull-down)		0.7	1.4	–

- Notes:
1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
 2. Measured with output reference load.
 3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
 4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
 5. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

Differential Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.



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Table 84: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TF_{diff}$

Note: 1. Output slew rate is verified by design and characterization and may not be subject to production testing.

Figure 79: Differential Output Slew Rate Definition

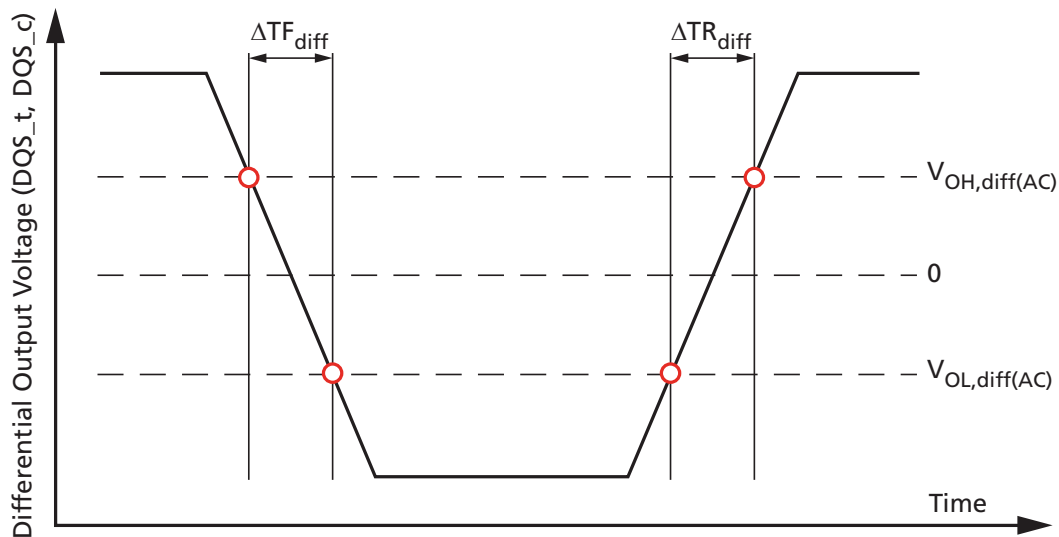


Table 85: Differential Output Slew Rate

Parameter	Symbol	Value		Unit
		Min	Max	
Differential output slew rate (output impedance = $40\Omega \pm 30\%$)	SRQ_{diff}	3.0	7.0	V/ns
Differential output slew rate (output impedance = $60\Omega \pm 30\%$)	SRQ_{diff}	2.0	5.0	V/ns

- Notes:
1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
 2. Measured with output reference load.
 3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
 4. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Output Characteristics and Operating Conditions

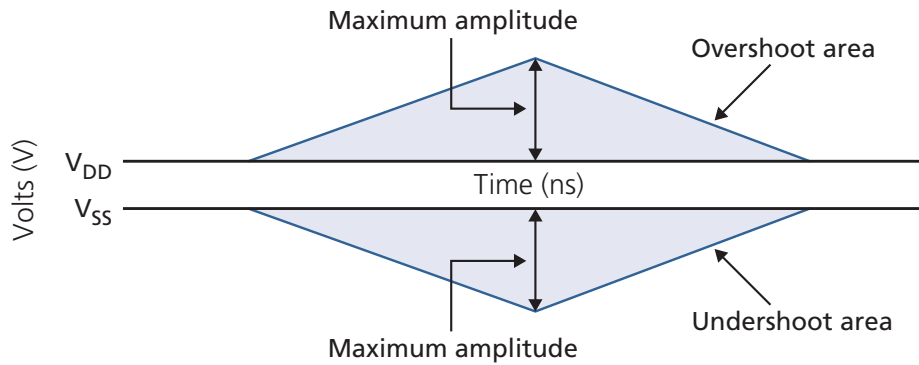
Table 86: AC Overshoot/Undershoot Specification

Applies for CA[9:0], CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM

Parameter	1066	933	800	667	533	466	400	333	266	200	Unit
Maximum peak amplitude provided for overshoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum area above V_{DD}^1	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum area below V_{SS}^2	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns

- Notes: 1. V_{DD} stands for V_{DD2} for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, DQS_t, and DQS_c.
 2. V_{SS} is for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, DQS_t, and DQS_c.

Figure 80: Overshoot and Undershoot Definition



- Notes: 1. V_{DD} stands for V_{DD2} for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, DQS_t, and DQS_c.
 2. V_{SS} is for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, DQS_t, and DQS_c.

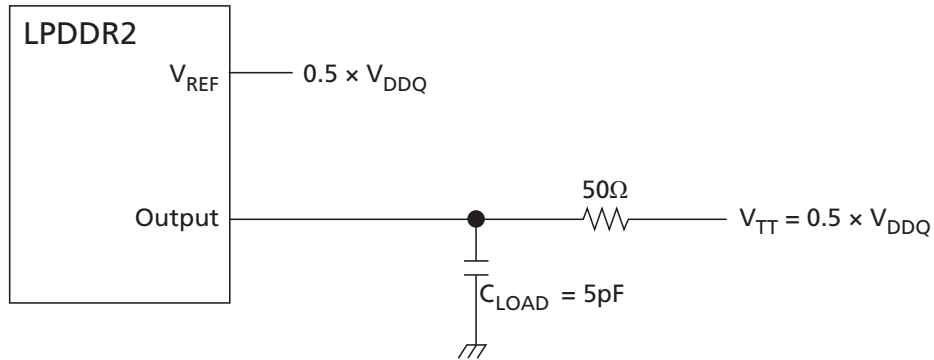
HSUL_12 Driver Output Timing Reference Load

The timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally with one or more coaxial transmission lines terminated at the tester electronics.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Output Driver Impedance

Figure 81: HSUL_12 Driver Output Reference Load for Timing and Slew Rate



Note: 1. All output timing parameter values (t_{DQSCK} , t_{DQSQ} , t_{QHS} , t_{HZ} , t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Output Driver Impedance

Output driver impedance is selected by a mode register during initialization. To achieve tighter tolerances, ZQ calibration is required. Output specifications refer to the default output drive unless specifically stated otherwise. The output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPD} is turned off.

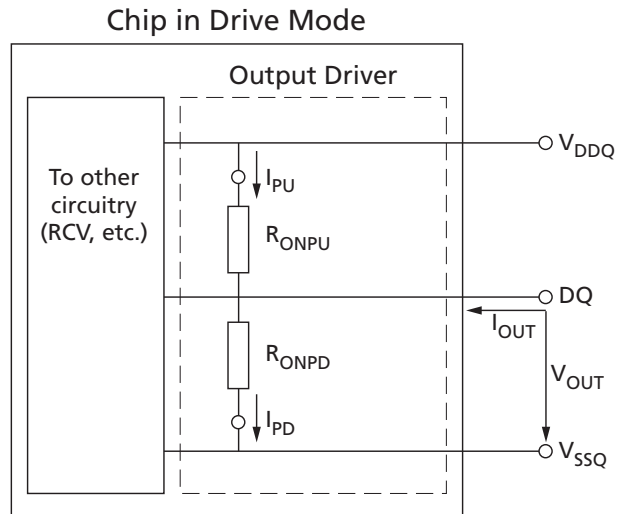
$$R_{ONPD} = \frac{V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPU} is turned off.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Output Driver Impedance

Figure 82: Output Driver



Output Driver Impedance Characteristics with ZQ Calibration

Output driver impedance is defined by the value of the external reference resistor R_{ZQ} . Typical R_{ZQ} is 240 ohms.

Table 87: Output Driver DC Electrical Characteristics with ZQ Calibration

Notes 1–4 apply to all parameters and conditions

R_{ONnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit	Notes
34.3Ω	R_{ON34PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/7$	
	R_{ON34PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/7$	
40.0Ω	R_{ON40PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/6$	
	R_{ON40PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/6$	
48.0Ω	R_{ON48PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/5$	
	R_{ON48PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/5$	
60.0Ω	R_{ON60PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/4$	
	R_{ON60PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/4$	
80.0Ω	R_{ON80PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/3$	
	R_{ON80PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/3$	
120.0Ω (optional)	$R_{ON120PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/2$	
	$R_{ON120PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/2$	
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	5

- Notes:
1. Applies across entire operating temperature range after calibration.
 2. $R_{ZQ} = 240\Omega$.
 3. The tolerance limits are specified after calibration, with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see Output Driver Temperature and Voltage Sensitivity.



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Output Driver Impedance

4. Pull-down and pull-up output driver impedances should be calibrated at $0.5 \times V_{DDQ}$.
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD} : Measure R_{ONPU} and R_{ONPD} , both at $0.5 \times V_{DDQ}$:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

For example, with $MM_{PUPD}(\text{MAX}) = 15\%$ and $R_{ONPD} = 0.85$, R_{ONPU} must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen.

Table 88: Output Driver Sensitivity Definition

Resistor	V_{OUT}	Min	Max	Unit
R_{ONPD}	$0.5 \times V_{DDQ}$	$85 - (dR_{ONdT} \cdot \Delta T) - (dR_{ONdV} \cdot \Delta V)$	$115 + (dR_{ONdT} \cdot \Delta T) + (dR_{ONdV} \cdot \Delta V)$	%
R_{ONPU}				

- Notes:
1. $\Delta T = T - T$ (at calibration). $\Delta V = V - V$ (at calibration).
 2. dR_{ONdT} and dR_{ONdV} are not subject to production testing; they are verified by design and characterization.

Table 89: Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
R_{ONdT}	R_{ON} temperature sensitivity	0.00	0.75	%/°C
R_{ONdV}	R_{ON} voltage sensitivity	0.00	0.20	%/mV

Output Impedance Characteristics Without ZQ Calibration

Output driver impedance is defined by design and characterization as the default setting.

Table 90: Output Driver DC Electrical Characteristics Without ZQ Calibration

$R_{ON,nom}$	Resistor	V_{OUT}	Min	Typ	Max	Unit
34.3Ω	R_{ON34PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/7$
	R_{ON34PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/7$
40.0Ω	R_{ON40PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/6$
	R_{ON40PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/6$
48.0Ω	R_{ON48PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/5$
	R_{ON48PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/5$
60.0Ω	R_{ON60PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/4$
	R_{ON60PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/4$
80.0Ω	R_{ON80PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/3$
	R_{ON80PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/3$



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Output Driver Impedance

Table 90: Output Driver DC Electrical Characteristics Without ZQ Calibration (Continued)

RON _{nom}	Resistor	V _{OUT}	Min	Typ	Max	Unit
120.0Ω (optional)	R _{ON120PD}	0.5 × V _{DDQ}	0.70	1.00	1.30	R _{ZQ} /2
	R _{ON120PU}	0.5 × V _{DDQ}	0.70	1.00	1.30	R _{ZQ} /2

- Notes: 1. Applies across entire operating temperature range without calibration.
2. R_{ZQ} = 240Ω.

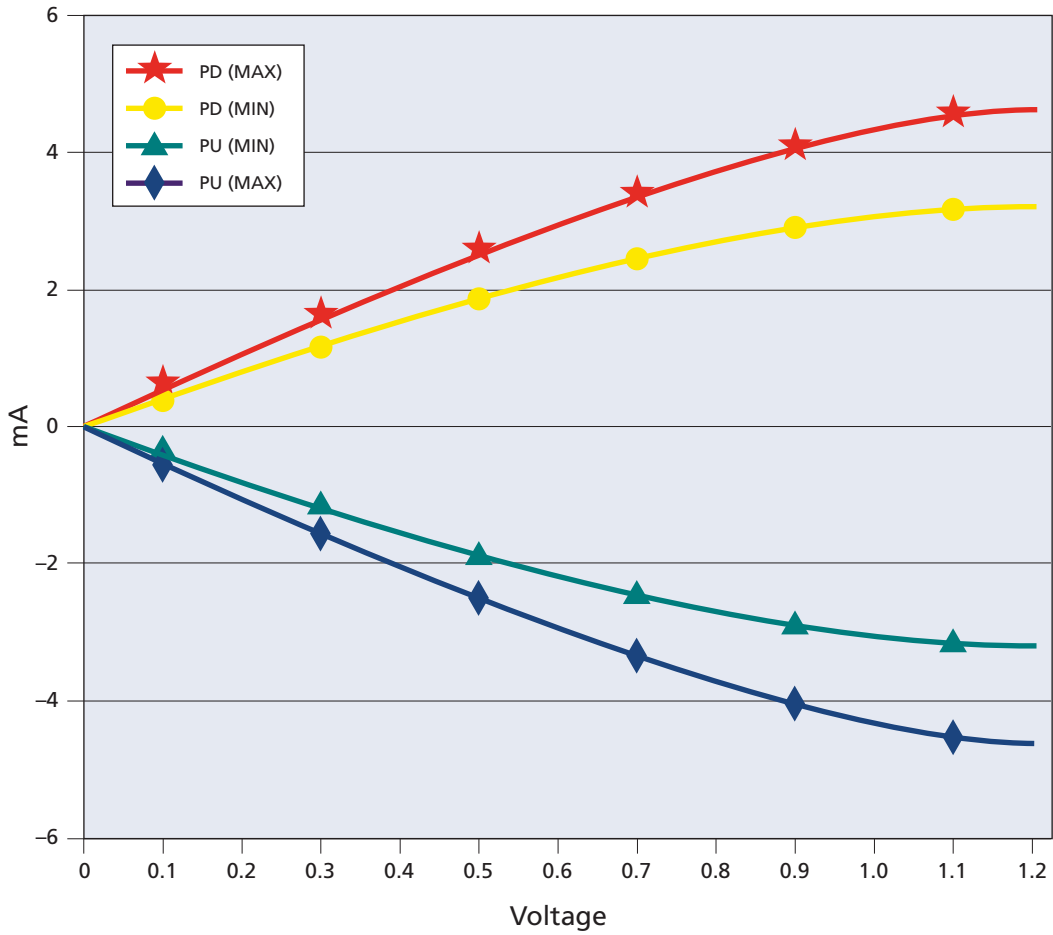
Table 91: I-V Curves

Voltage (V)	R _{ON} = 240Ω (R _{ZQ})							
	Pull-Down				Pull-Up			
	Current (mA) / R _{ON} (ohms)				Current (mA) / R _{ON} (ohms)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Output Driver Impedance

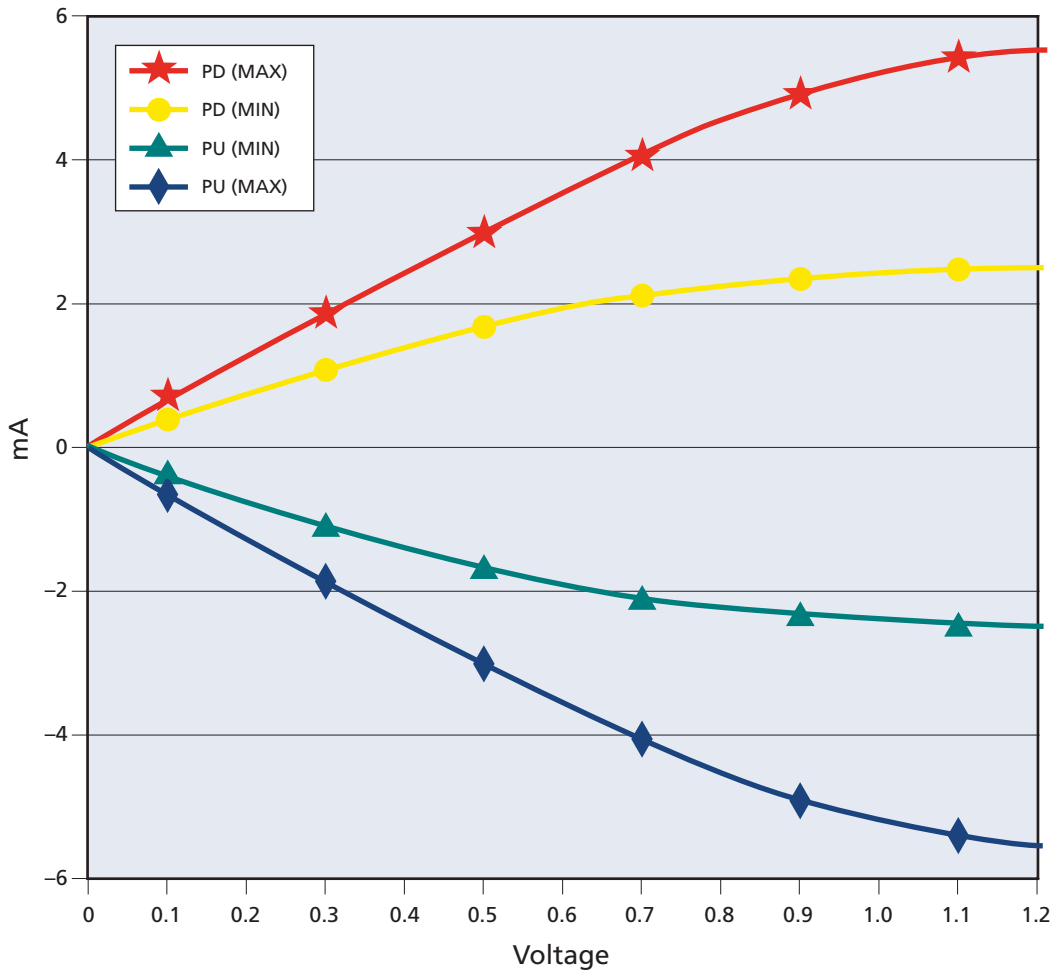
Figure 83: Output Impedance = 240 Ohms, I-V Curves After ZQRESET





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Output Driver Impedance

Figure 84: Output Impedance = 240 Ohms, I-V Curves After Calibration





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Electrical Specifications – I_{DD} Specifications and Conditions

Electrical Specifications – I_{DD} Specifications and Conditions

The following definitions and conditions are used in the I_{DD} measurement tables unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(DC)max}$
- HIGH: $V_{IN} \geq V_{IH(DC)min}$
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following three tables

Table 92: Switching for CA Input Signals

Notes 1–3 apply to all parameters and conditions

	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising	CK_t Rising/ CK_c Fall- ing	CK_t Fall- ing/ CK_c Rising
Cycle	N		N + 1		N + 2		N + 3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

- Notes:
1. CS# must always be driven HIGH.
 2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
 3. The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 93: Switching for I_{DD4R}

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	HLHLLHL	L
Rising	H	L	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Electrical Specifications – I_{DD} Specifications and Conditions

Table 93: Switching for I_{DD4R} (Continued)

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

- Notes: 1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
 2. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4R}.

Table 94: Switching for I_{DD4W}

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	HLHLLHL	L
Rising	H	L	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

- Notes: 1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
 2. Data masking (DM) must always be driven LOW.
 3. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4W}.

Table 95: I_{DD} Specification Parameters and Operating Conditions

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current (SDRAM): ^t CK = ^t CK _{min} ; ^t RC = ^t RC _{min} ; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	I _{DD01}	V _{DD1}	
	I _{DD02}	V _{DD2}	
	I _{DD0in}	V _{DDQ}	4
Idle power-down standby current: ^t CK = ^t CK _{min} ; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I _{DD2P1}	V _{DD1}	
	I _{DD2P2}	V _{DD2}	
	I _{DD2P,in}	V _{DDQ}	4
Idle power-down standby current with clock stop: CK _t = LOW, CK _c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I _{DD2PS1}	V _{DD1}	
	I _{DD2PS2}	V _{DD2}	
	I _{DD2PS,in}	V _{DDQ}	4
Idle non-power-down standby current: ^t CK = ^t CK _{min} ; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I _{DD2N1}	V _{DD1}	
	I _{DD2N2}	V _{DD2}	
	I _{DD2N,in}	V _{DDQ}	4



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Electrical Specifications – I_{DD} Specifications and Conditions

Table 95: I_{DD} Specification Parameters and Operating Conditions (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
Idle non-power-down standby current with clock stopped: CK _t = LOW; CK _c = HIGH; CKE is HIGH; CS _n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I _{DD2NS1}	V _{DD1}	
	I _{DD2NS2}	V _{DD2}	
	I _{DD2NS,in}	V _{DDQ}	4
Active power-down standby current: ^t CK = ^t CK _{min} ; CKE is LOW; CS _n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I _{DD3P1}	V _{DD1}	
	I _{DD3P2}	V _{DD2}	
	I _{DD3P,in}	V _{DDQ}	4
Active power-down standby current with clock stop: CK _t = LOW, CK _c = HIGH; CKE is LOW; CS _n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I _{DD3PS1}	V _{DD1}	
	I _{DD3PS2}	V _{DD2}	
	I _{DD3PS,in}	V _{DDQ}	4
Active non-power-down standby current: ^t CK = ^t CK _{min} ; CKE is HIGH; CS _n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I _{DD3N1}	V _{DD1}	
	I _{DD3N2}	V _{DD2}	
	I _{DD3N,in}	V _{DDQ}	4
Active non-power-down standby current with clock stopped: CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS _n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I _{DD3NS1}	V _{DD1}	
	I _{DD3NS2}	V _{DD2}	
	I _{DD3NS,in}	V _{DDQ}	4
Operating burst READ current: ^t CK = ^t CK _{min} ; CS _n is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer	I _{DD4R1}	V _{DD1}	
	I _{DD4R2}	V _{DD2}	
Operating burst WRITE current: ^t CK = ^t CK _{min} ; CS _n is HIGH between valid commands; One bank is active; BL = 4; WL = WL _{min} ; CA bus inputs are switching; 50% data change each burst transfer	I _{DD4W1}	V _{DD1}	
	I _{DD4W2}	V _{DD2}	
	I _{DD4W,in}	V _{DDQ}	4
All-bank REFRESH burst current: ^t CK = ^t CK _{min} ; CKE is HIGH between valid commands; ^t RC = ^t RFC _{abmin} ; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	I _{DD51}	V _{DD1}	
	I _{DD52}	V _{DD2}	
	I _{DD5IN}	V _{DDQ}	4
All-bank REFRESH average current: ^t CK = ^t CK _{min} ; CKE is HIGH between valid commands; ^t RC = ^t REFI; CA bus inputs are switching; Data bus inputs are stable	I _{DD5AB1}	V _{DD1}	
	I _{DD5AB2}	V _{DD2}	
	I _{DD5AB,in}	V _{DDQ}	4
Per-bank REFRESH average current: ^t CK = ^t CK _{min} ; CKE is HIGH between valid commands; ^t RC = ^t REFI/8; CA bus inputs are switching; Data bus inputs are stable	I _{DD5PB1}	V _{DD1}	5
	I _{DD5PB2}	V _{DD2}	5
	I _{DD5PB,in}	V _{DDQ}	4, 5
Self refresh current (–30°C to +85°C): CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	I _{DD61}	V _{DD1}	6
	I _{DD62}	V _{DD2}	6
	I _{DD6IN}	V _{DDQ}	4, 6
Self refresh current (+85°C to +105°C): CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I _{DD6ET1}	V _{DD1}	6, 7
	I _{DD6ET2}	V _{DD2}	6, 7
	I _{DD6ET,in}	V _{DDQ}	4, 6, 7



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Clock Specification

Table 95: I_{DD} Specification Parameters and Operating Conditions (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
Deep power-down current: CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I _{DD81}	V _{DD1}	7
	I _{DD82}	V _{DD2}	7
	I _{DD8IN}	V _{DDQ}	4, 7

- Notes:
1. I_{DD} values are the maximum of the distribution of the arithmetic mean.
 2. I_{DD} current specifications are tested after the device is properly initialized.
 3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh before going into the extended temperature range.
 4. Measured currents are the sum of V_{DDQ} and V_{DD2}.
 5. Per-bank REFRESH is only applicable for LPDDR2-S4 device densities 1Gb or higher.
 6. This is the general definition that applies to full-array self refresh. Refer to "IDD6 Full and Partial Array Self-Refresh Current" for details of Partial Array Self Refresh IDD6 specification.
 7. I_{DD6ET} and I_{DD8} are typical values, sampled only and not tested.

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 96: Definitions and Calculations

Symbol	Description	Calculation	Notes
t ^{CK} (avg) and nCK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit t ^{CK} (avg) represents the actual clock average t ^{CK} (avg) of the input clock under operation. Unit nCK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. t ^{CK} (avg) can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$t^{CK}(avg) = \left(\sum_{j=1}^N t^{CK}_j \right) / N$ Where N = 200	
t ^{CK} (abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
t ^{CH} (avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t^{CH}(avg) = \left(\sum_{j=1}^N t^{CH}_j \right) / (N \times t^{CK}(avg))$ Where N = 200	


Table 96: Definitions and Calculations (Continued)

Symbol	Description	Calculation	Notes
$t_{CL(avg)}$	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL(avg)} = \left(\sum_{j=1}^N t_{CL_j} \right) / (N \times t_{CK(avg)})$ Where $N = 200$	
$t_{JIT(per)}$	The single-period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.	$t_{JIT(per)} = \min/\max \text{ of } \left\{ t_{CK_i} - t_{CK(avg)} \right\}$ Where $i = 1$ to 200	1
$t_{JIT(per),act}$	The actual clock jitter for a given system.		
$t_{JIT(per),allowed}$	The specified clock period jitter allowance.		
$t_{JIT(cc)}$	The absolute difference in clock periods between two consecutive clock cycles. $t_{JIT(cc)}$ defines the cycle-to-cycle jitter.	$t_{JIT(cc)} = \max \text{ of } \left\{ t_{CK_{i+1}} - t_{CK_i} \right\}$	1
$t_{ERR(nper)}$	The cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.	$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j} \right) - (n \times t_{CK(avg)})$	1
$t_{ERR(nper),act}$	The actual cumulative error over n cycles for a given system.		
$t_{ERR(nper),allowed}$	The specified cumulative error allowance over n cycles.		
$t_{ERR(nper),min}$	The minimum $t_{ERR(nper)}$.	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	2
$t_{ERR(nper),max}$	The maximum $t_{ERR(nper)}$.	$t_{ERR(nper),max} = (1 + 0.68LN(n)) \times t_{JIT(per),max}$	2
$t_{JIT(duty)}$	Defined with absolute and average specifications for t_{CH} and t_{CL} , respectively.	$t_{JIT(duty),min} = \text{MIN}((t_{CH(ABS),min} - t_{CH(avg),min}), (t_{CL(ABS),min} - t_{CL(avg),min})) \times t_{CK(avg)}$ $t_{JIT(duty),max} = \text{MAX}((t_{CH(ABS),max} - t_{CH(avg),max}), (t_{CL(ABS),max} - t_{CL(avg),max})) \times t_{CK(avg)}$	

- Notes: 1. Not subject to production testing.
2. Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per),act}$ value.

$t_{CK(ABS)}$, $t_{CH(ABS)}$, and $t_{CL(ABS)}$

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Table 97: $t_{CK(ABS)}$, $t_{CH(ABS)}$, and $t_{CL(ABS)}$ Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	$t_{CK(ABS)}$	$t_{CK(avg),min} + t_{JIT(per),min}$	ps ¹
Absolute clock HIGH pulse width	$t_{CH(ABS)}$	$t_{CH(avg),min} + t_{JIT(duty),min}^2 / t_{CK(avg),min}$	$t_{CK(avg)}$


Table 97: $t_{CK(ABS)}$, $t_{CH(ABS)}$, and $t_{CL(ABS)}$ Definitions (Continued)

Parameter	Symbol	Minimum	Unit
Absolute clock LOW pulse width	$t_{CL(ABS)}$	$t_{CL(AVG),MIN} + t_{JIT(DUTY),MIN}^2/t_{CK(AVG),MIN}$	$t_{CK(AVG)}$

- Notes: 1. $t_{CK(AVG),MIN}$ is expressed in ps for this table.
2. $t_{JIT(DUTY),MIN}$ is a negative value.

Clock Period Jitter

The LPDDR2 device can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter ($t_{JIT(per)}$) in excess of the values found in the AC Timing section. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (t_{RCD} , t_{RP} , t_{RTP} , t_{WR} , t_{WRA} , t_{WTR} , t_{RC} , t_{RAS} , t_{RRD} , t_{FAW}) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support $t_{nPARAM} = RU[t_{PARAM}/t_{CK(AVG)}]$. During device operation where clock jitter is outside specification limits, the number of clocks or $t_{CK(AVG)}$, may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (t_{nPARAM}), when $t_{CK(AVG)}$ and $t_{ERR}(t_{nPARAM},act)$ exceed $t_{ERR}(t_{nPARAM},allowed)$, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left\{\frac{t_{nPARAM} + t_{ERR}(t_{nPARAM},act) - t_{ERR}(t_{nPARAM},allowed)}{t_{nPARAM}} - t_{CK(AVG)}\right\}, 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (t_{nPARAM}), clock cycle derating should be specified with $t_{JIT(per)}$.

For a given number of clocks (t_{nPARAM}), when $t_{CK(AVG)}$ plus $t_{ERR}(t_{nPARAM},act)$ exceed the supported cumulative $t_{ERR}(t_{nPARAM},allowed)$, derating is required. If the equation below results in a positive value for a core timing parameter (t_{CORE}), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = RU\left\{\frac{t_{nPARAM} + t_{ERR}(t_{nPARAM},act) - t_{ERR}(t_{nPARAM},allowed)}{t_{CK(AVG)}}\right\} - t_{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.



Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (t_{IS} , t_{IH} , t_{ISCKE} , t_{IHCKE} , t_{ISb} , t_{IHb} , t_{ISCKEb} , t_{IHCKEb}) are measured from a command/address signal (CKE, CS_n, or CA[9:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the $t_{JIT(per)}$ applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

t_{RPRE}

When the device is operated with input clock jitter, t_{RPRE} must be derated by the $t_{JIT(per),act,max}$ of the input clock that exceeds $t_{JIT(per),allowed,max}$. Output deratings are relative to the input clock:

$$t_{RPRE(min,derated)} = 0.9 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}} \right)$$

For example, if the measured jitter into a LPDDR2-800 device has $t_{CK(avg)} = 2500ps$, $t_{JIT(per),act,min} = -172ps$, and $t_{JIT(per),act,max} = +193ps$, then $t_{RPRE,min,derated} = 0.9 - (t_{JIT(per),act,max} - t_{JIT(per),allowed,max})/t_{CK(avg)} = 0.9 - (193 - 100)/2500 = 0.8628 t_{CK(avg)}$.

$t_{LZ(DQ)}$, $t_{HZ(DQ)}$, t_{DQSCK} , $t_{LZ(DQS)}$, $t_{HZ(DQS)}$

These parameters are measured from a specific clock edge to a data signal transition (DM_n or DQ_m, where: $n = 0, 1, 2, \text{ or } 3$; and $m = DQ[31:0]$), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by $t_{JIT(per)}$.

t_{QSH} , t_{QSL}

These parameters are affected by duty cycle jitter, represented by $t_{CH(abs)min}$ and $t_{CL(abs)min}$. These parameters determine the absolute data valid window at the device pin. The absolute minimum data valid window at the device pin = $\min [(t_{QSH(abs)min} \times t_{CK(avg)min} - t_{DQSQmax} - t_{QHSmax}), (t_{QSL(abs)min} \times t_{CK(avg)min} - t_{DQSQmax} - t_{QHSmax})]$. This minimum data valid window must be met at the target frequency regardless of clock jitter.

t_{RPST}

t_{RPST} is affected by duty cycle jitter, represented by $t_{CL(abs)}$. Therefore, $t_{RPST(abs)min}$ can be specified by $t_{CL(abs)min}$. $t_{RPST(abs)min} = t_{CL(abs)min} - 0.05 = t_{QSL(abs)min}$.

Clock Jitter Effects on WRITE Timing Parameters

t_{DS} , t_{DH}

These parameters are measured from a data signal (DM_n or DQ_m, where $n = 0, 1, 2, 3$; and $m = DQ[31:0]$) transition edge to its respective data strobe signal (DQS_{n_t}, DQS_{n_c}; $n = 0, 1, 2, 3$) crossing. The specification values are not affected by the amount of $t_{JIT(per)}$ applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

t_{DSS} , t_{DSH}



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These parameters are measured from a data strobe signal crossing (DQS_{x_t}, DQS_{x_c}) to its clock signal crossing (CK_t/CK_c). The specification values are not affected by the amount of ^tJIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^tDQSS

^tDQSS is measured from the clock signal crossing (CK_t/CK_c) to the first latching data strobe signal crossing (DQS_{x_t}, DQS_{x_c}). When the device is operated with input clock jitter, this parameter must be derated by the actual ^tJIT(per)_{act} of the input clock in excess of ^tJIT(per)_{allowed}.

$${}^tDQSS(\text{min,derated}) = 0.75 - \left(\frac{{}^tJIT(\text{per})_{\text{act,min}} - {}^tJIT(\text{per})_{\text{allowed,min}}}{{}^tCK(\text{avg})} \right)$$

$${}^tDQSS(\text{max,derated}) = 1.25 - \left(\frac{{}^tJIT(\text{per})_{\text{act,max}} - {}^tJIT(\text{per})_{\text{allowed,max}}}{{}^tCK(\text{avg})} \right)$$

For example, if the measured jitter into an LPDDR2-800 device has ^tCK(avg) = 2500ps, ^tJIT(per)_{act,min} = -172ps, and ^tJIT(per)_{act,max} = +193ps, then:

$${}^tDQSS(\text{min,derated}) = 0.75 - ({}^tJIT(\text{per})_{\text{act,min}} - {}^tJIT(\text{per})_{\text{allowed,min}}) / {}^tCK(\text{avg}) = 0.75 - (-172 + 100) / 2500 = 0.7788 \text{ } {}^tCK(\text{avg}), \text{ and}$$

$${}^tDQSS(\text{max,derated}) = 1.25 - ({}^tJIT(\text{per})_{\text{act,max}} - {}^tJIT(\text{per})_{\text{allowed,max}}) / {}^tCK(\text{avg}) = 1.25 - (193 - 100) / 2500 = 1.2128 \text{ } {}^tCK(\text{avg}).$$



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Refresh Requirements Parameters

Refresh Requirements Parameters

Table 98: Refresh Requirement Parameters (Per Density)

Parameter	Symbol	64Mb	128Mb	256Mb	512Mb	1Gb	2Gb	4Gb	8Gb	Unit	
Number of banks		4	4	4	4	8	8	8	8		
Refresh window: $T_{CASE} \leq 85^{\circ}$	t_{REFW}	32	32	32	32	32	32	32	32	ms	
Refresh window: $85^{\circ}C < T_{CASE} \leq 105^{\circ}C$	t_{REFW}	8	8	8	8	8	8	8	8	ms	
Required number of REFRESH commands (MIN)	R	2048	2048	4096	4096	4096	8192	8192	8192		
Average time between REFRESH commands (for reference only) $T_{CASE} \leq 85^{\circ}C$	REFab	t_{REFI}	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	μs
	REFpb	t_{REFIpb}	(REFpb not supported below 1Gb)				0.975	0.4875	0.4875	0.4875	μs
Refresh cycle time	t_{RFCab}	90	90	90	90	130	130	130	210	ns	
Per-bank REFRESH cycle time	t_{RFCpb}	na				60	60	60	90	ns	
Burst REFRESH window = $4 \times 8 \times t_{RFCab}$	t_{REFBW}	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	μs	

AC Timing

Table 99: AC Timing

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the t_{CK} minimum conditions (in multiples of t_{CK}) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/Max	t_{CK} Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Maximum frequency		–	–	533	466	400	333	266	200	166	MHz	
Clock Timing												
Average clock period	$t_{CK}(avg)$	MIN	–	1.875	2.15	2.5	3	3.75	5	6	ns	
		MAX	–	100	100	100	100	100	100	100		
Average HIGH pulse width	$t_{CH}(avg)$	MIN	–	0.45	0.45	0.45	0.45	0.45	0.45	0.45	$t_{CK}(avg)$	
		MAX	–	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Average LOW pulse width	$t_{CL}(avg)$	MIN	–	0.45	0.45	0.45	0.45	0.45	0.45	0.45	$t_{CK}(avg)$	
		MAX	–	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Absolute clock period	$t_{CK}(abs)$	MIN	–	$t_{CK}(avg)min \pm t_{JIT}(per)min$							ps	
Absolute clock HIGH pulse width (with allowed jitter)	$t_{CH}(abs), allowed$	MIN	–	0.43	0.43	0.43	0.43	0.43	0.43	0.43	$t_{CK}(avg)$	
		MAX	–	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Absolute clock LOW pulse width (with allowed jitter)	$t_{CL}(abs), allowed$	MIN	–	0.43	0.43	0.43	0.43	0.43	0.43	0.43	$t_{CK}(avg)$	
		MAX	–	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Clock period jitter (with supported jitter)	$t_{JIT}(per), allowed$	MIN	–	-90	-95	-100	-110	-120	-140	-150	ps	
		MAX	–	90	95	100	110	120	140	150		



**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
AC Timing**

Table 99: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the ^tCK minimum conditions (in multiples of ^tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	^t CK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Maximum clock jitter between two consecutive clock cycles (with allowed jitter)	^t JIT(cc), allowed	MAX	–	180	190	200	220	240	280	300	ps	
Duty cycle jitter (with allowed jitter)	^t JIT(duty), allowed	MIN	–	MIN ((^t CH(abs),min - ^t CH(avg),min), (^t CL(abs),min - ^t CL(avg),min)) × ^t CK(avg)							ps	
		MAX	–	MAX ((^t CH(abs),max - ^t CH(avg),max), (^t CL(abs),max - ^t CL(avg),max)) × ^t CK(avg)								
Cumulative errors across 2 cycles	^t ERR(2per), allowed	MIN	–	-132	-140	-147	-162	-177	-206	-221	ps	
		MAX	–	132	140	147	162	177	206	221		
Cumulative errors across 3 cycles	^t ERR(3per), allowed	MIN	–	-157	-166	-175	-192	-210	-245	-262	ps	
		MAX	–	157	166	175	192	210	245	262		
Cumulative errors across 4 cycles	^t ERR(4per), allowed	MIN	–	-175	-185	-194	-214	-233	-272	-291	ps	
		MAX	–	175	185	194	214	233	272	291		
Cumulative errors across 5 cycles	^t ERR(5per), allowed	MIN	–	-188	-199	-209	-230	-251	-293	-314	ps	
		MAX	–	188	199	209	230	251	293	314		
Cumulative errors across 6 cycles	^t ERR(6per), allowed	MIN	–	-200	-211	-222	-244	-266	-311	-333	ps	
		MAX	–	200	211	222	244	266	311	333		
Cumulative errors across 7 cycles	^t ERR(7per), allowed	MIN	–	-209	-221	-232	-256	-279	-325	-348	ps	
		MAX	–	209	221	232	256	279	325	348		
Cumulative errors across 8 cycles	^t ERR(8per), allowed	MIN	–	-217	-229	-241	-266	-290	-338	-362	ps	
		MAX	–	217	229	241	266	290	338	362		
Cumulative errors across 9 cycles	^t ERR(9per), allowed	MIN	–	-224	-237	-249	-274	-299	-349	-374	ps	
		MAX	–	224	237	249	274	299	349	374		
Cumulative errors across 10 cycles	^t ERR(10per), allowed	MIN	–	-231	-244	-257	-282	-308	-359	-385	ps	
		MAX	–	231	244	257	282	308	359	385		
Cumulative errors across 11 cycles	^t ERR(11per), allowed	MIN	–	-237	-250	-263	-289	-316	-368	-395	ps	
		MAX	–	237	250	263	289	316	368	395		
Cumulative errors across 12 cycles	^t ERR(12per), allowed	MIN	–	-242	-256	-269	-296	-323	-377	-403	ps	
		MAX	–	242	256	269	296	323	377	403		
Cumulative errors across $n = 13, 14, 15, \dots, 49, 50$ cycles	^t ERR(nper), allowed	MIN		$\sup{t}ERR(nper), allowed, min = (1 + 0.68 \ln(n)) \times \sup{t}JIT(per), allowed, min$							ps	
		MAX		$\sup{t}ERR(nper), allowed, max = (1 + 0.68 \ln(n)) \times \sup{t}JIT(per), allowed, max$								
ZQ Calibration Parameters												
Initialization calibration time	^t ZQINIT	MIN	–	1	1	1	1	1	1	1	μs	
Long calibration time	^t ZQCL	MIN	6	360	360	360	360	360	360	360	ns	
Short calibration time	^t ZQCS	MIN	6	90	90	90	90	90	90	90	ns	



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP AC Timing

Table 99: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the t_{CK} minimum conditions (in multiples of t_{CK}) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	t_{CK} Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Calibration RESET time	$t_{ZQRESET}$	MIN	3	50	50	50	50	50	50	50	ns	
READ Parameters³												
DQS output access time from CK_t/CK_c	t_{DQSCK}	MIN	–	2500	2500	2500	2500	2500	2500	2500	ps	
		MAX	–	5500	5500	5500	5500	5500	5500	5500		
DQSCK delta short	$t_{DQSCKDS}$	MAX	–	330	380	450	540	670	900	1080	ps	4
DQSCK delta medium	$t_{DQSCKDM}$	MAX	–	680	780	900	1050	1350	1800	1900	ps	5
DQSCK delta long	$t_{DQSCKDL}$	MAX	–	920	1050	1200	1400	1800	2400	–	ps	6
DQS-DQ skew	t_{DQSQ}	MAX	–	200	220	240	280	340	400	500	ps	
Data-hold skew factor	t_{QHS}	MAX	–	230	260	280	340	400	480	600	ps	
DQS output HIGH pulse width	t_{QSH}	MIN	–	$t_{CH(ABS)} - 0.05$							t_{CK} (avg)	
DQS output LOW pulse width	t_{QSL}	MIN	–	$t_{CL(ABS)} - 0.05$							t_{CK} (avg)	
Data half period	t_{QHP}	MIN	–	MIN (t_{QSH} , t_{QSL})							t_{CK} (avg)	
DQ/DQS output hold time from DQS	t_{QH}	MIN	–	$t_{QHP} - t_{QHS}$							ps	
READ preamble	t_{RPRE}	MIN	–	0.9	0.9	0.9	0.9	0.9	0.9	0.9	t_{CK} (avg)	7
READ postamble	t_{RPST}	MIN	–	$t_{CL(ABS)} - 0.05$							t_{CK} (avg)	8
DQS Low-Z from clock	$t_{LZ(DQS)}$	MIN	–	$t_{DQSCK(MIN)} - 300$							ps	
DQ Low-Z from clock	$t_{LZ(DQ)}$	MIN	–	$t_{DQSCK(MIN)} - (1.4 \times t_{QHS(MAX)})$							ps	
DQS High-Z from clock	$t_{HZ(DQS)}$	MAX	–	$t_{DQSCK(MAX)} - 100$							ps	
DQ High-Z from clock	$t_{HZ(DQ)}$	MAX	–	$t_{DQSCK(MAX)} + (1.4 \times t_{DQSQ(MAX)})$							ps	
WRITE Parameters³												
DQ and DM input hold time (V_{REF} based)	t_{DH}	MIN	–	210	235	270	350	430	480	600	ps	
DQ and DM input setup time (V_{REF} based)	t_{DS}	MIN	–	210	235	270	350	430	480	600	ps	
DQ and DM input pulse width	t_{DIPW}	MIN	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	t_{CK} (avg)	
Write command to first DQS latching transition	t_{DQSS}	MIN	–	0.75	0.75	0.75	0.75	0.75	0.75	0.75	t_{CK} (avg)	
		MAX	–	1.25	1.25	1.25	1.25	1.25	1.25	1.25	t_{CK} (avg)	
DQS input high-level width	t_{DQSH}	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	t_{CK} (avg)	


**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
AC Timing**
Table 99: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the t_{CK} minimum conditions (in multiples of t_{CK}) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	t_{CK} Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
DQS input low-level width	t_{DQSL}	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	t_{CK} (avg)	
DQS falling edge to CK setup time	t_{DSS}	MIN	–	0.2	0.2	0.2	0.2	0.2	0.2	0.2	t_{CK} (avg)	
DQS falling edge hold time from CK	t_{DSH}	MIN	–	0.2	0.2	0.2	0.2	0.2	0.2	0.2	t_{CK} (avg)	
Write postamble	t_{WPST}	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	t_{CK} (avg)	
Write preamble	t_{WPRE}	MIN	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	t_{CK} (avg)	
CKE Input Parameters												
CKE minimum pulse width (HIGH and LOW pulse width)	t_{CKE}	MIN	3	3	3	3	3	3	3	3	t_{CK} (avg)	
CKE input setup time	t_{ISCKE}	MIN	–	0.25	0.25	0.25	0.25	0.25	0.25	0.25	t_{CK} (avg)	9
CKE input hold time	t_{IHCKE}	MIN	–	0.25	0.25	0.25	0.25	0.25	0.25	0.25	t_{CK} (avg)	10
Command Address Input Parameters³												
Address and control input setup time (Vref based)	t_{IS}	MIN	–	220	250	290	370	460	600	740	ps	11
Address and control input hold time (Vref based)	t_{IH}	MIN	–	220	250	290	370	460	600	740	ps	11
Address and control input pulse width	t_{IPW}	MIN	–	0.40	0.40	0.40	0.40	0.40	0.40	0.40	t_{CK} (avg)	
Boot Parameters (10 MHz–55 MHz)^{12, 13, 14}												
Clock cycle time	t_{CKb}	MAX	–	100	100	100	100	100	100	100	ns	
		MIN	–	18	18	18	18	18	18	18		
CKE input setup time	t_{ISCKEb}	MIN	–	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
CKE input hold time	t_{IHCKEb}	MIN	–	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
Address and control input setup time	t_{ISb}	MIN	–	1150	1150	1150	1150	1150	1150	1150	ps	
Address and control input hold time	t_{IHb}	MIN	–	1150	1150	1150	1150	1150	1150	1150	ps	
DQS output data access time from CK_t/CK_c	t_{DQSCKb}	MIN	–	2.0	2.0	2.0	2.0	2.0	2.0	2.0	ns	
		MAX	–	10.0	10.0	10.0	10.0	10.0	10.0	10.0		
Data strobe edge to output data edge $t_{DQSQb} - 1.2$	t_{DQSQb}	MAX	–	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	
Data hold skew factor	t_{QHSb}	MAX	–	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	


**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
AC Timing**
Table 99: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the t_{CK} minimum conditions (in multiples of t_{CK}) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	t_{CK} Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Mode Register Parameters												
MODE REGISTER WRITE command period	t_{MRW}	MIN	5	5	5	5	5	5	5	5	t_{CK} (avg)	
MODE REGISTER READ command period	t_{MRR}	MIN	2	2	2	2	2	2	2	2	t_{CK} (avg)	
Core Parameters¹⁵												
READ latency	RL	MIN	3	8	7	6	5	4	3	3	t_{CK} (avg)	
WRITE latency	WL	MIN	1	4	4	3	2	2	1	1	t_{CK} (avg)	
ACTIVATE-to-ACTIVATE command period	t_{RC}	MIN	–	$t_{RAS} + t_{RPab}$ (with all-bank precharge), $t_{RAS} + t_{RPpb}$ (with per-bank precharge)							ns	17
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	t_{CKESR}	MIN	3	15	15	15	15	15	15	15	ns	
SELF REFRESH exit to next valid command delay	t_{XSR}	MIN	2	$t_{RFCab} + 10$							ns	
Exit power-down to next valid command delay	t_{XP}	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
CAS-to-CAS delay	t_{CCD}	MIN	2	2	2	2	2	2	2	2	t_{CK} (avg)	
Internal READ to PRECHARGE command delay	t_{RTP}	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
RAS-to-CAS delay	t_{RCD}	MIN	3	18	18	18	18	18	18	18	ns	
Row precharge time (single bank)	t_{RPpb}	MIN	3	18	18	18	18	18	18	18	ns	
Row precharge time (all banks)	t_{RPab} 4-bank	MIN	3	18	18	18	18	18	18	18	ns	
Row precharge time (all banks)	t_{RPab} 8-bank	MIN	3	21	21	21	21	21	21	21	ns	
Row active time	t_{RAS}	MIN	3	42	42	42	42	42	42	42	ns	
		MAX	–	70	70	70	70	70	70	70	μs	
WRITE recovery time	t_{WR}	MIN	3	15	15	15	15	15	15	15	ns	
Internal WRITE-to-READ command delay	t_{WTR}	MIN	2	7.5	7.5	7.5	7.5	7.5	10	10	ns	
Active bank <i>a</i> to active bank <i>b</i>	t_{RRD}	MIN	2	10	10	10	10	10	10	10	ns	
Four-bank activate window	t_{FAW}	MIN	8	50	50	50	50	50	50	60	ns	
Minimum deep power-down time	t_{DPD}	MIN	–	500	500	500	500	500	500	500	μs	
Temperature Derating¹⁶												


Table 99: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the t_{CK} minimum conditions (in multiples of t_{CK}) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	t_{CK} Min	Data Rate						Unit	Notes	
				1066	933	800	667	533	400			333
t_{DQCK} derating	t_{DQCK} (derated)	MAX	–	5620	6000	6000	6000	6000	6000	6000	ps	
Core timing temperature derating	t_{RCD} (derated)	MIN	–	$t_{RCD} + 1.875$						ns		
	t_{RC} (derated)	MIN	–	$t_{RC} + 1.875$						ns		
	t_{RAS} (derated)	MIN	–	$t_{RAS} + 1.875$						ns		
	t_{RP} (derated)	MIN	–	$t_{RP} + 1.875$						ns		
	t_{RRD} (derated)	MIN	–	$t_{RRD} + 1.875$						ns		

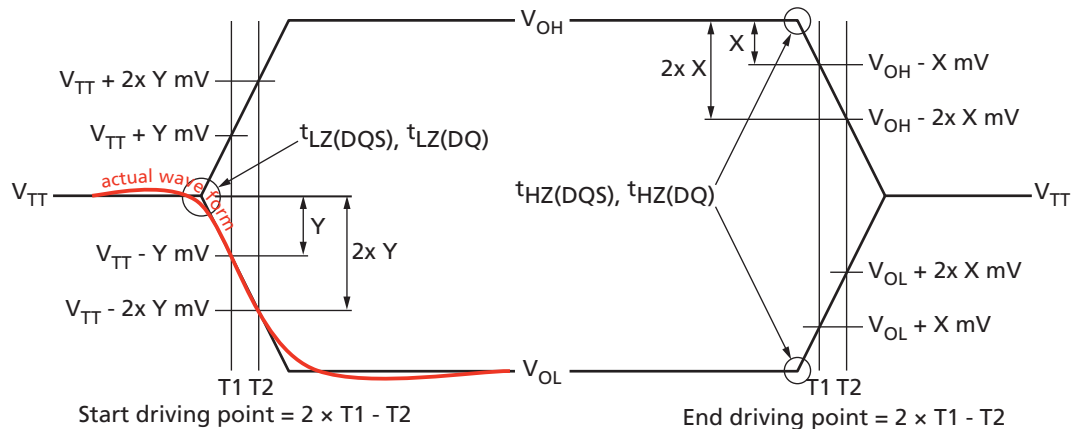
- Notes:
- Frequency values are for reference only. Clock cycle time (t_{CK}) is used to determine device capabilities.
 - All AC timings assume an input slew rate of 1 V/ns.
 - READ, WRITE, and input setup and hold values are referenced to V_{REF} .
 - t_{DQCKDS} is the absolute value of the difference between any two t_{DQCK} measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. t_{DQCKDS} is not tested and is guaranteed by design. Temperature drift in the system is $<10^{\circ}C/s$. Values do not include clock jitter.
 - t_{DQCKDM} is the absolute value of the difference between any two t_{DQCK} measurements (in a byte lane) within a 1.6 μ s rolling window. t_{DQCKDM} is not tested and is guaranteed by design. Temperature drift in the system is $<10^{\circ}C/s$. Values do not include clock jitter.
 - t_{DQCKDL} is the absolute value of the difference between any two t_{DQCK} measurements (in a byte lane) within a 32ms rolling window. t_{DQCKDL} is not tested and is guaranteed by design. Temperature drift in the system is $<10^{\circ}C/s$. Values do not include clock jitter.

For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). t_{HZ} and t_{LZ} transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for t_{RPST} , $t_{HZ}(DQS)$ and $t_{HZ}(DQ)$), or begins driving (for t_{RPRE} , $t_{LZ}(DQS)$, $t_{LZ}(DQ)$). The figure below shows a method to calculate the point when the device is no longer driving $t_{HZ}(DQS)$ and $t_{HZ}(DQ)$ or begins driving $t_{LZ}(DQS)$ and $t_{LZ}(DQ)$ by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters $t_{LZ}(DQS)$, $t_{LZ}(DQ)$, $t_{HZ}(DQS)$, and $t_{HZ}(DQ)$ are defined as single-ended. The timing parameters t_{RPRE} and t_{RPST} are determined from the differential signal DQS_t/DQS_c .

Output Transition Timing



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP CA and CS_n Setup, Hold, and Derating



7. Measured from the point when DQS_t/DQS_c begins driving the signal, to the point when DQS_t/DQS_c begins driving the first rising strobe edge.
8. Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
9. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK_t/CK_c crossing.
10. CKE input hold time is measured from CK_t/CK_n crossing to CKE reaching a HIGH/LOW voltage level.
11. Input setup/hold time for signal (CA[9:0], CS_n).
12. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. The letter b is appended to the boot parameter symbols (for example, ^tCK during boot is ^tCKb).
13. Mobile LPDDR2 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.
14. The output skew parameters are measured with default output impedance settings using the reference load.
15. The minimum ^tCK column applies only when ^tCK is greater than 6ns.
16. Timing derating applies for operation at 85°C to 105°C when the requirement to derate is indicated by mode register 4 op-code (see the MR4 Device Temperature (MA[7:0] = 04h) table).
17. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

CA and CS_n Setup, Hold, and Derating

For all input signals (CA and CS_n), the total required setup time (^tIS) and hold time (^tIH) are calculated by adding the data sheet ^tIS (base) and ^tIH (base) values to the Δ^tIS and Δ^tIH derating values, respectively. Example: ^tIS (total setup time) = ^tIS(base) + Δ^tIS. (See the series of tables following this section.)

The typical setup slew rate (^tIS) for a rising signal is defined as the slew rate between the last crossing of V_{REF(DC)} and the first crossing of V_{IH(AC)min}. The typical setup slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF(DC)} and the first crossing of V_{IL(AC)max}. If the actual signal is consistently earlier than the typical slew rate line between the shaded V_{REF(DC)}-to-(AC) region, use the typical slew rate for the derating value (see Figure 85 (page 157)). If the actual signal is later than the typical slew rate line anywhere between the shaded V_{REF(DC)}-to-AC region, the slew rate of a



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP CA and CS_n Setup, Hold, and Derating

tangent line to the actual signal from the AC level to the DC level is used for the derating value (see Figure 87 (page 159)).

The hold (t_{IH}) typical slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. The hold (t_{IH}) typical slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is consistently later than the typical slew rate line between the shaded DC-to- $V_{REF(DC)}$ region, use the typical slew rate for the derating value (see Figure 86 (page 158)). If the actual signal is earlier than the typical slew rate line anywhere between the shaded DC-to- $V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see Figure 88 (page 160)).

For a valid transition, the input signal must remain above or below $V_{IH}/V_{IL(AC)}$ for a specified time, t_{VAC} (see Table 104 (page 155)).

For slow slew rates the total setup time could be a negative value; that is, a valid input signal will not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition. A valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in Table 102, the derating values are obtained using linear interpolation. Typically, slew rate values are not subject to production testing. They are verified by design and characterization.

Table 100: CA and CS_n Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
t_{IS} (base)	0	30	70	150	240	300	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220mV$
t_{IH} (base)	90	120	160	240	330	390	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130mV$

Note: 1. AC/DC referenced for 1 V/ns CA and CS_n slew rate, and 2 V/ns differential CK_t/CK_c slew rate.

Table 101: CA and CS_n Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate				Reference
	400	333	266	200	
t_{IS} (base)	300	440	600	850	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 300mV$
t_{IH} (base)	400	540	700	950	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 200mV$

Note: 1. AC/DC referenced for 1 V/ns CA and CS_n slew rate, and 2 V/ns differential CK_t/CK_c slew rate.



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CA and CS_n Setup, Hold, and Derating**

Table 102: Derating Values for AC/DC-Based t_{IS}/t_{IH} (AC220)

Δt_{IS} , Δt_{IH} derating in ps

AC220 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+220mV$, $V_{IL(ac)}=V_{REF(dc)}-220mV$

DC100 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+130mV$, $V_{IL(dc)}=V_{REF(dc)}-130mV$

		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CA, CS_n slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: 1. Shaded cells are not supported.

Table 103: Derating Values for AC/DC-Based t_{IS}/t_{IH} (AC300)

Δt_{IS} , Δt_{IH} derating in ps

AC300 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+300mV$, $V_{IL(ac)}=V_{REF(dc)}-300mV$

DC200 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+200mV$, $V_{IL(dc)}=V_{REF(dc)}-200mV$

		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CA, CS_n slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: 1. Shaded cells are not supported.

Table 104: Required Time for Valid Transition – $t_{VAC} > V_{IH(AC)}$ and $< V_{IL(AC)}$

Slew Rate (V/ns)	t_{VAC} at 300mV (ps)		t_{VAC} at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–

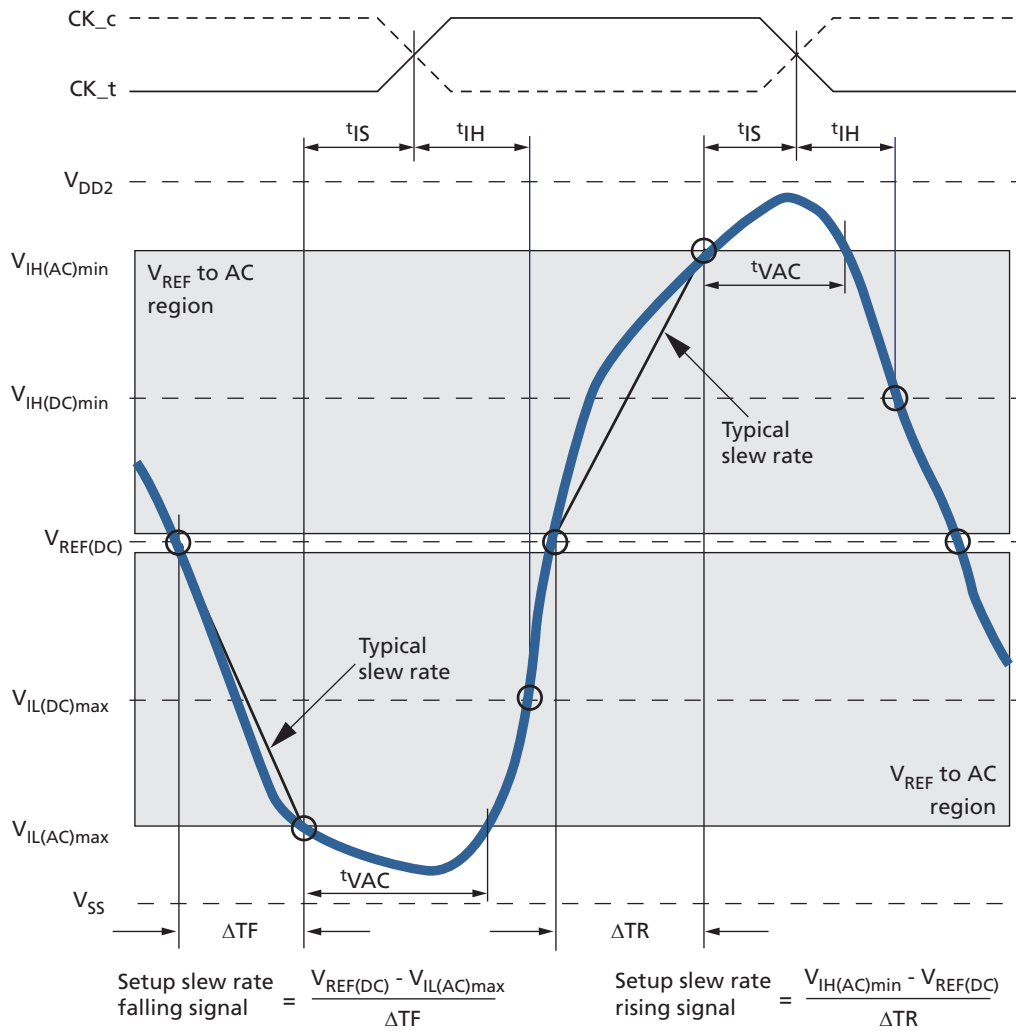

**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
CA and CS_n Setup, Hold, and Derating**
Table 104: Required Time for Valid Transition – $t_{VAC} > V_{IH(AC)}$ and $< V_{IL(AC)}$ (Continued)

Slew Rate (V/ns)	t_{VAC} at 300mV (ps)		t_{VAC} at 220mV (ps)	
	Min	Max	Min	Max
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
CA and CS_n Setup, Hold, and Derating

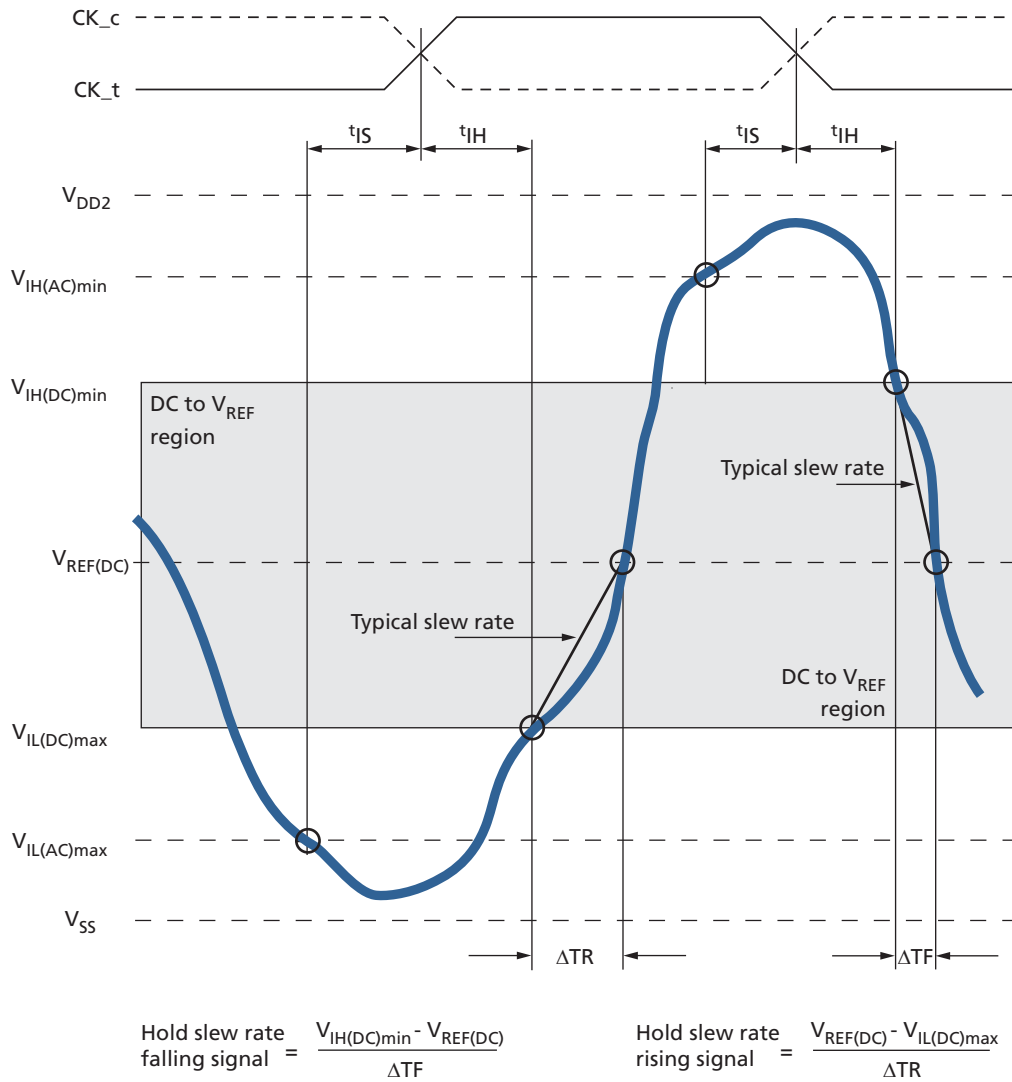
Figure 85: Typical Slew Rate and $t_{VAC} - t_{IS}$ for CA and CS_n Relative to Clock





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
CA and CS_n Setup, Hold, and Derating

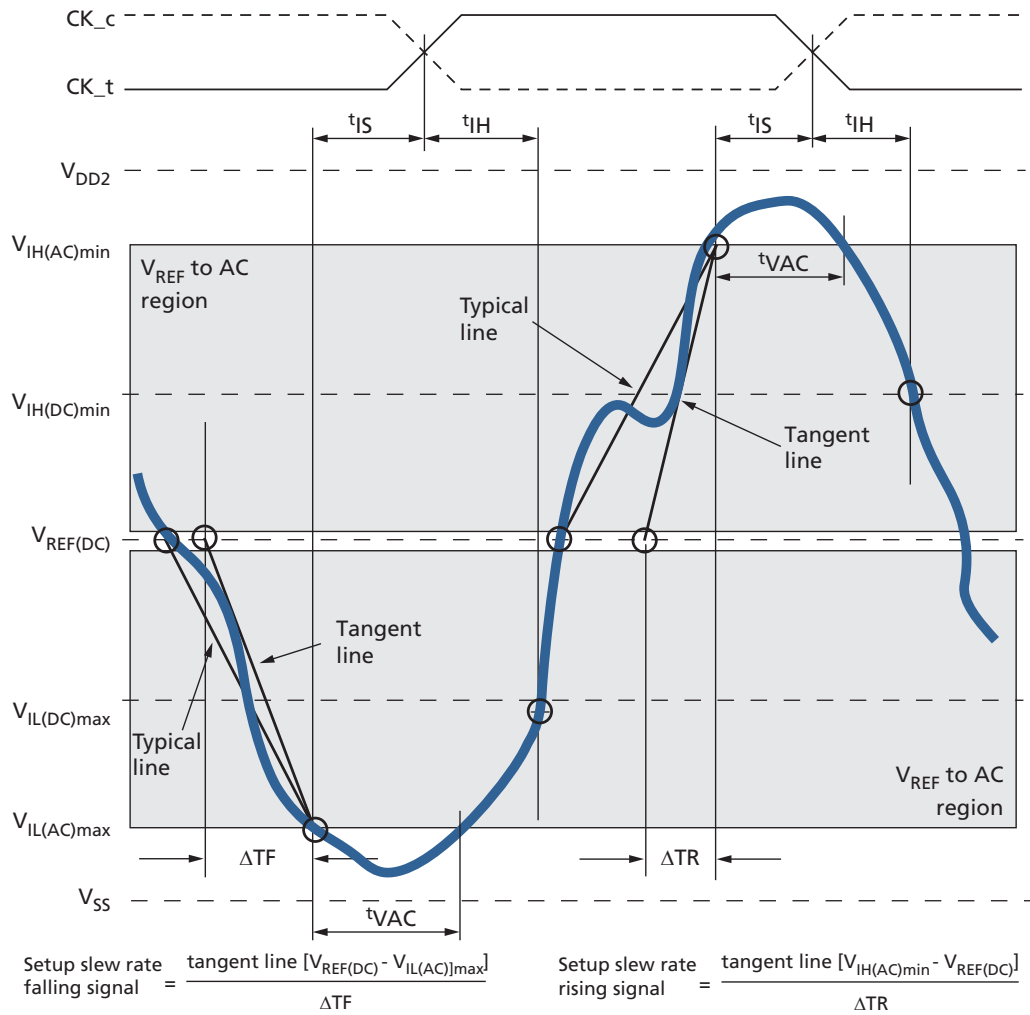
Figure 86: Typical Slew Rate – t_{IH} for CA and CS_n Relative to Clock





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
CA and CS_n Setup, Hold, and Derating

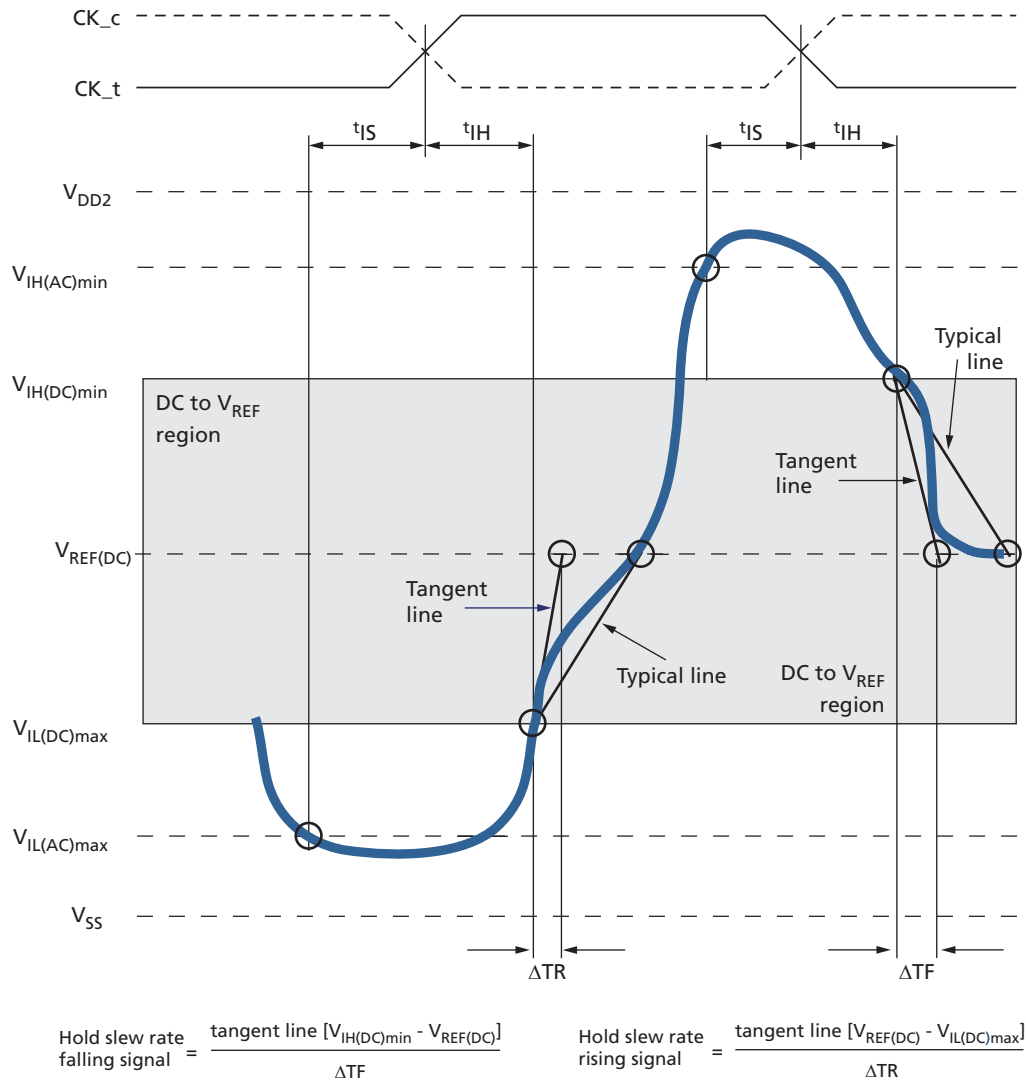
Figure 87: Tangent Line - t_{IS} for CA and CS_n Relative to Clock





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP CA and CS_n Setup, Hold, and Derating

Figure 88: Tangent Line – t_{IH} for CA and CS_n Relative to Clock





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Data Setup, Hold, and Slew Rate Derating

Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) the total required setup time (t_{DS}) and hold time (t_{DH}) are calculated by adding the data sheet $t_{DS}(\text{base})$ and $t_{DH}(\text{base})$ values (see the following table) to the Δt_{DS} and Δt_{DH} derating values, respectively (see the following derating tables). Example: $t_{DS} = t_{DS}(\text{base}) + \Delta t_{DS}$.

The typical t_{DS} slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. The typical t_{DS} slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$ (see the Typical Slew Rate and $t_{VAC} - t_{DS}$ for DQ Relative to Strobe figure).

If the actual signal is consistently earlier than the typical slew rate line in the figure, "Typical Slew Rate and $t_{VAC} - t_{IS}$ for CA and CS_n Relative to Clock (CA and CS_n Setup, Hold, and Derating), the area shaded gray between the $V_{REF(DC)}$ region and the AC region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded $V_{REF(DC)}$ region and the AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see figure "Tangent Line - t_{IS} for CA and CS_n Relative to Clock" in CA and CS_n Setup, Hold, and Derating).

The typical t_{DH} slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. The typical t_{DH} slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$ (see the Typical Slew Rate - DH for DQ Relative to Strobe figure).

If the actual signal is consistently later than the typical slew rate line between the shaded DC-level-to- $V_{REF(DC)}$ region, the typical slew rate should be used for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between shaded DC-to- $V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for the derating value (see the Tangent Line - t_{DH} for DQ with Respect to Strobe figure).

For a valid transition, the input signal must remain above or below $V_{IH}/V_{IL(AC)}$ for the specified time, t_{VAC} (see the Required Time for Valid Transition - $t_{VAC} > V_{IH(AC)}$ or $< V_{IL(AC)}$ table).

The total setup time for slow slew rates could be negative; that is, a valid input signal may not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition. A valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in the following tables, the derating values can be obtained using linear interpolation. Typically, slew rate values are not subject to production testing. They are verified by design and characterization.

Table 105: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
$t_{DS}(\text{base})$	-10	15	50	130	210	230	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220\text{mV}$



**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
Data Setup, Hold, and Slew Rate Derating**

Table 105: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate) (Continued)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
t ^{DS} (base)	80	105	140	220	300	320	V _{IH} /V _{IL(DC)} = V _{REF(DC)} ±130mV

Note: 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS_t/DQS_c slew rate.

Table 106: Data Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate				Reference
	400	333	266	200	
t ^{DS} (base)	180	300	450	700	V _{IH} /V _{IL(AC)} = V _{REF(DC)} ±300mV
t ^{DH} (base)	280	400	550	800	V _{IH} /V _{IL(DC)} = V _{REF(DC)} ±200mV

Note: 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS_t/DQS_c slew rate.

Table 107: Derating Values for AC/DC-Based t^{DS}/t^{DH} (AC220)

Δt^{DS}, Δt^{DH} derating in ps

AC220 Threshold -> V_{IH(ac)}=V_{REF(dc)}+220mV, V_{IL(ac)}=V_{REF(dc)}-220mV

DC130 Threshold -> V_{IH(dc)}=V_{REF(dc)}+130mV, V_{IL(dc)}=V_{REF(dc)}-130mV

		DQS _t , DQS _c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δt ^{DS}	Δt ^{DH}	Δt ^{DS}	Δt ^{DH}	Δt ^{DS}	Δt ^{DH}	Δt ^{DS}	Δt ^{DH}	Δt ^{DS}	Δt ^{DH}	Δt ^{DS}	Δt ^{DH}	Δt ^{DS}	Δt ^{DH}	Δt ^{DS}	Δt ^{DH}
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: 1. Shaded cells are not supported.



**8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
Data Setup, Hold, and Slew Rate Derating**

Table 108: Derating Values for AC/DC-Based t_{DS}/t_{DH} (AC300)

Δt_{DS} , Δt_{DH} derating in ps

AC300 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+300mV$, $V_{IL(ac)}=V_{REF(dc)}-300mV$

DC200 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+200mV$, $V_{IL(dc)}=V_{REF(dc)}-200mV$

		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: 1. Shaded cells are not supported.

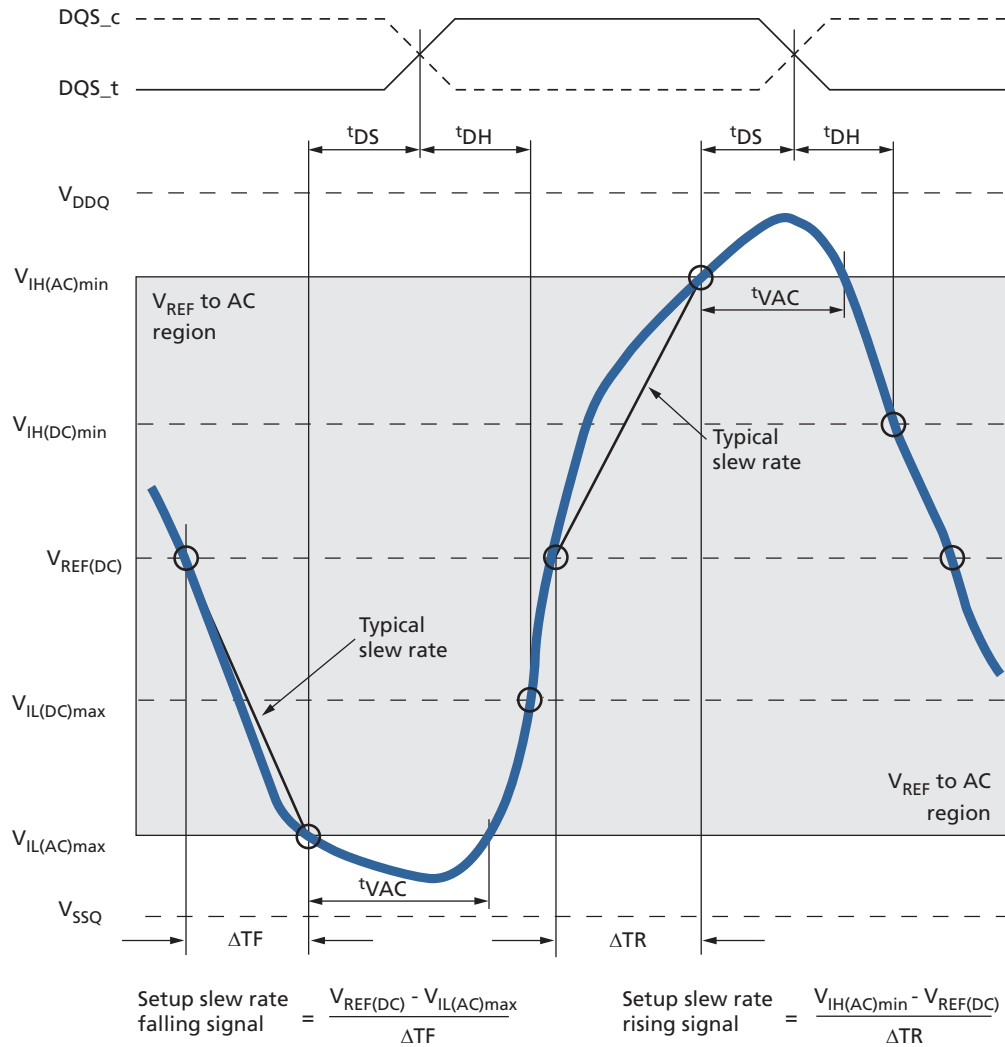
Table 109: Required Time for Valid Transition – $t_{VAC} > V_{IH(AC)}$ or $< V_{IL(AC)}$

Slew Rate (V/ns)	t_{VAC} at 300mV (ps)		t_{VAC} at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–



8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP
Data Setup, Hold, and Slew Rate Derating

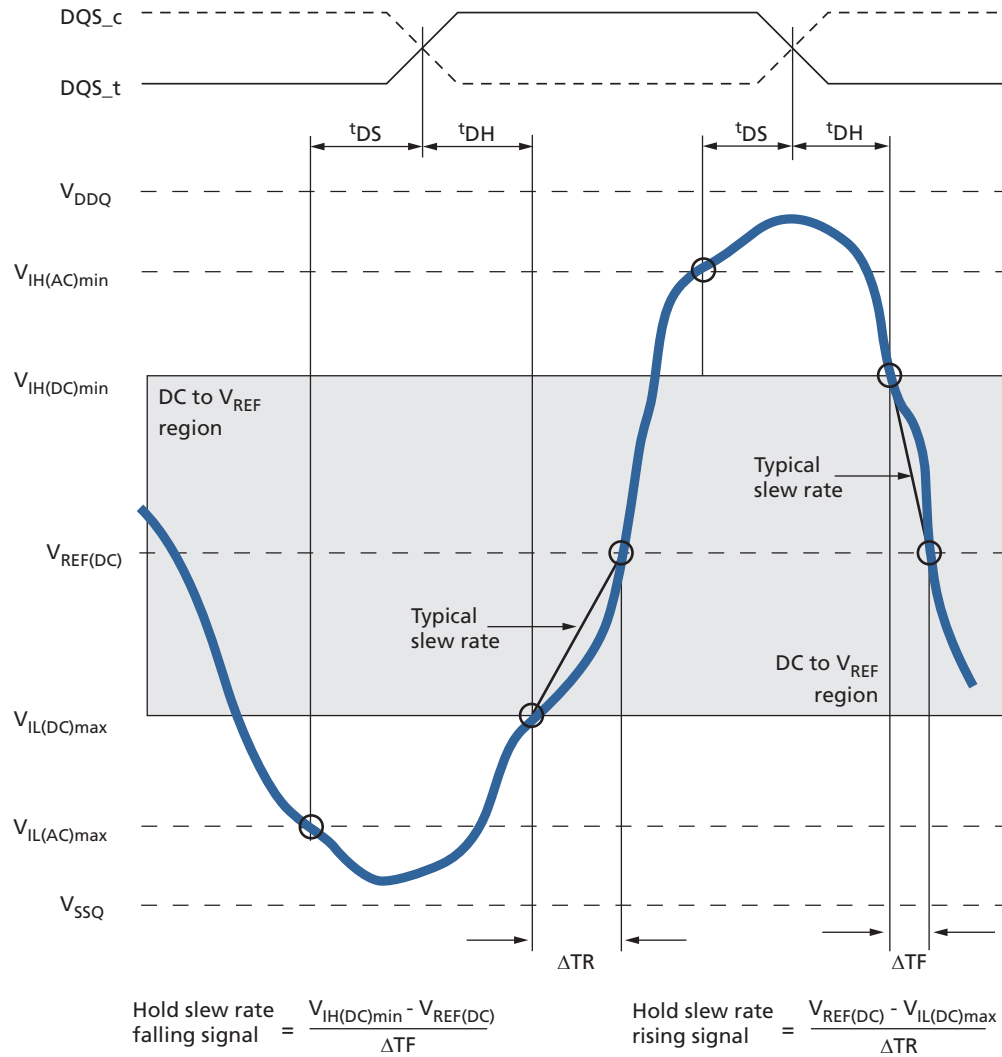
Figure 89: Typical Slew Rate and tVAC – tDS for DQ Relative to Strobe





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Data Setup, Hold, and Slew Rate Derating

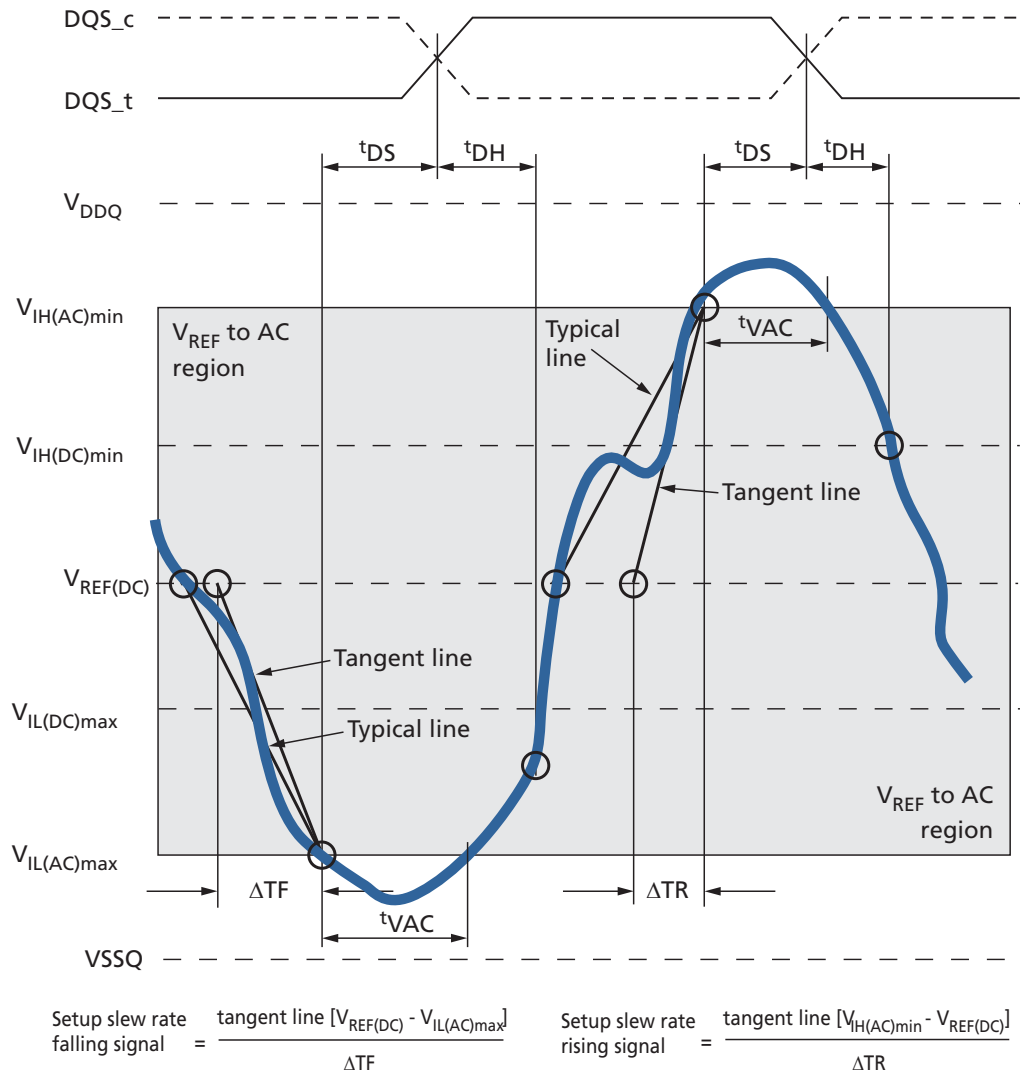
Figure 90: Typical Slew Rate – t_{DH} for DQ Relative to Strobe





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Data Setup, Hold, and Slew Rate Derating

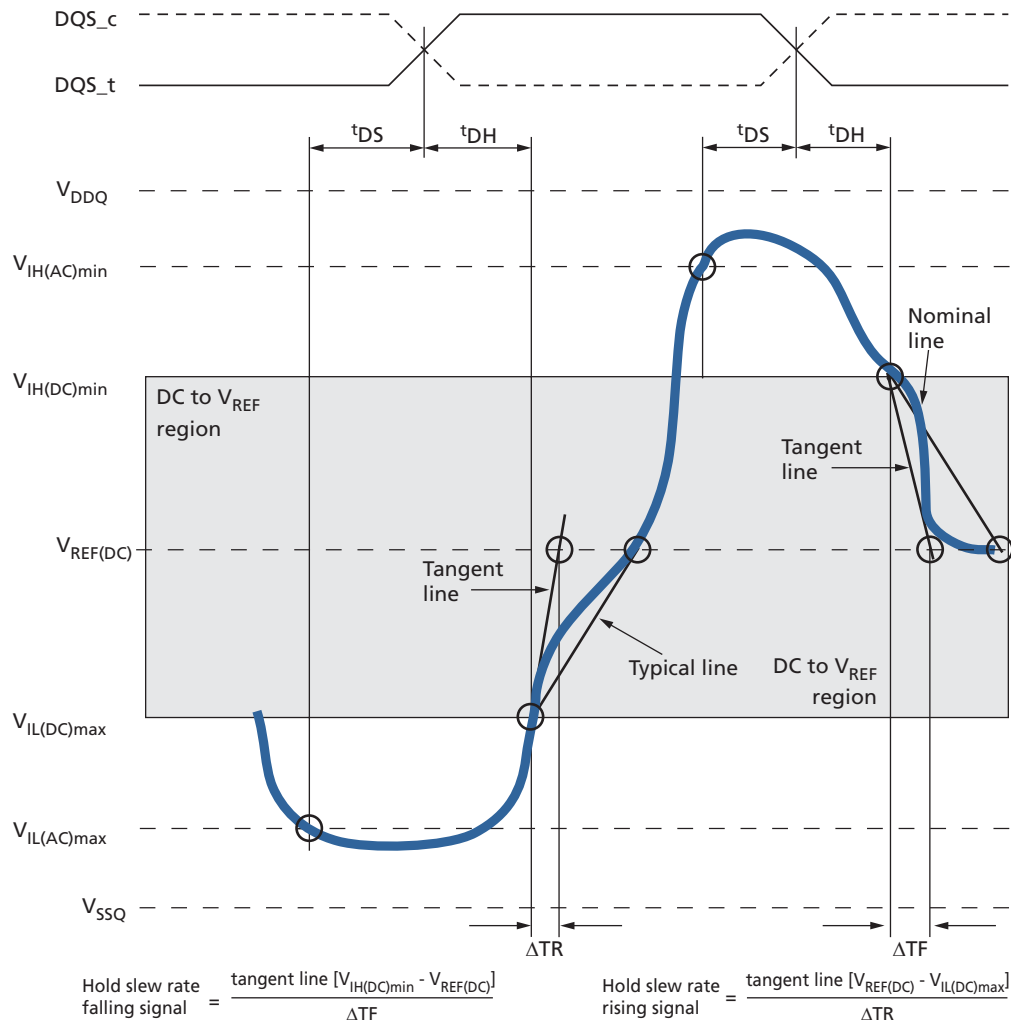
Figure 91: Tangent Line – t_{DS} for DQ with Respect to Strobe





8GB: eMMC and 8Gb: 2 x 4Gb Single-Channel LPDDR2 MCP Data Setup, Hold, and Slew Rate Derating

Figure 92: Tangent Line – t_{DH} for DQ with Respect to Strobe





Revision History

Rev. F – 05/15

- Modified header (title)
- Updated ball assignments figure, ball descriptions tables, and functional block diagram
- Updated CID OID value
- Added performance and current consumption tables
- Updated LPDDR2 section

Rev. E – 07/14

- Updated the CID values in the CID Register Field Parameters

Rev. D – 05/14

- Removed V_{DDCA} signal
- Removed ZQ1 signal
- Updated Signal Description table
- Updated EMCP Figure
- Updated Temperature Range on front page

Rev. C – 03/14

- Updated ball assignments in Ball Assignments and Descriptions

Rev. B – 01/14

- Updated ball assignments in Ball Assignments and Descriptions
- Updated electrical specification for eMMC in eMMC Electrical Specifications

Rev. A – 09/13

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.