O2Micro® Breathing Life into Mobility

OZ8556

1 cell LiIon Charger/Boost Controller

FEATURES

- High accuracy switched mode 1 cell LiIon charger with integrated MOSFETs
- 0.5% voltage mode accuracy
- 3% current mode accuracy
- Maximum charge current up to 4A
- 1MHz operating frequency
- OVP for charging
- Boost with integrated MOSFETs operating from battery voltage > 2.5V when adapter is not present
- Boost output voltage accuracy 5V +/-2%
- Boost Over Current Protection
- Integrated 5V LDO for V5V rail.
- Integrated power by adapter switch for VSYS rail
- Soft start for V5V and VSYS to avoid inrush current from adapter
- OVP/UVP protection for VADP
- UVP threshold adjustable
- VADP can sustain 20V voltage
- Adapter current sensing with programmable adapter current limit, accuracy 3%
- Dynamic Current Allocation
- Integrated 3.3V LDO with 1% output accuracy
- 3.3V DC/DC input voltage selector driving signals
- Over Temperature Protection.
- 12 hours safety timer
- Thermal sensing input

APPLICATIONS

- 1 cell LiIon handheld devices

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ8556LN	0^{o}C to 85^{o}C	QFN28 4x4mm Lead-Free Package

GENERAL DESCRIPTION

OZ8556 is a Charger/Boost Controller specially developed for 1 cell LiIon powered handheld devices such as MID, tablet, smart phone. It offers better performance at a lower cost by integrating 5V boost converter and replacing linear regulator with a switching mode charger. The charger has better efficiency and up to 4A current capability.

The boost converter is optimized to provide high efficiency over a wide load range, with a 20 µA typical current consumption under no load condition.

OZ8556 integrate power by adapter switch for V5V and VSYS rails. It also generates the driving signals for the 3.3V DC/DC input power selector.

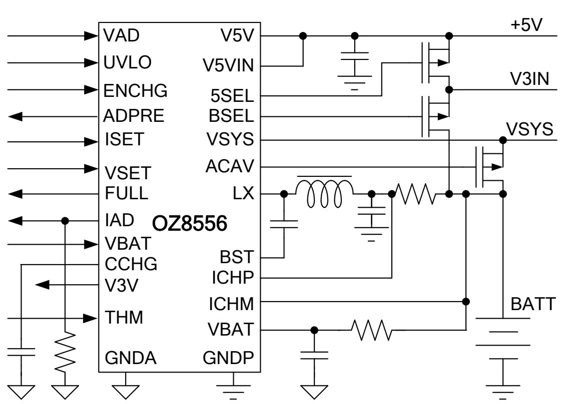
Once V5V is less than rising edge UVP of VADP, the charging will stop if UVLO pin is floating.

An integrated LDO is providing 3.3V/20mA at the V3V output.

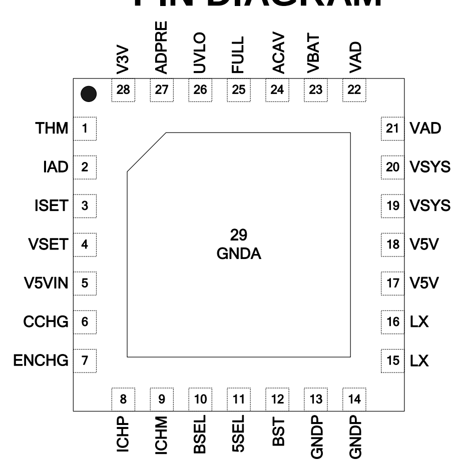
OZ8556 has embedded useful features like:

- Charger Enabling – system can decide to enable or disable the charger
- Over voltage protection for charging, with threshold CV+100mV
- Charge-current setting with wake-up charge (1/10 of normal charge current) for low battery voltage < 3V
- Charge-voltage setting from 3.600V to 4.425V. Voltage Mode CV=3.6+(3.3-VSET)/4
- Adapter available signal - ACAV - lets the system know the adapter is available also drives the power by battery switch.
- Adapter current output with programmable adapter current limit
- Thermistor sensing input to detect the state of the battery and adjust charge current accordingly.
  - No charge for temp < 0ºC
  - No charge for temp > 50ºC
- Battery Full open drain output that can be used to drive an LED for charging status indication.

SIMPLIFIED APPLICATION DIAGRAM



PIN DIAGRAM



BLOCK DIAGRAM

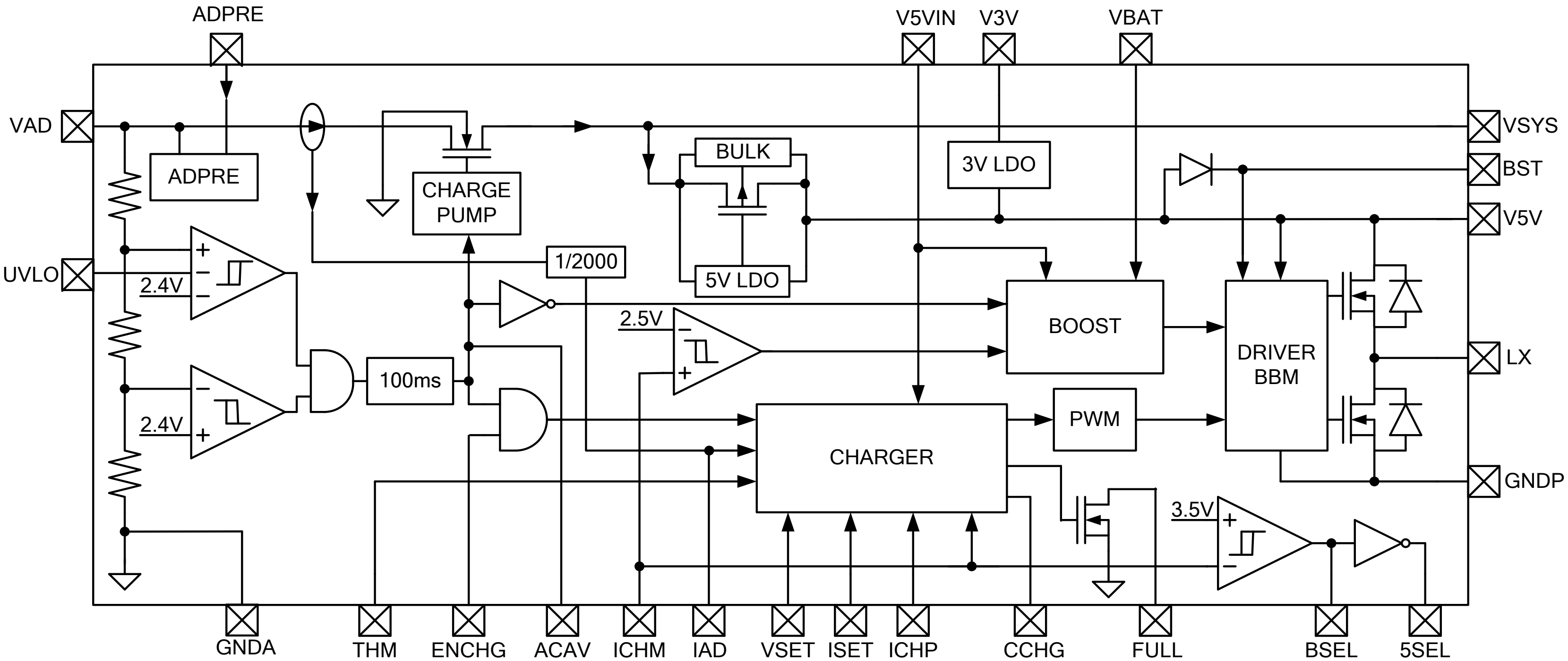


Figure 1: OZ8556 Block Diagram

PIN DESCRIPTION

Pin	Name	I/O	Type	Description
1	**THM**	I	Analog	Thermistor input. If $V_{THM} < 1.0V$, the charging is inhibited. If $1.0V < V_{THM} < 2.4V$ the charger operates normally. If $V_{THM} > 2.4V$ the charging is inhibited.
2	**IAD**	I/O	Analog	Adapter current programming and output pin. Depending on the resistor value placed on this pin the Adapter current limit can be set. The adapter current limit is given by the formula $I_{AD} = 3.3/R_{IAD} \cdot 2000$. So for example for R_{IAD} = 2k the adapter limit is 3.3A. Besides setting the adapter current limit this pin is an output which provides the adapter current information in a linear manner up to the adapter current limit where the output is 3.3V. This information can be used by the system.
3	**ISET**	I	Analog	The voltage applied on this pin defines the voltage drop on the current sense resistor according to the formula $VR_{CS} = V_{ISET}/50$. Therefore the charge current is $I_{CHG} = V_{ISET}/(50 \cdot R_{CS})$.
4	**VSET**	I	Analog	Setting the constant voltage CV = 3.6+(3.3-VSET)/4
5	**V5VIN**	P	Power	Power supply input for the analog circuitry. Use a 1μF capacitor to decouple towards GNDA. Connect to V5V with a resistor.
6	**CCHG**	O	Analog	Compensation pin for charger.
7	**ENCHG**	I	Digital	Charger Enable Pin. Charger is enabled if ENCHG = high and ACAV = high. Charger stops operating when charge current drops below 1/10 of the set current. Charging resumes if the battery voltage drops below CV with typical100mV.
8	**ICHP**	I	Analog	Current sense positive side.
9	**ICHM**	I	Analog	Current sense negative side. Also used to sense the battery voltage.
10	**BSEL**	O	Digital	Output for driving the Battery Switch Gate for the 3.3V DC/DC input rail.
11	**5SEL**	O	Digital	Output for driving the V5V Switch Gate for the 3.3V DC/DC input rail.
12	**BST**	P	Power	Power supply for high side driver
13	**GNDP**	P	Power	Ground for Power section.
14	**GNDP**	P	Power	Ground for Power section.
15	**LX**	P	Power	Switching Node Connection.
16	**LX**	P	Power	Switching Node Connection.
17	**V5V**	P	Power	5V supply for the system. Power for the charger/boost Power Stage.
18	**V5V**	P	Power	5V supply for the system. Power for the charger/boost Power Stage.
19	**VSYS**	P	Power	Power for the system rail VSYS.
20	**VSYS**	P	Power	Power for the system rail VSYS.
21	**VAD**	P	Power	Adapter input.
22	**VAD**	P	Power	Adapter input.
23	**VBAT**	P	Power	Power supply input for the analog circuit when boost works. Use a 1μF capacitor to GNDA. Connect to ICHM through a 100Ω resistor.
24	**ACAV**	O	Digital	Adapter available signal. Logic active high (when high = V5V). Used to drive the power by battery switch gate for VSYS rail.
25	**FULL**	O	Open Drain	Indicates charge terminated. It is pulled low as long as the charger is operating (ENCHG and ACAV are high and charge current > $I_{SET}/10$)
26	**UVLO**	I	Analog	Setting the UVP threshold of adapter VADP. A resistor divider from VADP to GNDA is needed. It compares with internal 2.415V. Better to place a smaller ceramic capacitor from UVLO to GNDA. If leave UVLO floating, default UVP is set internally as 4.75V for rising edge, and 4.70V for falling edge.
27	**ADPRE**	O	Analog	Adapter pre-regulator 4.5V to 7V. A 100nF decoupling capacitor required towards GNDA.
28	**V3V**	O	Power	3.3V LDO output. A 1μF decoupling capacitor required towards GNDA.
29	**GNDA**	P	Power	Ground for the analog circuits.

ABSOLUTE MAXIMUM RATINGS

VAD, UVLO to GNDP (GNDP connected to GNDA) .... -0.3V to +20V
V5V, V5VIN, VSYS to GNDP (GNDP connected to GNDA) .... -0.3V to +6V
ADPRE to GNDA (GNDP connected to GNDA) .... -0.3V to +7V
BST referred to LX .... -0.3V to +6V
LX referred to GNDP and V5V .... GNDP-0.5V to V5V+0.5V
THM, IAD, ISET, VSET, ICHP, ICHM, VBAT to GNDA (GNDP connected to GNDA) .... -0.3V to V5V+0.3V
ENCHG, V3V, BSEL, 5SEL, CCHG to GNDA (GNDP connected to GNDA) .... -0.3V to V5V+0.3V
ACAV to GNDA (GNDP connected to GNDA) .... -0.3V to VSYS+0.3V
FULL to GNDA (GNDP connected to GNDA and 3.3k pull up resistor on FULL pin) .... -0.3V to +6V
Maximum Operating Junction temperature .... +125°C
Storage temperature range .... -55°C to +150°C

NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

VAD to GNDA .... 4.75V to 5.75V
ENCHG .... 0V to V5V
ICHP, ICHM, VBAT .... 0V to 4.5V
THM, ISET, VSET .... 0V to V3V
Operating temperature range (ambient) .... 0°C to 85°C

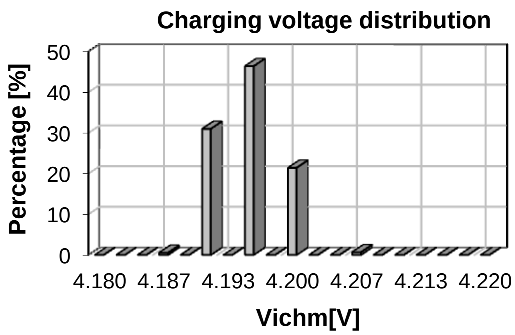
ELECTRICAL SPECIFICATIONS

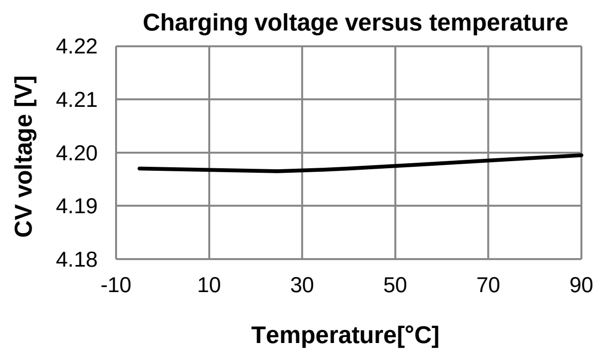
Unless otherwise specified: T_A = 0°C to 85°C, VAD = 5.2V, R_{IAD} = 2kΩ, V_{THM} = 1.5V

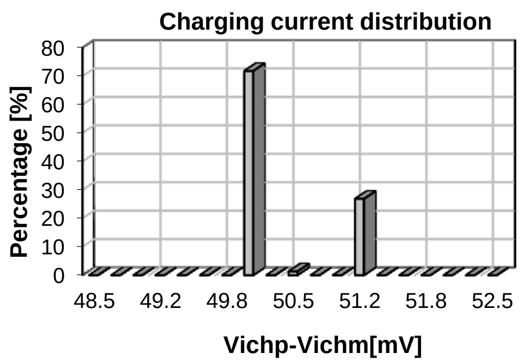
Parameter	Test Conditions	Measured	Limits			Units
			Min	Typ	Max	
Adapter						
Adapter protection threshold	VAD Rising, UVLO is floating	UVP	4.70	4.75	4.80	V
		OVP	5.95	6.00	6.05	V
	VAD Falling, UVLO is floating	UVP	4.65	4.70	4.75	V
		OVP	5.77	5.82	5.87	V
	VAD rising, 1:1 resistor divider from VAD to GNDA	UVP	4.78	4.83	4.88	V
	VAD falling, 1:1 resistor divider from VAD to GNDA	UVP	4.68	4.73	4.78	V
Adapter Power By LDO output voltage	VAD from 4.7V to 5.6V. Load current 1A	V5V	4.6	5.15	5.3	V
V5V Power by adapter MOSFET Rdson	Load current 1A	R(VSYS,V5V)	-	55	-	mΩ
VSYS Power by adapter MOSFET Rdson	Load current 1A	R(VAD,VSYS)	-	55	-	mΩ
Drivers						
High side power MOSFET Rdson	Load current 1A	R(V5V,LX)	-	60	-	mΩ
Low side power MOSFET Rdson	Load current 1A	R(LX,GND)	-	60	-	mΩ
ACAV, BSEL, 5SEL pull up Rdson	Pull down with 250mA		-	5	-	Ω
ACAV, BSEL, 5SEL pull down Rdson	Pull up with 50mA		-	50	-	Ω
BSEL, 5SEL BBM time			-	25	-	ns
FULL low level	Open drain pulled up with 5mA		-	-	0.1	V

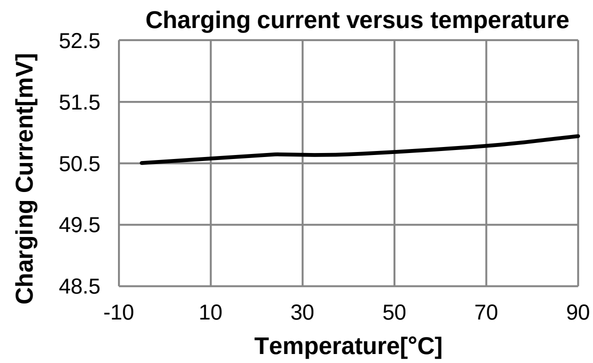
Parameter	Test Conditions	Measured	Limits			Units
			Min	Typ	Max	
Charger Controller						
Voltage Mode (CV)	V_{SET} = 0.9V	V_{ICHM}	4.18	4.2	4.22	V
Current Mode (CC)	V_{ISET} = 2.5V	V_{ICHP} -V_{ICHM}	48.5	50	52.5	mV
Wake-up charge current		V_{ICHP} -V_{ICHM}	3	5.5	8	mV
Wake-up voltage threshold **(V_{WK_TH})**		V_{ICHM}	2.95	3.00	3.05	V
Adapter Current Limit		V_{IAD}	3.25	3.3	3.35	V
Adapter Current Accuracy	I_{VAD} = 2A,R_{IAD}=2kΩ	V_{IAD}	1.95	2.0	2.05	V
THM cold threshold	Temp decreasing. No charge	V_{THM}	2.35	2.40	2.45	V
THM cold hysteresis	Temp increasing. Start charge	V_{THM}	40	100	140	mV
THM hot threshold	Temp increasing. No charge	V_{THM}	0.98	1.00	1.04	V
THM hot hysteresis	Temp decreasing. Start charge	V_{THM}	40	100	140	mV
ENCHG ON Threshold	ENCHG Rising	V_{ENCHG}	1.4	1.5	1.6	V
ENCHG ON hysteresis	ENCHG Falling	V_{ENCHG}	80	150	200	mV
Operating Frequency	ENCHG=high, adapter present	LX	900	1000	1100	kHz
Wake-up Charge Timer	Guaranteed by design		80	90	100	min
Charge Timer	Guaranteed by design		10	12	14	hr
Recharge threshold		CV – V_{ICHM}	70	100	130	mV
OVP_threshold		V_{ICHM} - CV	70	100	130	mV
Boost Controller						
V3IN selector threshold	V_{BATT} decreasing	V_{VBAT}	3.375	3.475	3.575	V
V3IN selector hysteresis	V_{BATT} increasing	V_{VBAT}	50	200	270	mV
V5V accuracy	Boost operating	V_{V5V}	4.9V	5.00	5.1V	V
V3V LDO accuracy	ILOAD < 20mA	V_{V3V}	3.267	3.300	3.333	V
Operating current	No load on V5V		-	20	60	µA
LX negative pulse width (ON-Time)	V_{BATT} = 3V		312	520	728	ns
Battery UVLO threshold	V_{BATT} increasing	V_{VBAT}	2.48	2.58	2.70	V
Battery UVLO hysteresis	V_{BATT} decreasing	V_{VBAT}	50	125	200	mV

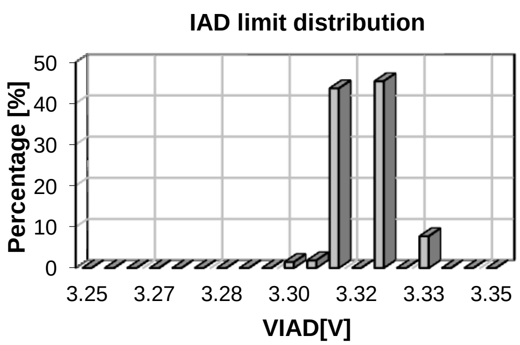
TYPICAL OPERATING CHARACTERISTICS

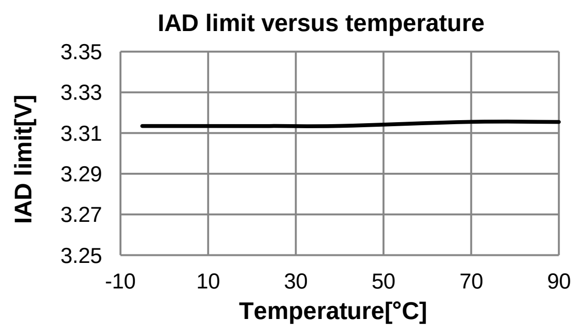


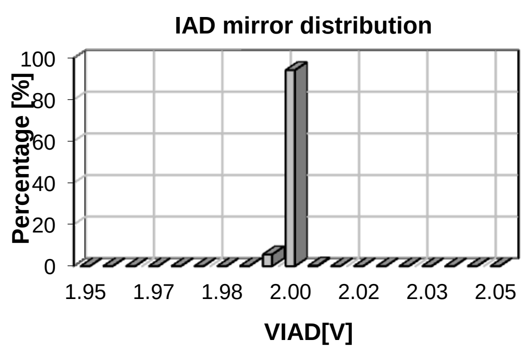


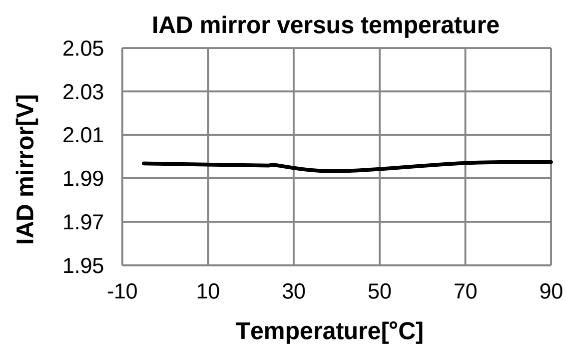




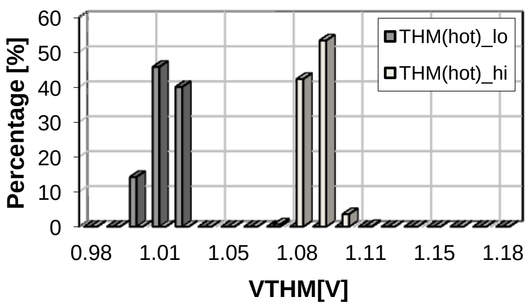




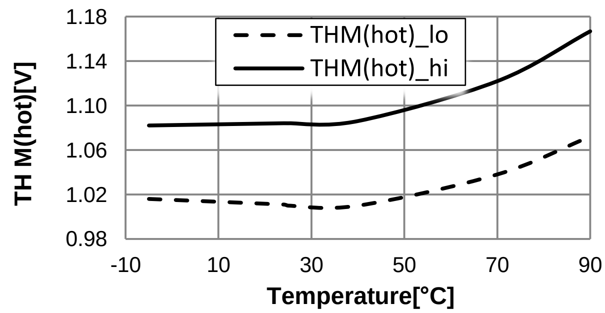




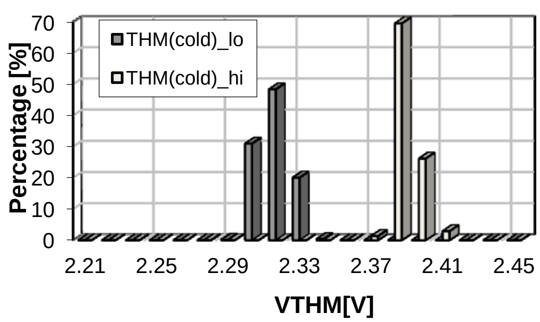
THM(hot) threshold distribution



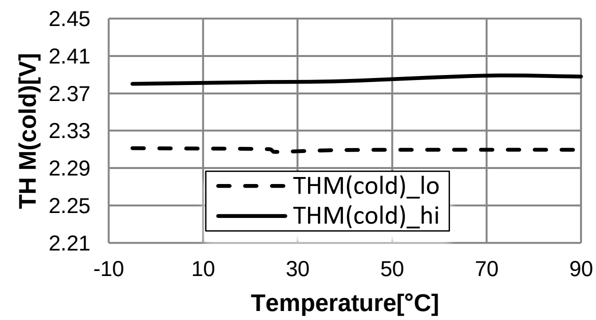
THM(hot) threshold versus temperature



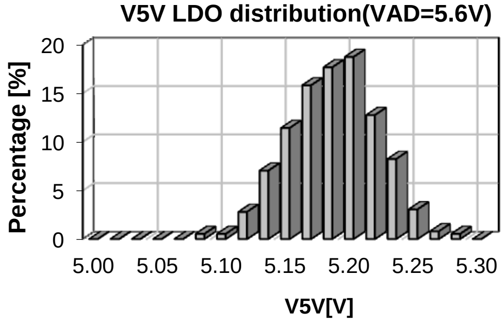
THM(cold) threshold distribution



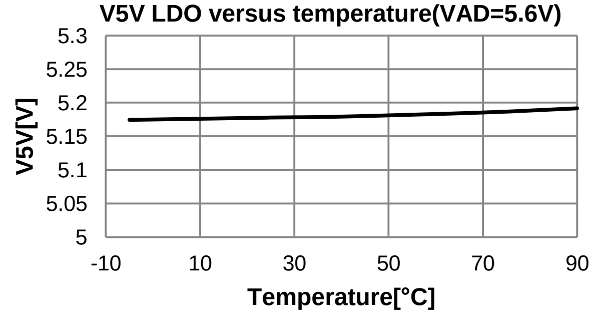
THM(cold) threshold versus temperature



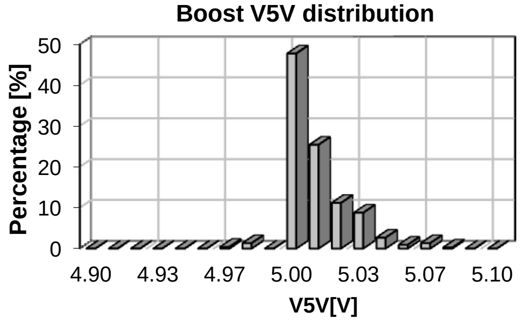
V5V LDO distribution(VAD=5.6V)



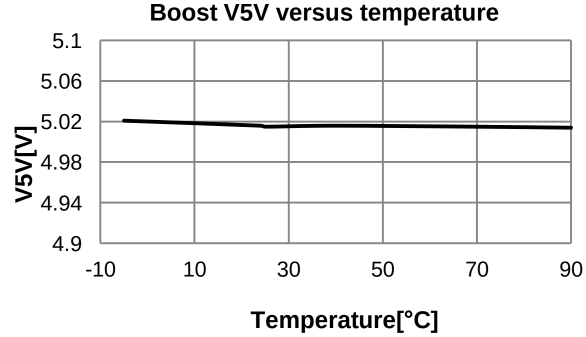
V5V LDO versus temperature(VAD=5.6V)



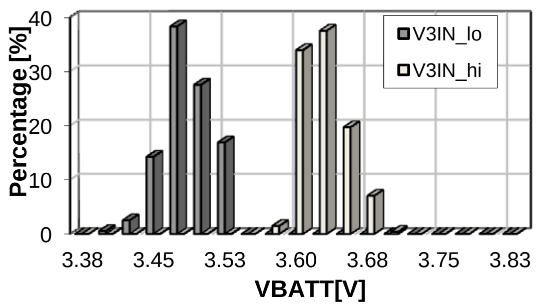
Boost V5V distribution



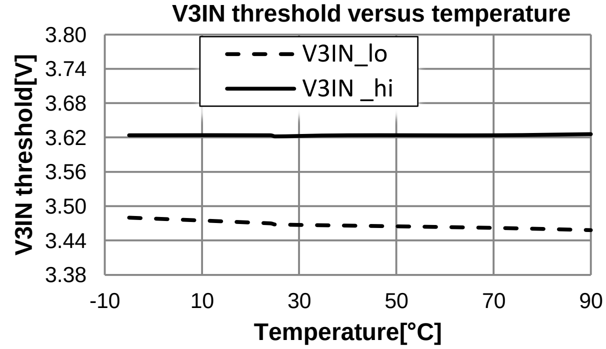
Boost V5V versus temperature



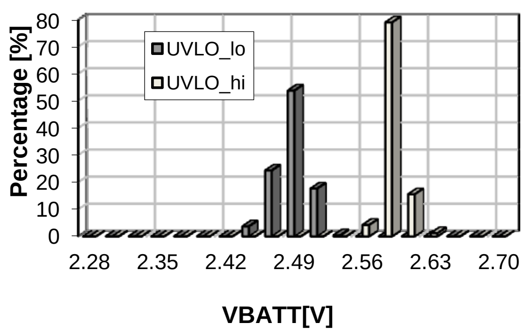
V3IN threshold distribution



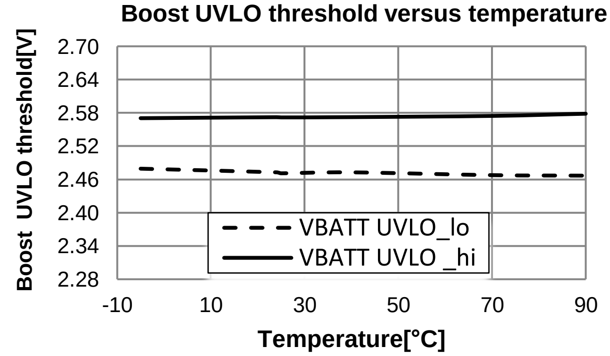
V3IN threshold versus temperature



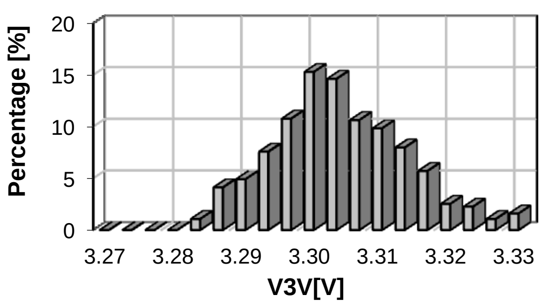
Boost UVLO threshold distribution



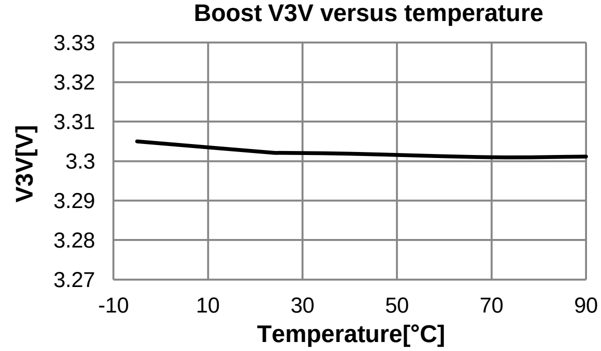
Boost UVLO threshold versus temperature



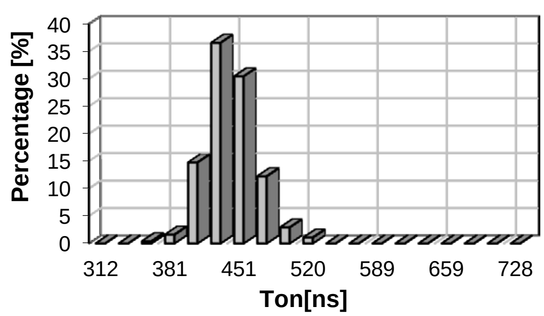
Boost V3V distribution



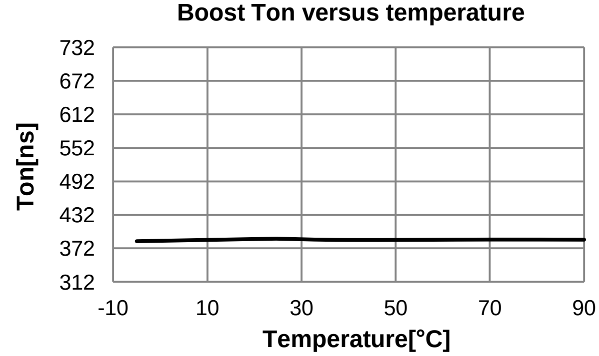
Boost V3V versus temperature



Boost Ton distribution



Boost Ton versus temperature



FUNCTIONAL DESCRIPTION

OZ8556 is a charger/boost controller optimized for 1 cell LiIon batteries. The charger is able to provide up to 4A charge current. The boost is providing 5V on V5V rail while operating from the battery. Both charger and boost are using the same two switch mode integrated MOSFET. OZ8556 does have also integrated two powers by adapter MOSFET used for VSYS system power rail and for V5V power rail. OZ8556 also integrates the power selector drivers for the 3.3V DC/DC input (V3IN on Figure 5) in order to achieve the highest possible efficiency for the system with the benefit of extending the battery life.

Startup Sequence

Startup sequence is shown in Figure 2. ACAV signal is asserted HIGH when the adapter voltage (VAD) exceeds typically 4.75V when UVLO pin is floating and is lower than 6.00V. A delay of more than 100ms is applied to ACAV signal avoiding the inrush current through the internal power switch towards VSYS.

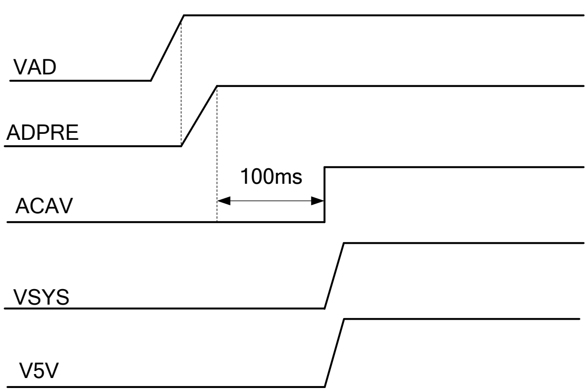


Figure 2: Adapter insertion startup time sequence

Shutdown Sequence

ACAV signal turns LOW when the adapter is removed. The system voltage drops and becomes lower than battery voltage, and then the MOSFET Battery to VSYS (M3 in Figure 5) is turned ON. The system is now powered by battery

Adapter pre-regulator

ADPRE output provides a pre-regulated voltage of 4.5V to 7V from VAD input voltage of 5V to 20V.
The regulated voltage ensures that UVP and OVP functions work when VAD input voltage gets out of range (higher than 6V or lower than 4.75V).

Adapter Available Signal

ACAV signal is providing information to the system that an adapter presence is detected. This signal is also used to drive the VSYS side power by battery switch. ACAV signal is based on the condition that the adapter input VAD pin voltage exceeds typically 4.75V when UVLO pin is floating and it is lower than 6.00V. ACAV is asserted if the adapter voltage remains within the limits for more than 100ms. In order to avoid inrush current the internal power by adapter switch for VSYS will be turned ON only after ACAV signal was asserted high. The V5V power by adapter switch will be turned ON with a minimum delay after the 5V boost is disabled in order to keep this rail valid. The V5V power by adapter switch has also 5V LDO function, keeping the V5V voltage within 4.75V and 5.25V.
If the adapter voltage is higher than 6.00V, ACAV is de-asserted and the internal power by switches for VSYS and V5V are turned OFF.
If UVLO pin is floating and the adapter voltage is lower than 4.75V, ACAV is de-asserted and the internal power switches for VSYS and V5V are turned OFF.
If UVLO pin is connected to external resistor divider, adapter UVP threshold is set by the below formula:

$$V_{AD\_UVP} = 2.415 \times (1 + \frac{R_7}{R_8})\ (V) \quad (1)$$

For example R_7=R_8=100kΩ as in the application schematic, the adapter UVP threshold is 4.83V typical.

Programming Adapter current

When operating from the adapter, the V5V rail is regulated to 5.15V typically by a low dropout regulator which monitors the current passing through it. The system rail VSYS is connected directly to the adapter through an internal switch which monitors the current through it. The information about adapter current available on IAD pin is a sum of VSYS and V5V current. The adapter current limit for dynamic current allocation is programmable through the resistor placed on IAD pin, according to the formula below:

$$I_{AD} = 2000 \times \frac{3.3V}{R_{IAD}(ohm)}\ (A) \qquad (2)$$

Using a typical value of R_{IAD} = 2kΩ, the adapter current limit is 3.3A.

IAD Signal

When adapter is present, OZ8556 provides the adapter current information at IAD pin in a linear manner up to the adapter current limit where the output is 3.3V. This information can be used by the system.

DC/DC buck and DC/DC boost converters

Figure 3 shows the OZ8556 charger/boost architecture that integrates a basic pulse-width-modulated (PWM) buck converter controller as LiIon battery charger with integrated MOSFETs and a basic constant ripple current (CRC) boost converter controller that uses the same internal MOSFETs to provide the 5V rail V5V when operating from the battery that battery voltage is more than 2.5V. The boost converter output voltage accuracy is 5.0V ±2%.

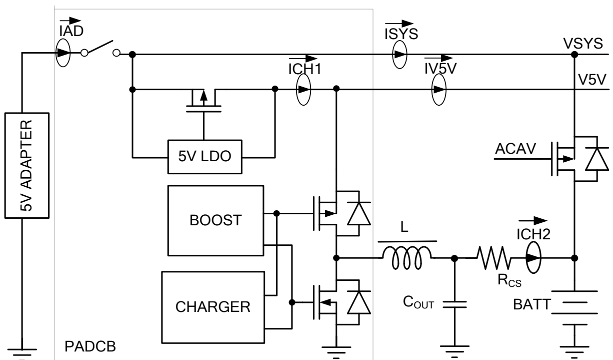


Figure 3: OZ8556 system

Dual High-side current sensing and dynamic current allocation

Figure 3 shows the typical power supply system architecture in PAD. The adapter provides the system current, ISYS, through an internal switch. It also supplies ICH1 current to 5V load of V5V output and ICH2 current to charger through a 5V LDO or an internal switch. It is desirable to have a charger that can charge the battery as fast as possible, even when the system is in use. However, a typical AC adapter has limited current capability, which means that it may not be able to support full operational power of the system and a fast charge current at the same time.
OZ8556 uses the internal MOSFET's R_{DSON} for sensing I_{AD} and one sensing resistor R_{CS} for sensing I_{CH}. The adapter high side current sensing ensures that the current limit of the AC adapter is not exceeded. After supporting the system and V5V power requirements, OZ8556 dynamically diverts all remaining adapter power to the charger by achieving the maximum charge rate.
The other high side current sensor, R_{CS}, is used to detect and regulate the battery charge current. When battery is full, OZ8556 will stop the charging process. If the battery is still functional but deeply discharged (battery voltage below 3V), charging will occur at the wake up value that is 1/10 the normal charge current.
Also note that with the dynamic charge current allocation implemented, the actual charge current, I_{CH2}, may be less than the set value, since it is subject to the following constraint:

$$I_{CH1} \le I_{AD\_MAX} - I_{SYS}$$

$$I_{CH2} = (I_{CH1} - I_{V5V})/D$$

Where I_{AD_MAX} is the adapter current limit, I_{SYS} is the current supplied to the system, I_{V5V} is the current supplied to the V5V load and D is the duty cycle.

Constant Current (CC) and Constant Voltage (CV) Operating Modes

OZ8556 uses three error amplifiers: EA1 for the adapter current limitation, EA2 for charging current regulation, and EA3 for charging voltage regulation. The outputs of these three error amplifiers are connected to CCHG pin for compensation.
Therefore, whenever the AC adapter current limit is exceeded; EA1 output will control the CCHG voltage. The charger's duty cycle will be reduced until the total adapter current falls within its limit value. While operating in constant current mode, the error amplifier EA2 will control the CCHG pin voltage. The circuit operates to regulate the charger output current according to the ISET voltage.
Conversely, while in constant voltage operating mode, the error amplifier EA3 will control the CCHG pin. The circuit operates to regulate the charger output voltage according to VPROG voltage (the output of the Σ-block in **Figure 4**):

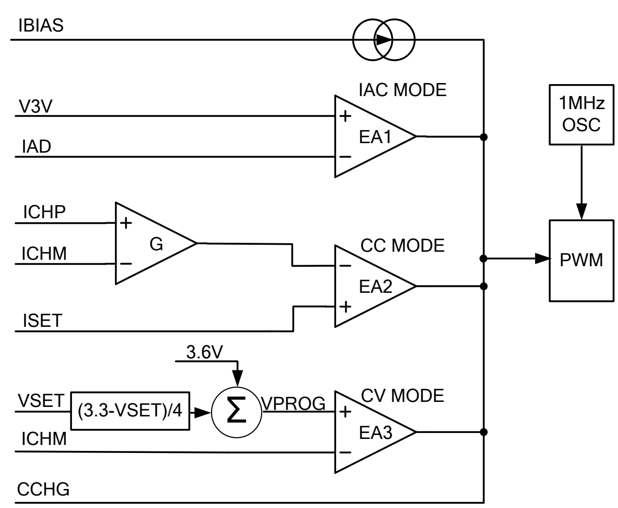


Figure 4: Voltage and Current Regulation

Setting charging current - wake up current

The charging current can be programmed by the voltage applied on the ISET pin, according to the following equation:

$$I_{CHG} = \frac{V_{ISET}}{50 \times R_{CS}} \text{(A)} \qquad (3)$$

The charging current also depends on the value of the sense resistor: R_{CS}. For a 25mΩ resistor and 2.5V V_{ISET}, the charging current is typically 2A. For OZ8556, the maximum charging current is up to 4A.
If the voltage of the charged battery is lower than 3V, the charging current is 1/10 of normal charging current.

Setting Charging Voltage

Depending on the type of LiIon battery the charging voltage (V_{ICHM}) can be programmed through the VSET pin according to the equation:

$$V_{ICHM} = 3.6 + \frac{3.3 - VSET}{4} \text{(V)} \qquad (4)$$

Charge-voltage can be set from 3.600V to 4.425V through VSET pin voltage setting from 3.3V to 0V.For example for a 4.2V constant voltage battery, V_{SET} = 0.9V can be obtained from the resistor divider R1=240kΩ and R2=90kΩ from V3V pin which provides an accurate 3.3V.

Battery Full signal, Charge Indicator

FULL pin is an open drain which is pulled low as long as the charger is operating. It can be used to drive an LED to show the charger activity or using a simple pull-up resistor can offer a battery full signal to the system. Once the charger is operating in CV mode and the charge current drops below 1/10 of the set charge current the charger will automatically turn OFF, signaling to the system on the FULL pin that the battery is fully charged.

Automatic Recharge

The system will continue to monitor the battery voltage. If the battery voltage due to load or self discharge will drop below CV with typical 100mV, the charger will automatically start charging the battery again.

Charger Time Out

The charger has a time out function for wake-up charge and normal charge. For wake-up charge the internal timer is set to typically 90 minutes. After 90 minutes of charging, if the battery voltage didn't exceed 3V, the charger is turned OFF and will not resume operation unless VBATT exceeds 3V. The timer can be reset by inserting a new battery, by plugging out/in the adapter, or by cycling ENCHG signal.
For normal charging the timer is set to 12 hours.
If the charger is still operating after typical 12 hours it will be turned OFF and will resume operating only if the condition (CV- V_{ICHM}) <100mV is met.
The timer can be reset by inserting a new battery, by plugging out/in the adapter, or by cycling ENCHG signal.

Adjusting the HOT and COLD thresholds

The THM input voltage is monitored by 2 comparators (HOT and COLD). If V_{THM} < 1.0V the HOT comparator will assert the "HOT" state and will stop charging. If V_{THM} > 2.4V the COLD comparator will assert the "COLD" state and will stop charging.
In order to make the computations simple, it is recommended to have R_{THM} (25ºC) = R_5. (See Figure 5) In this case the cold threshold is obtained by the ratio R_{THM} (5ºC) / R_5 = 3.125 which is the typical ratio for thermistor from most manufacturers. If needed, R_5 value can be fine tuned to get the proper threshold.
At 45ºC the thermistor resistance typically decreases to 0.43 of the R_{THM} (25ºC) value. This will give the actual trip threshold at around 1.00V. If a higher trip temperature is required, a series resistor can be inserted with the thermistor to adjust the "HOT" threshold.

Battery over Voltage Protection

Battery OVP is assured during normal charging by an over-voltage threshold of CV+100mV typical. When asserted, the charging current stops.

Charging enabling

Normal charging is enabled when all the following conditions are fulfilled:

- ENCHG is high
- ACAV is high
- V_{BATT} > V_{WK_TH}
- No charger time-out and no OTP triggered
- No battery OVP triggered.
- V5V is more than rising edge UVP of VADP when UVLO pin is floating.

Boost enabling

Normal Boost is enabled when all the following conditions are fulfilled:

- ACAV is low
- V_{BATT} > 2.5V
- No boost OTP triggered
- No boost input OCP triggered.

V3IN power selector

The power selector for the 3.3V DC/DC input is controlled by the BSEL and 5SEL outputs which are driving the gates of the corresponding MOSFETs. There is an internal BBM of typically 25ns between these 2 signals to avoid shoot through between the V5V rail and battery. The output drivers pull up resistance is typically 5Ω in order to turn OFF the MOSFET fast, and the pull down resistance is typically 50Ω in order to turn them ON slow. This will avoid inrush current into the decoupling capacitor of 3.3V DC/DC input. When the adapter is plugged IN, BSEL is high and 5SEL is low. When the adapter is not present and battery voltage is over 3.5V, BSEL is low and 5SEL is high.

Over Temperature Protection

Over Temperature Protection is activated if the die temperature exceeds typically 145ºC.
When the adapter is present and OTP is triggered, the charger and power by adapter switches are turned OFF. When the adapter is not present, it turns OFF the boost converter.

Boost Input Over Current Protection

Boost OCP is triggered if LX voltage on Ton time exceeds 0.52V. In that case the boost converter is turned OFF and is latched.

Boost OCP can be reset by reinserting the battery.
The real boost protection current I_{OCP} on Ton time is as the following equation:

$$I_{OCP} = \frac{V_{LX}}{R_{dson\_lowsideswitch}} \text{ (A)} \qquad (5)$$

Micro Controller Interface

OZ8556 can be easily implemented and interfaced with a micro-controller. It has 3 input and 3 output ports meant for two-way communications.
ISET, VSET inputs are used to set the charging parameters. ENCHG pin is used to set whether charging or not.
ACAV, FULL and IAD outputs provide the status Information to the host system.

TYPICAL APPLICATION SCHEMATIC

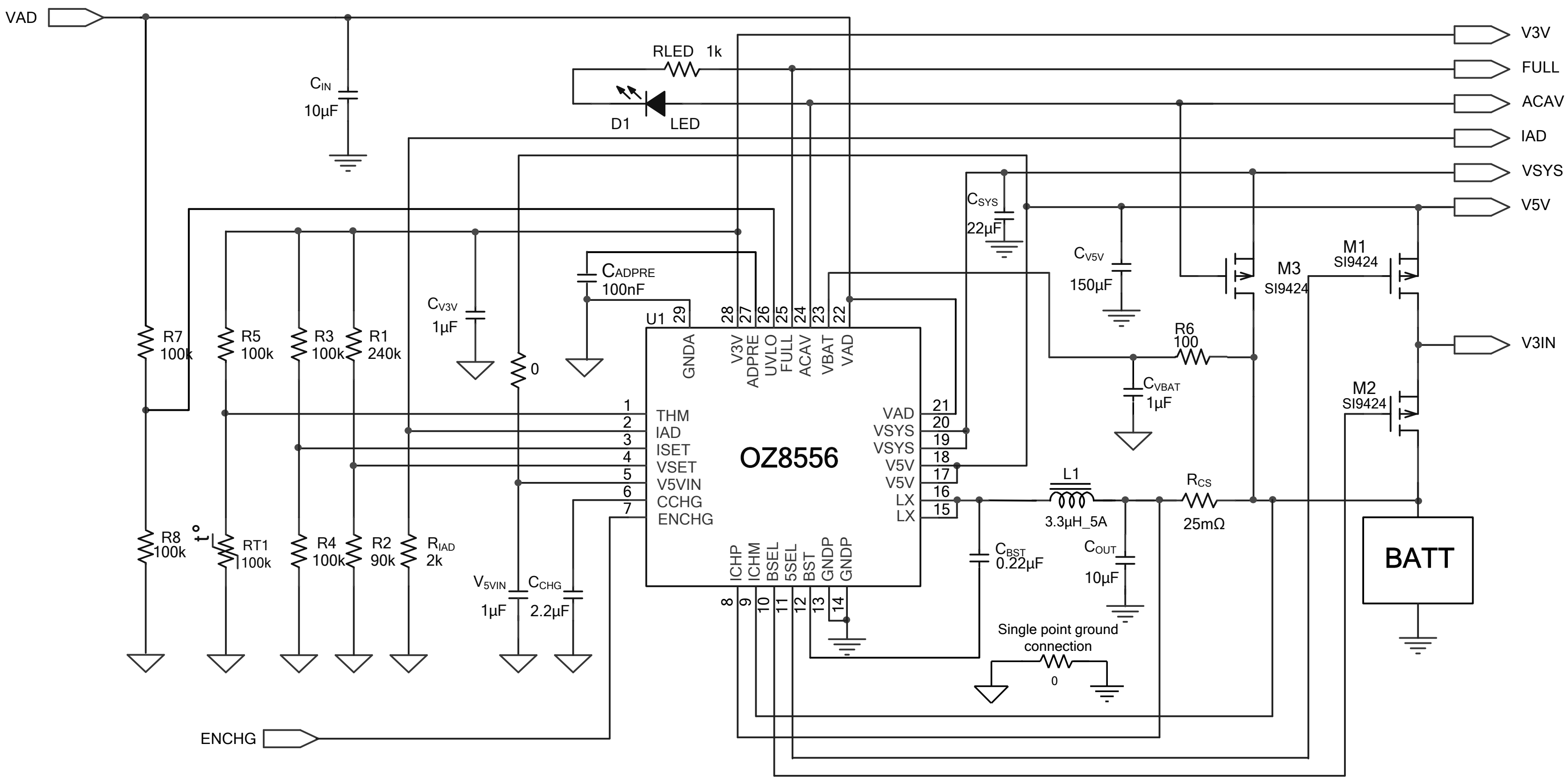


Figure 5: OZ8556 Typical Application Schematic

BILL OF MATERIALS

Item	Qty	Reference	Value	Vendor	Part Number	PCB Footprint
1.	1	R1	240k 1%	Any	-	0603
2.	1	R2	90K 1%	Any	-	0603
3.	5	R3, R4, R5,R7,R8	100k 1%	Any	-	0603
4.	1	R6	100Ω 1%	Any	-	0603
5.	1	R_{IAD}	2k 1%	Any	-	0603
6.	1	R_{ICHP}	1.5k 1%	Any	-	0603
7.	1	R_{LED}	1k 5%	Any	-	0603
8.	1	R_{CS}	25mΩ 1%	Any	-	1210
9.	2	C_{V5VIN},C_{CHG}	2.2µF/6.3V	Any	-	0805
10.	1	C_{IN}	10µF/25V	Any	-	1210
11.	1	C_{OUT}	10µF/6.3V	Any	-	1206
12.	1	C_{V5V}	150µF/6.3V	Any	-	SPCAP
13.	1	C_{V3V},	1µF/6.3V	Any	-	0603
14.	1	C_{SYS}	22µF/6.3V	Any	-	1210
15.	1	C_{ADPRE}	100nF	Any	-	0603
16.	1	C_{VBAT}	1µF/6.3V	Any	-	0603
17.	1	C_{BST}	0.22uF/6.3V	Any	-	0603
18.	1	L1	3.3µH/5A	TRIO Technology	EM-33AM05V01	7.3x6.9x3mm
19.	3	M1, M2, M3	-	Fairchild	SI9424	SO-8
20.	1	D1	LED	Any	-	-
21.	1	**U1**	**-**	**O2Micro**	**OZ8556**	**QFN28**

COMPONENT SUPPLIERS

Manufacturer	Contact Information	
	Phone	Website
Power MOSFETs		
Vishay	1-402-563-6866	www.vishay.com
Fairchild	1-703-478-5800	www.fairchildsemi.com
Inductors		
Vishay	1-402-563-6866	www.vishay.com
TRIO Technologies	011-886-2-8227-9268	www.trio-tw.com
TOKO	1-408-432-8281	www.toko.com
Diode		
Vishay	1-402-563-6866	www.vishay.com
Fairchild	1-703-478-5800	www.fairchildsemi.com
Capacitors		
Taiyo-Yuden		www.t-yuden.com
Johanson Dielectrics	1-818-364-9800	www.johansondielectrics.com
TDK	1-800-344-2112	www.tdk.com
Resistors		
Vishay	1-402-563-6866	www.vishay.com
TDK	1-800-344-2112	www.tdk.com

PCB LAYOUT RECOMMENDATIONS

In order to achieve low switching losses and a stable PWM operation there are certain guidelines that should be followed when PCB layout is done.

The power and signal ground should be routed as separated nets and connected together in a single point, preferably at the negative terminal of the battery. The signal ground should be laid out as a copper shape preferably on an internal layer that covers the area under the IC and the components placed near the IC that need to be connected to the signal ground. This will be like a local signal ground separated from the ground plane. All components connected to the signal ground should use vias to connect to the local signal ground.

The decoupling capacitors on V5VIN, V3V, ADPRE, CCHG, UVLO and VBAT to GNDA as well as VSYS and VAD towards GNDP should be placed as close as possible to the IC.

The decoupling capacitors on BST to LX should be placed as close as possible to the IC.

The noisy switching loop formed by the input decoupling capacitors, internal power switches, inductor, and output decoupling capacitors should be kept as small as possible to minimize EMI radiation. The feedback signals from the current sense resistor should be routed as short as possible avoiding the noisy areas. Kelvin connections are recommended at the current sense resistors.

For detailed PCB layout and routing recommendations, consult OZ8556 User Guide**.**

APPLICATION PERFORMANCE CHARACTERISTICS

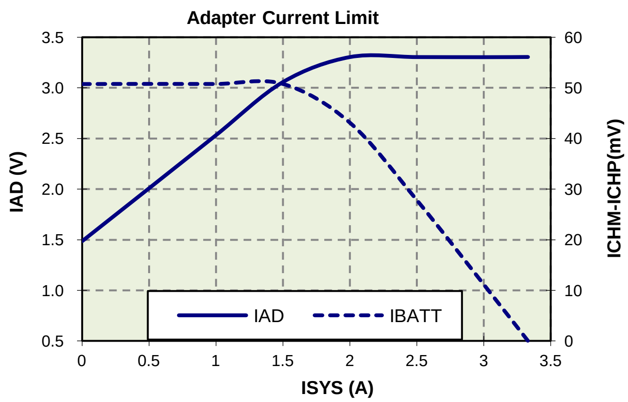


Figure 6: Adapter current limit

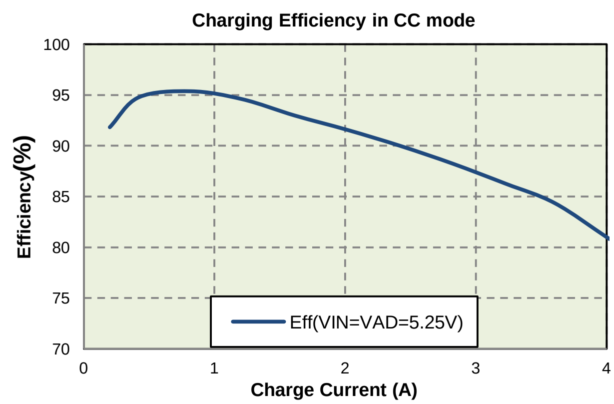


Figure 7: Charger efficiency (VAD = 5.25V, VBATT = 3.6V)

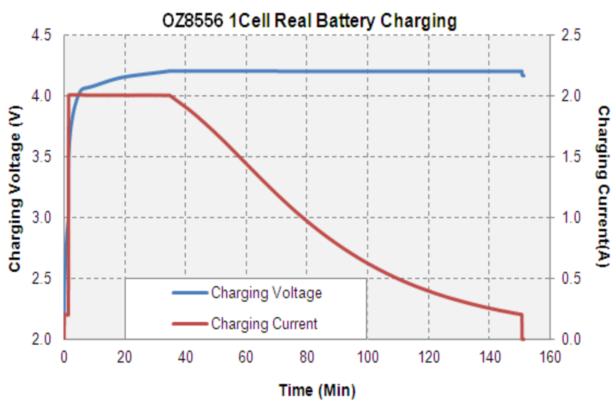


Figure 8: 1-cell real battery charging test

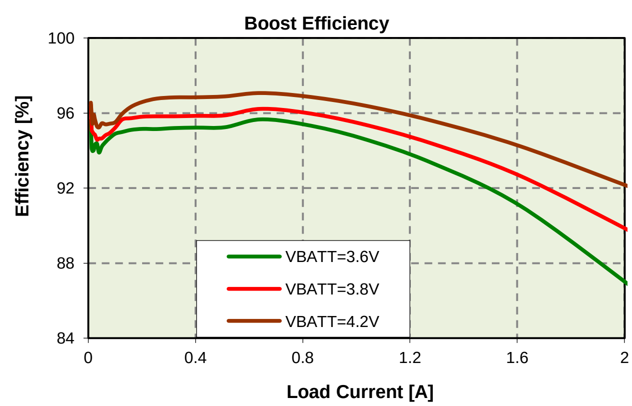


Figure 9: Boost converter efficiency

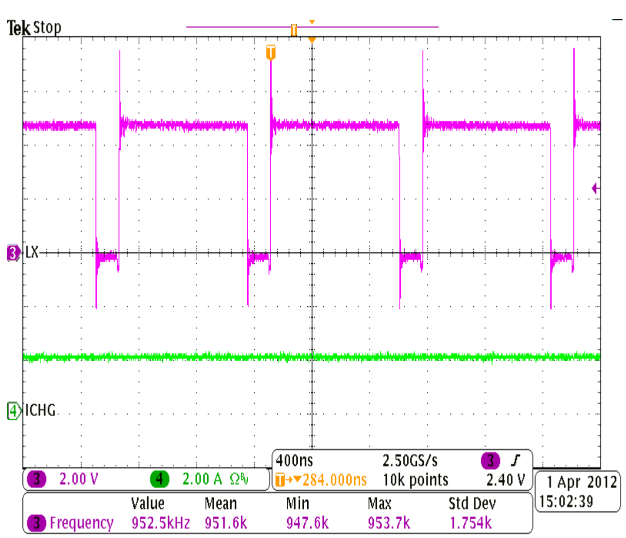


Figure 10: LX waveform, 2A charge current,

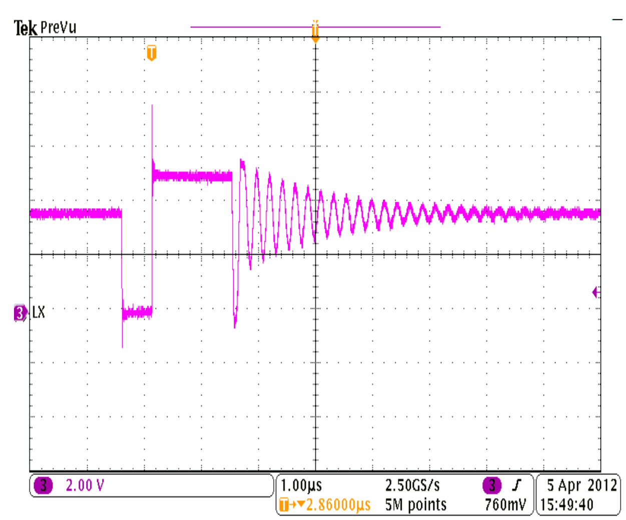
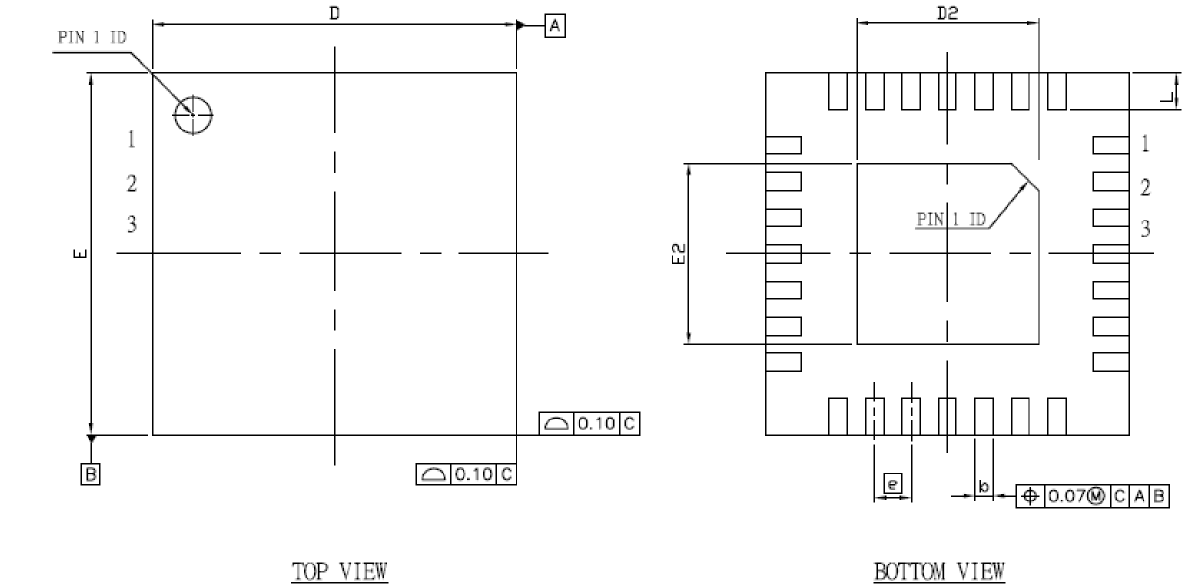


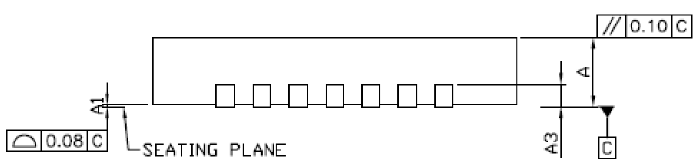
Figure 11: Boost LX waveform, V_{ICHM} = 4.0V and I_{V5V} = 0A

PACKAGE INFORMATION – 28 PIN QFN (4x4mm)

Exposed pad is GNDA (pin 29) and must be fully soldered to PCB

28Ld QFN 4x4mm Package Outline Drawing





SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	4.00 BSC		
D2	1.85	2.00	2.15
E	4.00 BSC		
E2	1.85	2.00	2.15
e	0.40 BSC		
L	0.30	0.40	0.50

Notes:
1. ALL DIMENSIONS ARE IN MILLIMETER
2. REFER TO JEDEC STD MO−220

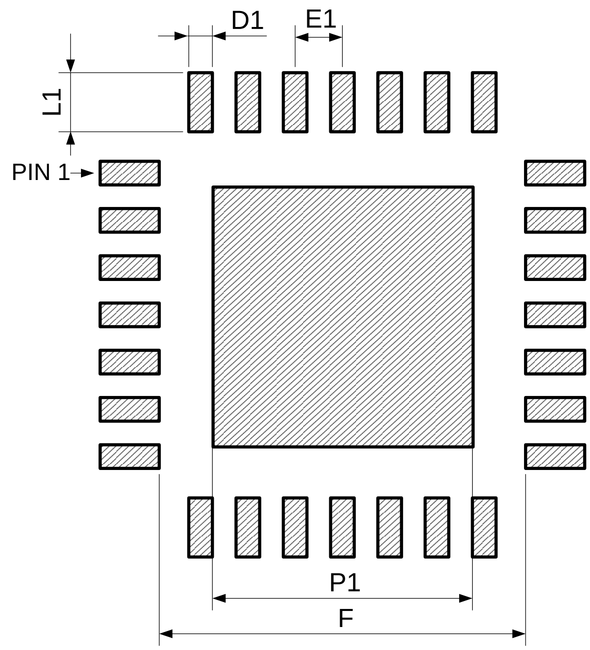
Rth j-a (QFN-28 4x4mm package) = 34ºC/W
Rth j-c (QFN-28 4x4mm package) = 4.6ºC/W

DIMENSION TABLE

SYMBOL	SPECIFICATION
	28L QLP 4X4 BODY
D1	0.20
E1	0.40
L1	0.90
P1	2.10
F	3.00

All dimensions are given in millimeters.

RECOMMENDED LANDING PATTERN



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